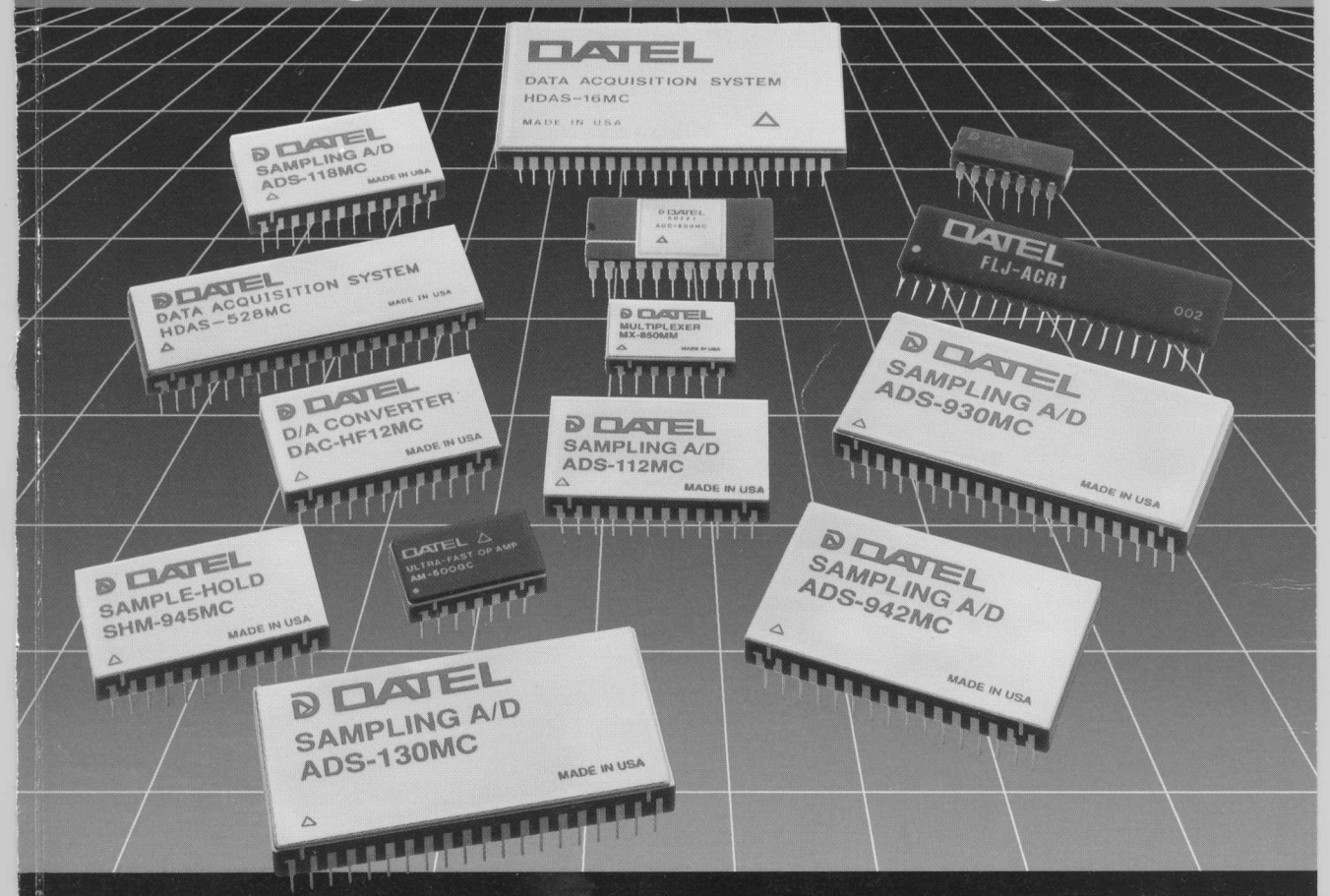
DATEL

DATABOOK VOLUME 1

COMPONENTS



INNOVATION AND EXCELLENCE IN PRECISION DATA ACQUISITION

COMPANY HISTORY

Founded in 1970, DATEL is a multinational company located approximately 35 miles south of Boston in Mansfield, Massachusetts. Our modern 180,000 square-foot facility houses our administrative offices, components and sub-systems engineering groups, modular and sub-systems production facilities, and the most modern thin-film and thick-film hybrid production facility in the industry. DATEL's hybrid manufacturing operation is a fully certified MIL-STD-1772 facility, supporting our high quality standards.

Our worldwide sales network extends to every major data acquisition product marketplace. The people who implement this sales network are skilled professionals dedicated to providing our customers with the highest possible standards of data acquisition products available today.

PRODUCT INFORMATION

DATEL offers one of the industry's broadest data acquisition product lines, meeting the rapidly growing need for components and sub-systems to interface with computers in industrial, commercial, scientific and military applications. These products employ five basic technologies: monolithic CMOS, monolithic bipolar, thin-film hybrid, thick-film hybrid and discrete component circuits. Many products employ a combination of these technologies to achieve higher levels of performance and complexity. The present product lines include: data converters, sample-hold amplifiers, analog multiplexers, amplifiers, data acquisition sub-systems, computer analog I/O boards, process monitor/controllers, digital panel meters, thermal printers, digital calibrators and power supplies.

DATEL

PRODUCT INDEX

Section 1. Sampling Analog-to-Digital Converters

Section 2. Analog-to-Digital Converters

Section 3. Digital-to-Analog Converters

Section 4. Sample/Hold Amplifiers

Section 5. Hybrid Data Acquisition Systems

Section 6. Analog Multiplexers

Section 7. Amplifiers

Section 8. Active Filters

HOW TO USE THIS DATABOOK

If you know the **MODEL NUMBER**, use the Product Index on the first page.

If you know the **PRODUCT TYPE**, refer to the Subject Index on page two to determine the proper section, then refer to the **SELECTION GUIDE TABLE** at the beginning of that section.

If you want **PRICE** and **AVAILABILITY** information contact your local DATEL salesperson or representative.

For all **OTHER INFORMATION**, such as New Product Highlights, Available Literature, available High Reliability Product Programs, a listing of available DESC drawings, Substitution Guide and Ordering Guide, use the Subject Index.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

GENERAL INDEX

AVAILABLE LITERATURE

DATEL'S ALL NEW DATA ACQUISITION HANDBOOK SERIES

The following additional Handboods are presented in complete data sheet format and include Selection Guides, Application Notes, and Ordering Information.

Volume 2. Data Acquisition Boards
DVME, Multibus, PC Bus

Volume 3. Industrial Monitor and Control Products
Process Monitors, Digital Panel Meters, Thermal Panel Printers, Bench-top and Hand-held Calibrators

Volume 4. Power Products
DC/DC Converters, Power Supplies

Also available are the following Application Notes:

AN-1 High-Speed A/D Converter Designs: Layout and Interfacing Pitfalls

AN-2 Picking the Right Sample-and-Hold Amp for Various Data Acquisition Needs

AN-3 Data Converters: Getting to Know Dynamic Specifications

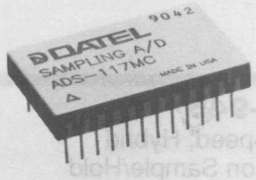
Data Acquisition and Conversion Handbook:
A technical guide to A/D - D/A converters and their applications.

NEW PRODUCTS

ADS-117
12-Bit, 2.0 MHz, Low-Power
Sampling A/D Converter

Features

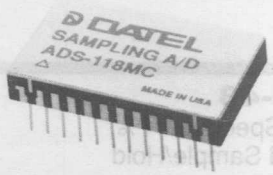
- 2.0 MHz minimum throughput
- Functionally complete
- Small 24-pin DIP
- Low-power, 1.4 Watts
- Three-state output buffers
- Samples to Nyquist



ADS-118
12-Bit, 5.0 MHz, Low-Power
Sampling A/D Converter

Features

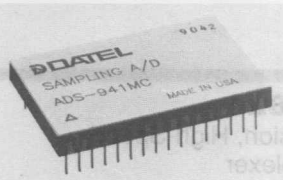
- 5.0 MHz minimum throughput
- Functionally complete
- Small 24-pin DIP
- Low-power, 2.3 Watts
- Three-state output buffers
- Samples to Nyquist



ADS-941
14-Bit, 1.0 MHz, High Resolution
Sampling A/D Converter

Features

- 1.0 MHz minimum throughput
- Functionally complete
- Small 32-pin DIP
- Low-power, 2.8 Watts
- Three-state output buffers
- Samples up to Nyquist



ADS-942
14-Bit, 2.0 MHz, High Resolution
Sampling A/D Converter

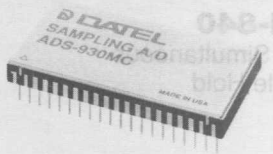
Features

- 2.0 MHz minimum throughput
- Functionally complete
- Small 32-pin DIP
- Low-power 2.9 Watts
- Three-state output buffers
- Samples up to Nyquist

ADS-930
16-Bit, 500 KHz, High Resolution
Sampling A/D Converter

Features

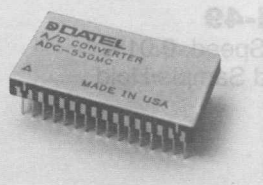
- 500 KHz sampling rate
- Functionally complete
- Small 40-pin DIP
- Low-power, 1.8 Watts
- Three-state output buffers
- Samples up to Nyquist
- 16-Word FIFO memory



ADC-530
12-Bit,Ultra-Fast, Low-Power
A/D Converter

Features

- 350 nSec MAX. conversion time
- Low-power, 2.1 Watts
- Small initial errors
- Three-state output buffers
- Small 32-pin DIP
- No missing codes



NEW PRODUCTS

HDAS-950/951
16-Bit, 100 KHz
Data Acquisition Systems

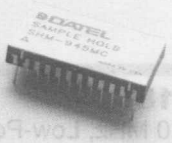
Features

- 16-bit resolution, 100 KHz
- 8 SE 4 D channels
- Miniature 40-pin DDIP
- Full-scale gain range from 100 mV to 10V
- High-impedance output state

SHM-945
High-Speed, Hybrid
Precision Sample/Hold

Features

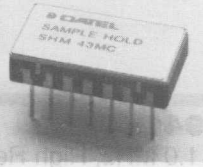
- 500 nSec MAX acquisition time to 0.00076%
- Differential input
- 0.0004% linearity
- 16-bit performance over military temperature range
- Small 24-pin DDIP package
- Operates at different gain settings



SHM-43
High-Speed, 0.01%
Hybrid Sample/Hold

Features

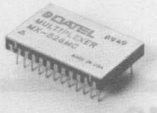
- 35 nS MAX acquisition time to 0.01%
- 1 Picosecond aperture uncertainty
- 75 MHz small-signal bandwidth
- 520 Milliwatt maximum power dissipation
- Small 14-pin DIP package
- CMOS control signal



MX-826
Precision, High-Speed
Multiplexer

Features

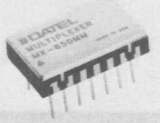
- 225 nSec Max. settling time to 0.01%
- 400 nSec. Max. settling time to 0.003%
- 150 nSec. Max. settling time to 0.1%
- 8 Channels single-ended inputs
- 395 Milliwatts power dissipation
- Small 24-pin DDIP package



MX-850
Precision, High Speed
Multiplexer

Features

- 50 Nanoseconds settling time to 0.01%
- 70 Nanoseconds settling time to 0.003%
- 100 Nanoseconds settling time to 0.001%
- 4 Channels, single-ended inputs
- 207 Milliwatts power dissipation
- Small 14-pin DIP package



MSH-840
Quad Simultaneous
Sample Hold

Features

- 4 Simultaneous sample/holds
- Internal 4 channel multiplexer
- 750 nSec acquisition time, 10V step to 0.01%
- 2 channels with optional X10 gain
- Control logic for interfacing to A/D's
- Low-power, 1.5 Watts

SHM-49
High-Speed, 0.01%
Hybrid Sample/Hold

Features

- 16 MHz small signal bandwidth
- Small 8-pin DIP or LCC package
- 200 nS Max. acquisition time to 0.01%
- 72 dB feedthrough attenuation
- ±25 Picoseconds aperture uncertainty
- 413 Milliwatts power dissipation

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ADS-120
12-Bit, 20 MHz
Sampling A/D Converter

Features

- 20 MHz minimum throughput
- Samples to Nyquist
- Functionally complete
- Small 40-pin DIP
- Low-power, 4.2 Watts
- Three-state output buffers
- High input bandwidth

ADS-944
14-Bit, 5.0 MHz, High Resolution
Sampling A/D Converter

Features

- 5.0 MHz minimum throughput
- Functionally complete
- Small 32-pin DIP
- Low-power, 3.4 Watts
- Three-state output buffers
- Samples to Nyquist

ADS-945
14-Bit, 10.0 MHz, High Resolution
Sampling A/D Converter

Features

- 10 MHz sampling rate
- Functionally complete
- Small 40-pin DIP
- Low-power, 4.2 Watts
- Three-state output buffers
- Samples up to Nyquist
- 16-Word FIFO memory

ADS-976
16-Bit, 200 KHz, Low-Power
Sampling A/D Converter

Features

- 200 KHz sampling rate
- Compatible to industry standard ADC76, AD376, AD1376
- Small 32-pin DIP
- Low-power, 1.8 Watts
- Samples to Nyquist
- 16-Word FIFO memory

FLT-DL
4- and 5- Pole High Frequency
Digitally Programmable
Active Filters

Features

- Digitally programmable
- 4- and 5-pole CAUER response
- Cascadable 7-pole CAUER response
- Cutoff frequencies to 1.2 MHz
- Small 32-pin DIP
- -55 to +125 °C operation

NEW PRODUCTS

ADS-120
12-Bit, 20 MHz
Sampling A/D Converter

Features

- 20 MHz minimum throughput
- Samples to Nyquist
- Functionally complete
- Small 40-pin DIP
- Low-power, 4.2 Watts
- Three-state output buffers
- High input bandwidth

ADS-944
14-Bit, 5.0 MHz, High Resolution
Sampling A/D Converter

Features

- 5.0 MHz minimum throughput
- Functionally complete
- Small 32-pin DIP
- Low-power, 3.4 Watts
- Three-state output buffers
- Samples to Nyquist

ADS-945
14-Bit, 10.0 MHz, High Resolution
Sampling A/D Converter

Features

- 10 MHz sampling rate
- Functionally complete
- Small 40-pin DIP
- Low-power, 4.2 Watts
- Three-state output buffers
- Samples up to Nyquist
- 16-Word FIFO memory

ADS-976
16-Bit, 200 KHz, Low-Power
Sampling A/D Converter

Features

- 200 KHz sampling rate
- Compatible to industry standard ADC76, ADZ76, AD1376
- Small 32-pin DIP
- Low-power, 1.8 Watts
- Samples to Nyquist
- 16-Word FIFO memory

FLT-DIL
4- and 5- Pole High Frequency
Digitally Programmable
Active Filters

Features

- Digitally programmable
- 4- and 5-pole CAUER response
- Cascadable 7-pole CAUER response
- Cutoff frequencies to 1.2 MHz
- Small 32-pin DIP
- -55 to +125 °C operation

SAMPLING A/D CONVERTERS

	Model	Resolution (Bits)	Throughput (MHz)	Linearity Error (Max)	Power Watts (Max)	Case	Page
	ADC-HS12B	12	0.066	±3/4 LSB	1.8	32-Pin DIP	2-51
	ADS-111	12	0.500	±3/4 LSB	1.8	24-Pin DIP	1-1
	ADS-112	12	1.0	±3/4 LSB	1.7	24-Pin DIP	1-5
	ADS-193	12	1.0	±3/4 LSB	1.7	40-Pin DIP	1-35
	ADS-21PC	12	1.3	±1 LSB	2.5	46-Pin DIP	1-39
	ADS-132	12	2.0	±3/4 LSB	3.2	32-Pin DIP	1-31
Preliminary	**ADS-117**	12	2.0	±3/4 LSB	1.8	24-Pin DIP	1-9
Preliminary	**ADS-118**	12	5.0	±1 LSB	2.5	24-Pin DIP	1-13
	ADS-131	12	5.0	±1 LSB	4.0	40-Pin DIP	1-25
	ADS-130	12	10.0	±1 LSB	4.2	40-Pin DIP	1-19
Advanced	**ADS-120**	12	20.0	±1 LSB	4.2	40-Pin DIP	1-17
	ADS-924	14	0.300	±1 LSB	1.8	24-Pin DIP	1-43
	ADS-928	14	0.500	±3/4 LSB	3.4	32-Pin DIP	1-47
Preliminary	**ADS-941**	14	1.0	±3/4 LSB	3.3	32-Pin DIP	1-53
Preliminary	**ADS-942**	14	2.0	±1 LSB	3.4	32-Pin DIP	1-57
Advanced	**ADS-944**	14	5.0	±1 LSB	3.4	40-Pin DIP	1-61
Advanced	**ADS-945**	14	10.0	±1 LSB	4.2	40-Pin DIP	1-63
Advanced	**ADS-976**	16	0.200	±2 LSB	1.8	32-Pin DIP	1-65
Preliminary	**ADS-930**	16	0.500	±1 1/2 LSB	2.4	40-Pin DIP	1-51

Contact DATEL for your
Data Acquisition component
needs.

Dial
1-800-233-2765
for
Applications Assistance

ADS-111

12-Bit, 500 KHz, Low-Power Sampling A/D Converter

FEATURES

- **12-Bit resolution**
- **Internal Sample/Hold**
- **500 KHz minimum throughput**
- **Functionally complete**
- **Small 24-pin DIP**
- **Low-power, 1.4 Watts**
- **Three-state output buffers**
- **No missing codes**

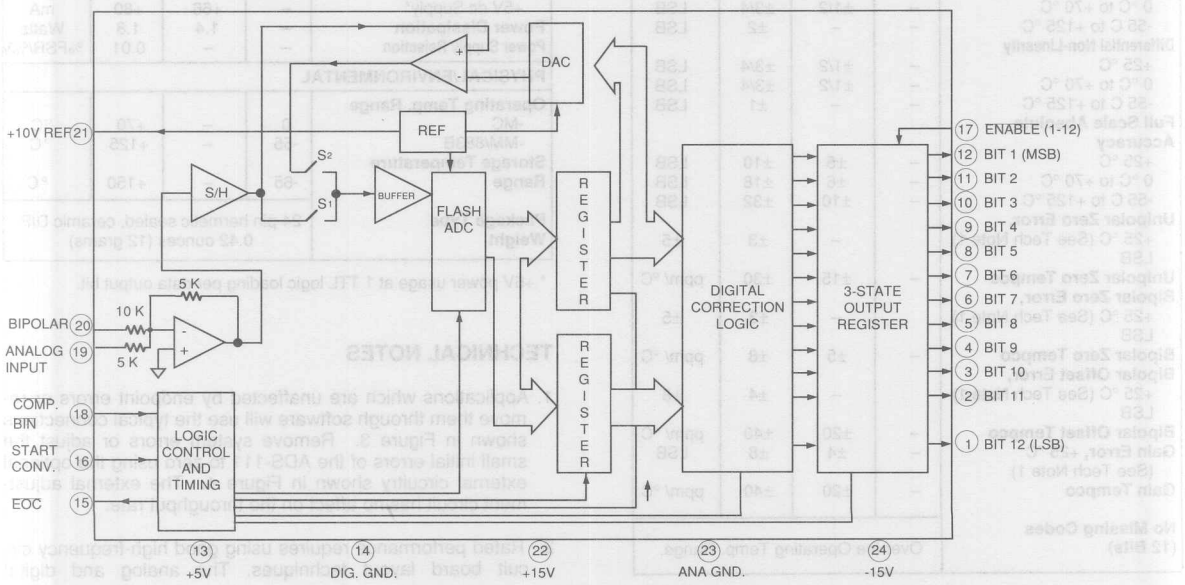
GENERAL DESCRIPTION

DATEL's ADS-111 is a 12-bit, functionally complete, sampling A/D converter that is packaged in a space-saving 24-pin ceramic DIP. A minimum throughput rate of 500 KHz is achieved while only dissipating 1.4 Watts.

Manufactured using thick-film and thin-film hybrid technology, a proprietary chip and unique laser trimming schemes, the ADS-111's exclusive performance is based upon a digitally-corrected subranging architecture.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 OUT (LSB)	13	+5V
2	BIT 11 OUT	14	DIGITAL GROUND
3	BIT 10 OUT	15	EOC
4	BIT 9 OUT	16	START CONVERT
5	BIT 8 OUT	17	ENABLE (1-12)
6	BIT 7 OUT	18	COMP BIN
7	BIT 6 OUT	19	ANALOG INPUT
8	BIT 5 OUT	20	BIPOLAR
9	BIT 4 OUT	21	+10V REF
10	BIT 3 OUT	22	+15V
11	BIT 2 OUT	23	ANALOG GROUND
12	BIT 1 OUT (MSB)	24	-15V



ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 22)	0 to +18	Volts dc
-15V Supply (Pin 24)	0 to -18	Volts dc
+5V Supply (Pin 13)	-0.5 to +7.0	Volts dc
Digital Inputs (Pins 16, 17, 18)	-0.3 to +6.0	Volts dc
Analog Input (Pin 18)	-15 to +15	Volts dc
Lead Temp.(10 Sec.)	300 max	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and +5V dc unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range				
ADS-111	–	±5	–	Volts dc
(See Table 4 also)	–	0 to +10	–	Volts dc
Input Impedance	5.0	15.0	–	M Ohms
Input Capacitance	–	3	5	pf
DIGITAL INPUTS				
Logic Levels				
Logic "1"	2.0	–	–	Volts dc
Logic "0"	–	–	0.8	Volts dc
Logic Loading "1"	–	–	5.0	µA
Logic Loading "0"	–	–	-200	µA
A/D PERFORMANCE				
Integral Non-Linearity				
+25 °C	–	±1/2	±3/4	LSB
0 °C to +70 °C	–	±1/2	±3/4	LSB
-55 C to +125 °C	–	–	±2	LSB
Differential Non-Linearity				
+25 °C	–	±1/2	±3/4	LSB
0 °C to +70 °C	–	±1/2	±3/4	LSB
-55 C to +125 °C	–	–	±1	LSB
Full Scale Absolute Accuracy				
+25 °C	–	±5	±10	LSB
0 °C to +70 °C	–	±6	±18	LSB
-55 C to +125 °C	–	±10	±32	LSB
Unipolar Zero Error, +25 °C (See Tech Note 1)		–	±3	±5 LSB
Unipolar Zero Tempco	–	±15	±30	ppm/ °C
Bipolar Zero Error, +25 °C (See Tech Note 1)		–	±3	±5 LSB
Bipolar Zero Tempco	–	±5	±8	ppm/ °C
Bipolar Offset Error, +25 °C (See Tech Note 1)		–	±4	±8 LSB
Bipolar Offset Tempco	–	±20	±40	ppm/ °C
Gain Error, +25 °C (See Tech Note 1)	–	±4	±8	LSB
Gain Tempco	–	±20	±40	ppm/ °C
No Missing Codes (12 Bits)	Over the Operating Temp. Range.			

OUTPUTS	MIN.	TYP.	MAX.	UNITS
Logic Levels				
Logic "1"	2.4	–	–	Volts dc
Logic "0"	–	–	0.4	Volts dc
Logic Loading "1"	–	–	-160	µA
Logic Loading "0"	–	–	6.4	mA
Internal Reference Voltage, +25 °C	+9.98	+10.0	+10.02	Volts dc
Drift.	–	±5	±30	ppm/ °C
External Current	–	–	1.5	mA
Resolution	12 Bits			
Output Coding				
(Pin 18 Hi)	Straight binary/offset binary			
(Pin 18 Low)	Complementary binary / Complementary offset binary			
DYNAMIC PERFORMANCE				
Conversion Rate				
+25 °C	500	600	–	KHz
0 °C to +70 °C	500	600	–	KHz
-55 C to +125 °C	500	–	–	KHz
Total Harmonic Distortion				
DC to 60 KHz at Vin ≤5V p-p	-65	-70	–	dB
DC to 40 KHz at Vin = 10V p-p	-65	-70	–	dB
Slew Rate	–	90	–	V/µSec.
Aperture Delay Time	–	20	–	nSec.
Aperture Uncertainty	–	±100	–	pSec.
S/H Acquisition Time to 0.01% (10V step)				
+25 °C	–	–	715	nSec.
0 °C to +70 °C	–	–	765	nSec.
-55 °C to +125 °C	–	–	900	nSec.
(Sinusoidal Input)	–	–	465	nSec.
POWER REQUIREMENTS				
Power Supply Range				
+15V dc Supply	+14.25	+15.0	+15.75	Volts dc
-15V dc Supply	-14.25	-15.0	-15.75	Volts dc
+5V dc Supply	+4.5	+5.0	+5.5	Volts dc
Power Supply Current				
+15V dc Supply	–	+38	+50	mA
-15V dc Supply	–	-36	-47	mA
+5V dc Supply*	–	+66	+80	mA
Power Dissipation	–	1.4	1.8	Watts
Power Supply Rejection	–	–	0.01	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range				
-MC	0	–	+70	°C
-MM/883B	-55	–	+125	°C
Storage Temperature Range	-65	–	+150	°C
Package Type	24-pin hermetic sealed, ceramic DIP			
Weight	0.42 ounces (12 grams)			

* +5V power usage at 1 TTL logic loading per data output bit.

TECHNICAL NOTES

1. Applications which are unaffected by endpoint errors or remove them through software will use the typical connections shown in Figure 3. Remove system errors or adjust the small initial errors of the ADS-111 to zero using the optional external circuitry shown in Figure 4. The external adjustment circuit has no affect on the throughput rate.

2. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital

grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

3. Bypass the analog and digital supplies and the +10V reference (pin 21) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 21) to analog ground (pin 23).

4. Obtain straight binary/offset binary output coding by tying COMP BIN (pin 18) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie the COMP BIN pin to ground. The COMP BIN signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

5. To obtain three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 17) to a logic "0" (low). Otherwise, connect $\overline{\text{ENABLE}}$ (pin 17) to a logic "1" (high).

TIMING

Figure 2 shows the relationship between the various input signals. The timing shown applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design

Table 1. Input Range Selection

INPUT RANGE	INPUT PIN	TIE TOGETHER
±5V dc	Pin 19	Pin 20 to Pin 21
0 to+10V dc	Pin 19	Pin 20 to Ground

Table 2. Zero and Gain Adjust

FSR	ZERO ADJUST +1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to +10V dc	+1.22mV dc	+9.9963V dc
±5V dc	+1.22mVdc	+4.9963V dc

Table 3. Input Ranges (using external calibration)

INPUT RANGE	R1	R2	UNIT
0 to +10V, ±5V	2	2	K Ohms
0 to +5V, ±2.5V	2	6	K Ohms
0 to +2.5V, ±1.25V	2	14	K Ohms

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3, Figure 4, and Table 1 for the appropriate full-scale range (FSR). Apply a pulse of 200 nanoseconds minimum to the START CONVERT input (pin 16) at a rate of 250 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments
   Apply a precision voltage reference source between the amplifier's analog input and ground. Adjust the output of the reference source per Table 2 . For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with the COMP BIN (pin 18) tied high (straight binary) or between 1111 1111 1111 and 1111 1111 1110 with pin 18 tied low (complementary binary).

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with (pin 18) tied high (offset binary) or between 0111 1111 1111 and 0111 1111 1110 with (pin 18) tied low (complementary offset binary).

3. Full-Scale Adjustment
   Set the output of the voltage reference used in step 2 to the value shown in Table 2. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for (pin 18) tied high or between 0000 0000 0001 and 0000 0000 0000 for (pin 18) tied low.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 4 .

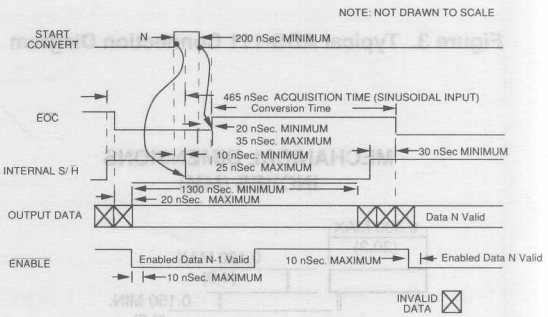


Figure 2. ADS-111 Timing Diagram

Table 4. Output Coding

INPUT RANGE 0 to +10V	UNIPOLAR SCALE	STRAIGHT BIN. COMP. BINARY OUTPUT CODING MSB LSB		BIPOLAR SCALE	INPUT RANGES
		MSB	LSB		
+9.9976V	+FS -1 LSB	1111 1111 1111	0000 0000 0000	+FS -1 LSB	+4.9976V
+8.7500V	7/8 FS	1110 0000 0000	0001 1111 1111	+3/4 FS	+3.7500V
+7.5000V	3/4 FS	1100 0000 0000	0011 1111 1111	+1/2 FS	+2.5000V
+5.0000V	1/2 FS	1000 0000 0000	0111 1111 1111	0	0.0000V
+2.5000V	1/4 FS	0100 0000 0000	1011 1111 1111	-1/2 FS	-2.5000V
+1.2500V	1/8 FS	0010 0000 0000	1101 1111 1111	+3/4 FS	-3.7500V
+0.0024V	1 LSB	0000 0000 0001	1111 1111 1110	-FS + 1 LSB	-4.9976V
0.0000V	0	0000 0000 0000	1111 1111 1111	-FS	-5.0000V
		OFF. BINARY	COMP. OFF. BIN.		

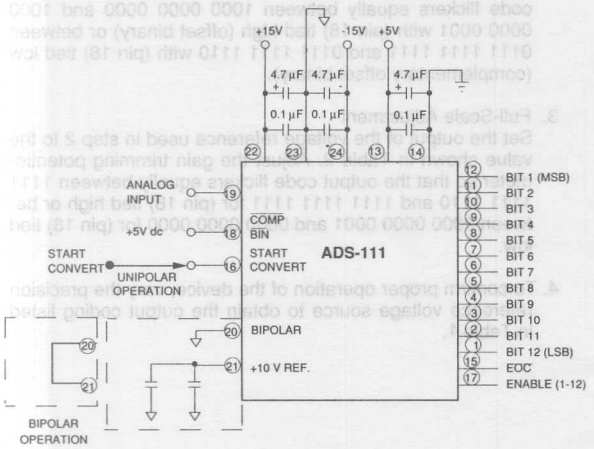
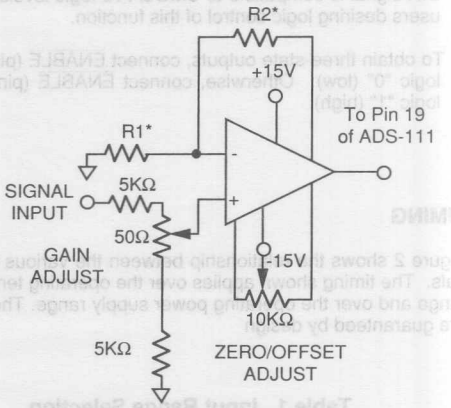


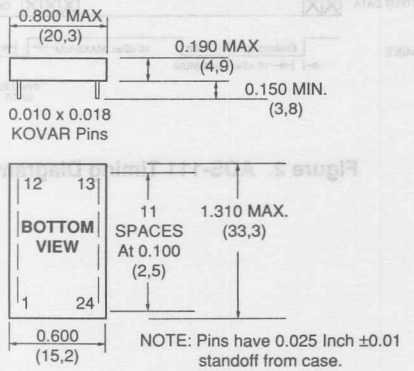
Figure 3. Typical ADS-111 Connection Diagram



*For the values of R1 and R2 see Table 3.

Figure 4. Optional Calibration Circuit

MECHANICAL DIMENSIONS INCHES (MM)



ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	SEAL
ADS-111MC	0 °C to +70 °C	Hermetic
ADS-111MM	-55 °C to +125 °C	Hermetic
ADS-111/883B	-55 °C to +125 °C	Hermetic

ACCESSORY

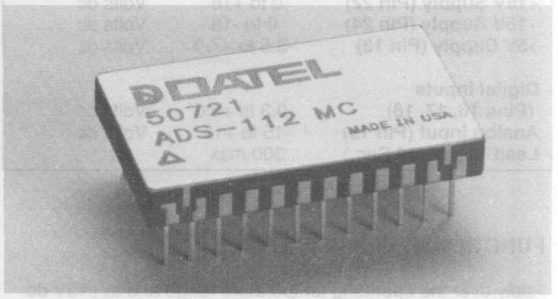
ADS-EVAL1 Evaluation Board (without ADS-111)
Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required.

ADS-112

12-Bit, 1.0 MHz Low-Power Sampling A/D Converter

FEATURES

- 12-Bit resolution
- Internal Sample/Hold
- 1.0 MHz minimum throughput
- Functionally complete
- Small 24-pin DIP
- Low-power, 1.3 Watts
- Three-state output buffers
- Samples to Nyquist
- No missing codes



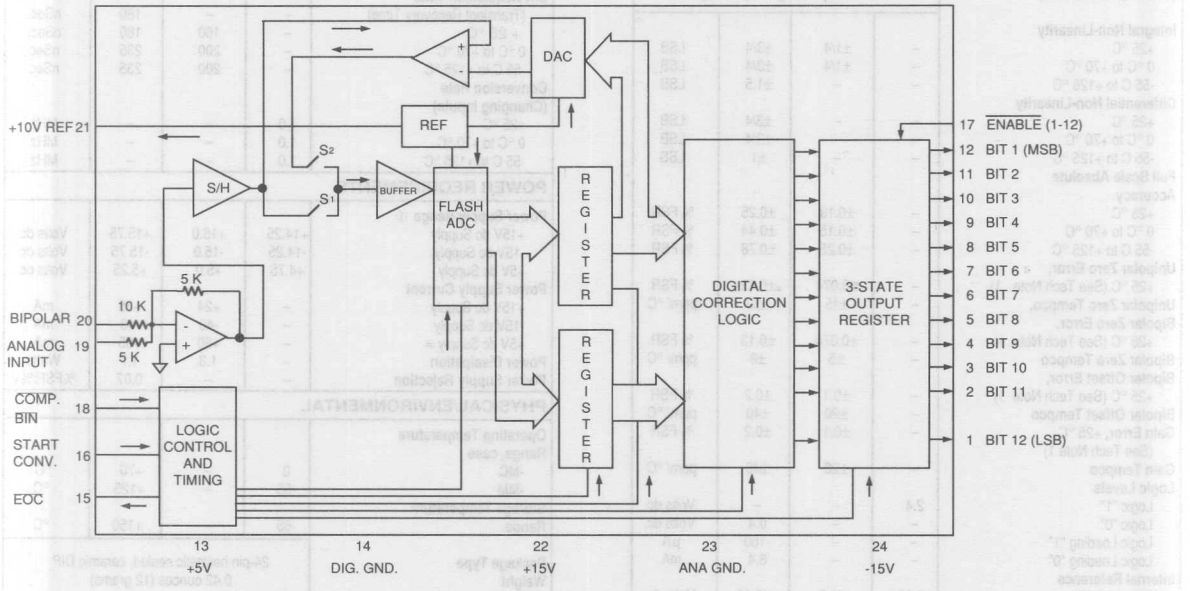
GENERAL DESCRIPTION

DATEL's ADS-112 is a 12-bit, functionally complete, sampling A/D converter that is packaged in a space-saving 24-pin ceramic DIP. A minimum throughput rate of 1.0 MHz is achieved while only dissipating 1.3 Watts. The ADS-112 digitizes signals up to Nyquist.

Typical applications include spectrum, transient, vibration and waveform analysis. This device is also ideally suited for radar, sonar, video digitization, medical instrumentation and high-speed data acquisition systems.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 OUT (LSB)	13	+5V
2	BIT 11 OUT	14	DIGITAL GROUND
3	BIT 10 OUT	15	EOC
4	BIT 9 OUT	16	START CONVERT
5	BIT 8 OUT	17	ENABLE (1-12)
6	BIT 7 OUT	18	COMP BIN
7	BIT 6 OUT	19	ANALOG INPUT
8	BIT 5 OUT	20	BIPOLAR
9	BIT 4 OUT	21	+10V REF
10	BIT 3 OUT	22	+15V
11	BIT 2 OUT	23	ANALOG GROUND
12	BIT 1 OUT (MSB)	24	-15V



ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 22)	0 to +18	Volts dc
-15V Supply (Pin 24)	0 to -18	Volts dc
+5V Supply (Pin 13)	-0.5 to +7.0	Volts dc
Digital Inputs (Pins 16, 17, 18)	-0.3 to +6.0	Volts dc
Analog Input (Pin 19)	-15 to +15	Volts dc
Lead Temp. (10 Sec.)	300 max	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and +5V dc unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range				
ADS-112	–	±5	–	Volts dc
(See Table 4 also)	–	0 to +10	–	Volts dc
Input Impedance	4.5	5.0	–	K Ohms
Input Capacitance	–	6	15	pf
DIGITAL INPUTS				
Logic Levels				
Logic "1"	2.0	–	–	Volts dc
Logic "0"	–	–	0.8	Volts dc
Logic Loading "1"	–	–	5	µA
Logic Loading "0"	–	–	-200	µA
A/D PERFORMANCE				
No Missing Codes (12 Bits; fin=500 KHz)	Over the Operating Temp. Range.			
Integral Non-Linearity				
+25 °C	–	±1/4	±3/4	LSB
0 °C to +70 °C	–	±1/4	±3/4	LSB
-55 C to +125 °C	–	–	±1.5	LSB
Differential Non-Linearity				
+25 °C	–	–	±3/4	LSB
0 °C to +70 °C	–	–	±3/4	LSB
-55 C to +125 °C	–	–	±1	LSB
Full Scale Absolute Accuracy				
+25 °C	–	±0.13	±0.25	% FSR
0 °C to +70 °C	–	±0.15	±0.44	% FSR
-55 C to +125 °C	–	±0.25	±0.78	% FSR
Unipolar Zero Error, +25 °C (See Tech Note 1)	–	±0.074	±0.13	% FSR
Unipolar Zero Tempco.	–	±15	±30	ppm/ °C
Bipolar Zero Error, +25 °C (See Tech Note 1)	–	±0.074	±0.13	% FSR
Bipolar Zero Tempco	–	±5	±8	ppm/ °C
Bipolar Offset Error, +25 °C (See Tech Note 1)	–	±0.1	±0.2	% FSR
Bipolar Offset Tempco	–	±20	±40	ppm/ °C
Gain Error, +25 °C (See Tech Note 1)	–	±0.1	±0.2	% FSR
Gain Tempco	–	±20	±40	ppm/ °C
Logic Levels				
Logic "1"	2.4	–	–	Volts dc
Logic "0"	–	–	0.4	Volts dc
Logic Loading "1"	–	–	-160	µA
Logic Loading "0"	–	–	6.4	mA
Internal Reference Voltage, +25 °C	+9.98	+10.0	+10.02	Volts dc
Drift.	–	±5	±30	ppm/ °C
External Current	–	–	1.5	mA

OUTPUTS	MIN.	TYP.	MAX.	UNITS
Resolution	12 Bits			
Output Coding				
(Pin 18 Hi)	Straight binary/offset binary			
(Pin 18 Low)	Complementary binary / Complementary offset binary			
DYNAMIC PERFORMANCE				
In-Band Harmonics (-0.5 dB)				
DC to 100 KHz	-75	-81	–	FS -dB
100 KHz to 500 KHz	-70	-75	–	FS -dB
Total Harm. Distort. (-0.5 dB)				
DC to 100 KHz	-75	-78	–	FS -dB
100 KHz to 500 KHz	-68	-73	–	FS -dB
Signal-to-Noise Ratio (w/o distort., -0.5 dB)				
DC to 100 KHz	-68	-72	–	FS -dB
100KHz to 500 KHz	-67	-71	–	FS -dB
Signal-to-Noise Ratio (& distort., -0.5 dB)				
DC to 100 KHz	-66	-70	–	FS -dB
100 KHz to 500 KHz	-66	-70	–	FS -dB
Effective Bits, -0.5 dB				
DC to 100 KHz	11.0	11.4	–	bits
100 KHz to 500 KHz	10.6	11.25	–	bits
Two-Tone Intermodulation Distort. (fin = 75 KHz, 105 KHz, Fs = 1 MHz, -7 dB	-80	-88	–	FS -dB
Two-Tone Intermodulation Distort. (fin = 480 KHz, 490 KHz, Fs = 1 MHz, -0.5 dB)	-65	-68	–	FS -dB
Input Bandwidth				
Small Signal (-20 dB input)	3.5	5	–	MHz
Full Power (0 dB input)	2.5	4	–	MHz
Slew Rate	–	150	–	V/µSec.
Aperture Delay Time	–	–	20	nSec.
Effect. Aperture Delay Time	–	–	16	nSec.
Aperture Uncertainty (Jitter)				
(RMS)	–	–	±15	pSec.
(peak)	–	–	±50	pSec.
Overvoltage Recovery Time	–	–	1000	nSec.
S/H Acquisition Time				
(Transient Recovery Time)	–	–	180	nSec.
+ 25 °C	–	160	180	nSec.
0 °C to +70 °C	–	200	235	nSec
-55 C to +125 °C	–	200	235	nSec
Conversion Rate (Changing Inputs)				
+25 °C	1.0	–	–	MHz
0 °C to +70 °C	1.0	–	–	MHz
-55 C to +125 °C	1.0	–	–	MHz
POWER REQUIREMENTS				
Power Supply Range ①				
+15V dc Supply	+14.25	+15.0	+15.75	Volts dc
-15V dc Supply	-14.25	-15.0	-15.75	Volts dc
+5V dc Supply	+4.75	+5.0	+5.25	Volts dc
Power Supply Current				
+15V dc Supply	–	+24	+35	mA
-15V dc Supply	–	-40	-48	mA
+5V dc Supply ≠	–	+80	+95	mA
Power Dissipation	–	1.3	1.7	Watts
Power Supply Rejection	–	–	0.07	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temperature Range, case				
-MC	0	–	+70	°C
-MM	-55	–	+125	°C
Storage Temperature Range	-65	–	+150	°C
Package Type	24-pin hermetic sealed, ceramic DIP			
Weight	0.42 ounces (12 grams)			

① For ±12V, +5V operation, contact DATEL
② +5V power usage at 1 TTL logic loading per data output bit.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

TECHNICAL NOTES

1. Applications which are unaffected by endpoint errors or remove them through software will use the typical connections shown in Figure 3. Remove system errors or adjust the small initial errors of the ADS-112 to zero using the optional external circuitry shown in Figure 4. The external adjustment circuit has no affect on the throughput rate.

2. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital ground are connected internally. Avoid ground-related problems by connecting the digital and analog ground to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

3. Bypass the analog and digital supplies and the +10V reference (pin 21) to ground with a 4.7µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 21) to analog ground (pin 23).

4. Obtain straight binary/offset binary output coding by tying $\overline{\text{COMP BIN}}$ (pin 18) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie pin 18 to ground. The pin 18 signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

5. To enable the three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 17) to a logic "0" (low). To disable, connect pin 17 to a logic "1" (high).

TIMING

Figure 2 shows the relationship between the various input signals. The timing shown applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

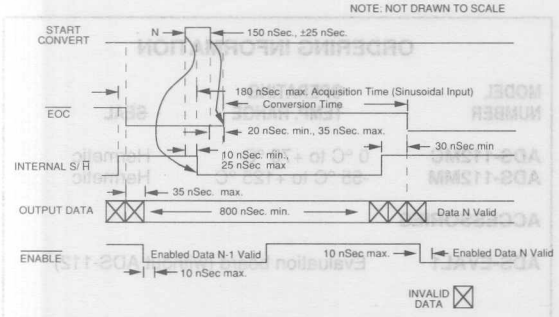


Figure 2. ADS-112 Timing Diagram

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3, Figure 4, and Table 2 for the appropriate full-scale range (FSR). Apply a pulse of 150 nanoseconds to the START CONVERT input (pin 16) at a rate of 250 KHz. This rate is chosen to reduce the flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments
   Apply a precision voltage reference source between the amplifier's analog input and ground. Adjust the output of the reference source per Table 3. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with $\overline{\text{COMP BIN}}$ (pin 18) tied high (straight binary) or between 1111 1111 1111 and 1111 1111 1110 with pin 18 tied low (complementary binary).

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with pin 18 tied high (offset binary) or between 0111 1111 1111 and 0111 1111 1110 with pin 18 tied low (complementary offset binary).

3. Full-Scale Adjustment
   Set the output of the voltage reference used in step 2 to the value shown in Table 3. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for pin 18 tied high or between 0000 0000 0001 and 0000 0000 000 for pin 18 tied low.

To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 5.

Table 2. Input Range Selection

INPUT RANGE	INPUT PIN	TIE TOGETHER
±5V dc	Pin 19	Pin 20 to Pin 21
0 to+10V dc	Pin 19	Pin 20 to Ground

Table 3. Zero and Gain Adjust

FSR	ZERO ADJUST +1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to +10V dc	+1.22mV dc	+9.9963V dc
±5V dc	+1.22mVdc	+4.9963V dc

Table 4. Input Ranges (using external calibration)

INPUT RANGE	R1	R2	UNIT
0 to +10V, ±5V	2	2	K Ohms
0 to +5V, ±2.5V	2	6	K Ohms
0 to +2.5V, ±1.25V	2	14	K Ohms

Table 6. Output Coding for Bipolar Operation

		STRAIGHT BIN. COMP. BINARY			
INPUT RANGE	UNIPOLAR	OUTPUT CODING		BIPOLAR	INPUT RANGES
0 to +10V	SCALE	MSB LSB	MSB LSB	SCALE	
+9.9976V	+FS -1 LSB	1111 1111 1111	0000 0000 0000	+FS -1 LSB	+4.9976V
+8.7500V	7/8 FS	1110 0000 0000	0001 1111 1111	+3/4 FS	+3.7500V
+7.5000V	3/4 FS	1100 0000 0000	0011 1111 1111	+1/2 FS	+2.5000V
+5.0000V	1/2 FS	1000 0000 0000	0111 1111 1111	0	0.0000V
+2.5000V	1/4 FS	0100 0000 0000	1011 1111 1111	-1/2 FS	-2.5000V
+1.2500V	1/8 FS	0010 0000 0000	1101 1111 1111	-3/4 FS	-3.7500V
+0.0024V	1 LSB	0000 0000 0001	1111 1111 1110	-FS +1 LSB	-4.9976V
0.0000V	0	0000 0000 0000	1111 1111 1111	-FS	-5.0000V
		OFF. BINARY COMP. OFF. BIN.			

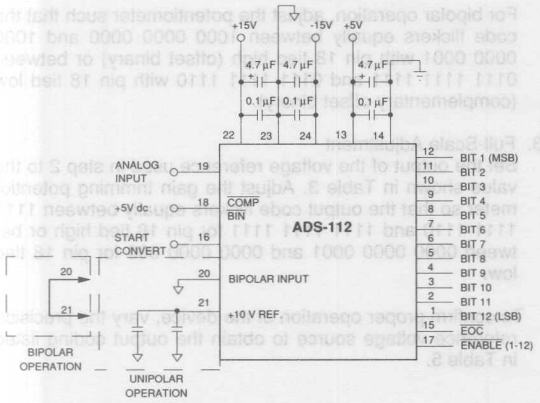


Figure 3. Typical ADS-112 Connection Diagram

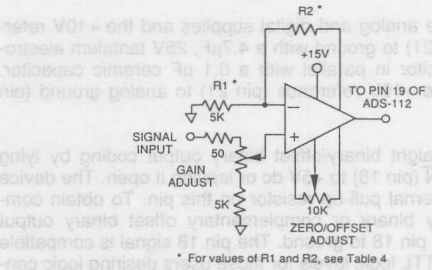


Figure 4. Optional Calibration Circuit

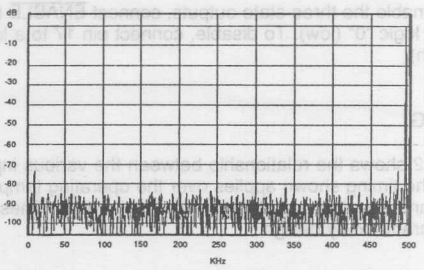
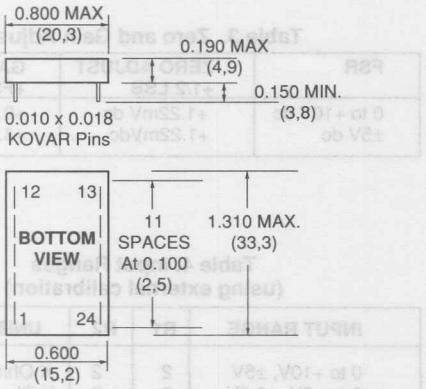


Figure 5. FFT Analysis of ADS-112

MECHANICAL DIMENSIONS
INCHES (mm)



NOTE: Pins have 0.025 Inch ±0.01 standoff from case.

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	SEAL
ADS-112MC	0 °C to +70 °C	Hermetic
ADS-112MM	-55 °C to +125 °C	Hermetic

ACCESSORIES

ADS-EVAL1 Evaluation board (without ADS-112)

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required.

For availability of MIL-STD-883B versions, contact DATEL.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

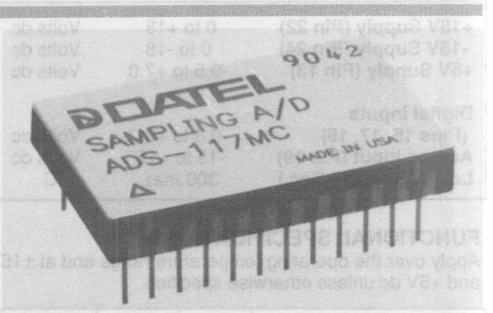
ADS-117

12-Bit, 2.0 MHz, Low-Power Sampling A/D Converter

PRELIMINARY PRODUCT DATA

FEATURES

- 12-Bit resolution
- Internal Sample/Hold
- 2.0 MHz minimum throughput
- Functionally complete
- Small 24-pin DIP
- Low-power, 1.4 Watts
- Three-state output buffers
- Samples to Nyquist

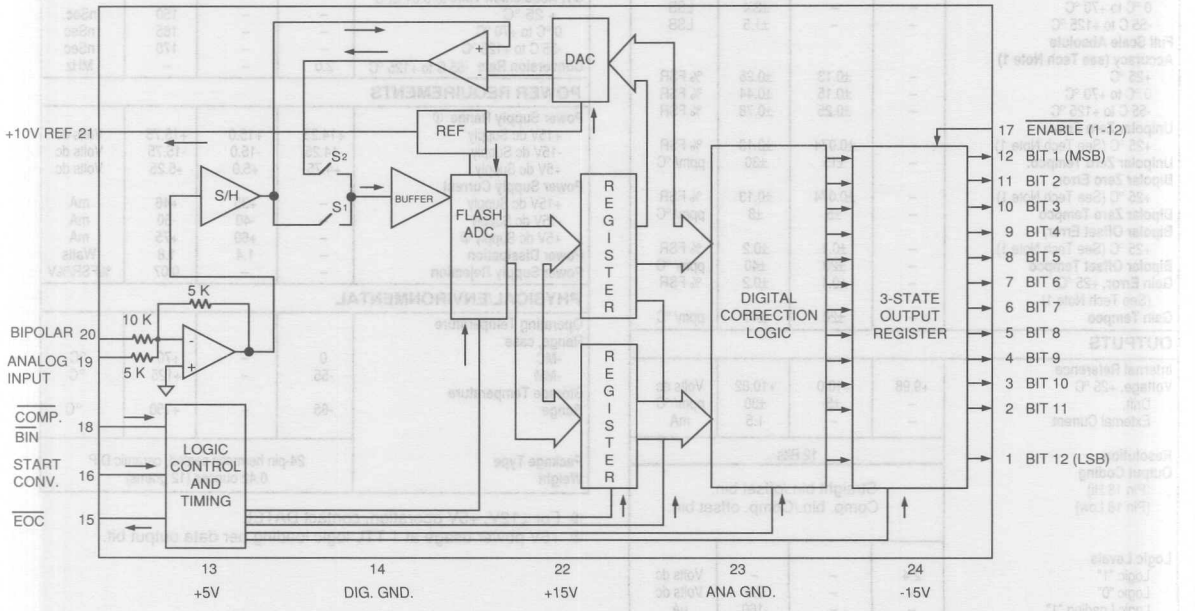


GENERAL DESCRIPTION

DATEL's ADS-117 is a 12-bit, functionally complete, sampling A/D converter that is packaged in a space-saving 24-pin ceramic DIP. A minimum throughput rate of 2.0 MHz is achieved while only dissipating 1.4 Watts. The ADS-117 digitizes signals up to Nyquist.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 OUT (LSB)	13	+5V
2	BIT 11 OUT	14	DIGITAL GROUND
3	BIT 10 OUT	15	EOC
4	BIT 9 OUT	16	START CONVERT
5	BIT 8 OUT	17	ENABLE (1-12)
6	BIT 7 OUT	18	COMP BIN
7	BIT 6 OUT	19	ANALOG INPUT
8	BIT 5 OUT	20	BIPOLAR
9	BIT 4 OUT	21	+10V REF
10	BIT 3 OUT	22	+15V
11	BIT 2 OUT	23	ANALOG GROUND
12	BIT 1 OUT (MSB)	24	-15V



ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 22)	0 to +18	Volts dc
-15V Supply (Pin 24)	0 to -18	Volts dc
+5V Supply (Pin 13)	-0.5 to +7.0	Volts dc
Digital Inputs (Pins 16, 17, 18)	-0.3 to +6.0	Volts dc
Analog Input (Pin 19)	-15 to +15	Volts dc
Lead Temp. (10 Sec.)	300 max	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and +5V dc unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range				
ADS-117	–	±5	–	Volts dc
(See Table 2 also)	–	0 to +10	–	Volts dc
Input Impedance	4.5	5.0	–	K Ohms
Input Capacitance	–	6	15	pf
DIGITAL INPUTS				
Logic Levels				
Logic "1"	2.0	–	–	Volts dc
Logic "0"	–	–	0.8	Volts dc
Logic Loading "1"	–	–	5	µA
Logic Loading "0"	–	–	-200	µA
PERFORMANCE				
No Missing Codes (12 Bits; fin=1.0 MHz)	Over the Operating Temp. Range.			
Integral non-Linearity				
+25 °C	–	±1/4	±3/4	LSB
0 °C to +70 °C	–	±1/4	±3/4	LSB
-55 C to +125 °C	–	–	±2	LSB
Differential Non-Linearity				
+25 °C	–	–	±3/4	LSB
0 °C to +70 °C	–	–	±3/4	LSB
-55 C to +125 °C	–	–	±1.5	LSB
Full Scale Absolute Accuracy (see Tech Note 1)				
+25 °C	–	±0.13	±0.25	% FSR
0 °C to +70 °C	–	±0.15	±0.44	% FSR
-55 C to +125 °C	–	±0.25	±0.78	% FSR
Unipolar Zero Error, +25 °C (See Tech Note 1)	–	±0.074	±0.13	% FSR
Unipolar Zero Tempco.	–	±15	±30	ppm/ °C
Bipolar Zero Error, +25 °C (See Tech Note 1)	–	±0.074	±0.13	% FSR
Bipolar Zero Tempco	–	±5	±8	ppm/ °C
Bipolar Offset Error, +25 °C (See Tech Note 1)	–	±0.1	±0.2	% FSR
Bipolar Offset Tempco	–	±20	±40	ppm/ °C
Gain Error, +25 °C (See Tech Note 1)	–	±0.1	±0.2	% FSR
Gain Tempco	–	±20	±40	ppm/ °C
OUTPUTS				
Internal Reference Voltage, +25 °C	+9.98	+10.0	+10.02	Volts dc
Drift.	–	±5	±30	ppm/ °C
External Current	–	–	1.5	mA
Resolution	12 Bits			
Output Coding (Pin 18 Hi)	Straight bin./offset bin.			
(Pin 18 Low)	Comp. bin./Comp. offset bin.			
Logic Levels				
Logic "1"	2.4	–	–	Volts dc
Logic "0"	–	–	0.4	Volts dc
Logic Loading "1"	–	–	-160	µA
Logic Loading "0"	–	–	6.4	mA

OUTPUT CONT.	MIN.	TYP.	MAX.	UNITS
DYNAMIC PERFORMANCE				
In-Band Harmonics (-0.5 dB)				
DC to 100 KHz	-75	-81	–	FS -dB
100 KHz to 500 KHz	-70	-75	–	FS -dB
500 KHz to 1 MHz	-67	-70	–	FS -dB
Total Harm. Distort. (-0.5 dB)				
DC to 100 KHz	-75	-78	–	FS -dB
100 KHz to 500 KHz	-68	-73	–	FS -dB
500 KHz to 100 MHz	-66	-71	–	FS -dB
Signal-to-Noise Ratio (w/o distort., -0.5 dB)				
DC to 100 KHz	-68	-72	–	FS -dB
100KHz to 500 KHz	-67	-71	–	FS -dB
500 KHz to 1 MHz	-66	-71	–	FS -dB
Signal-to-Noise Ratio & distort., -0.5 dB				
DC to 100 KHz	-66	-70	–	FS -dB
100 KHz to 500 KHz	-66	-70	–	FS -dB
500 KHz to 1 MHz	-65	-70	–	FS -dB
Effective Bits, -0.5 dB				
DC to 100 KHz	11.0	11.4	–	bits
100 KHz to 500 KHz	10.6	11.25	–	bits
500 KHz to 1 MHz	10.5	11.0	–	bits
Two-Tone Intermodulation Distort. (fin = 75 KHz, 105 KHz, Fs = 1 MHz, -7 dB	-80	-88	–	FS -dB
Two-Tone Intermodulation Distort. (fin = 970 KHz, 990 KHz, Fs = 2 MHz, -0.5 dB)	-65	-68	–	FS -dB
Input Bandwidth				
Small Signal (-20 dB input)	8	10	–	MHz
Full Power (0 dB input)	5	7	–	MHz
Feedthrough (1 MHz)	-72	-74	–	dB
Slew Rate	–	210	–	V/µSec.
Aperture Delay Time	–	–	20	nSec.
Effect. Aperture Delay Time	–	–	16	nSec.
Aperture Uncertainty (Jitter)				
(RMS)	–	±5	±15	pSec.
(peak)	–	–	±40	pSec.
Overvoltage Recovery Time	–	–	1000	nSec.
S/H Acquisition Time to 0.01%FS				
+ 25 °C	–	–	150	nSec.
0 °C to +70 °C	–	–	165	nSec
-55 C to +125 °C	–	–	170	nSec
Conversion Rate -55 C to +125 °C	2.0	–	–	MHz
POWER REQUIREMENTS				
Power Supply Range ①				
+15V dc Supply	+14.25	+15.0	+15.75	Volts dc
-15V dc Supply	-14.25	-15.0	-15.75	Volts dc
+5V dc Supply	+4.75	+5.0	+5.25	Volts dc
Power Supply Current				
+15V dc Supply	–	+35	+46	mA
-15V dc Supply	–	-40	-50	mA
+5V dc Supply ②	–	+60	+75	mA
Power Dissipation	–	1.4	1.8	Watts
Power Supply Rejection	–	–	0.07	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temperature Range, case				
-MC	0	–	+70	°C
-MM	-55	–	+125	°C
Storage Temperature Range	-65	–	+150	°C
Package Type	24-pin hermetic sealed, ceramic DIP			
Weight	0.42 ounces (12 grams)			

① For ±12V, +5V operation, contact DATEL

② +5V power usage at 1 TTL logic loading per data output bit.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

move them through software will use the typical connections shown in Figure 3. Remove system errors or adjust the small initial errors of the ADS-117 to zero using the optional external circuitry shown in Figure 4. The external adjustment circuit has no affect on the throughput rate.

2. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital grounds are connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

3. Bypass the analog and digital supplies and the +10V reference (pin 21) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 21) to analog ground (pin 23).

4. Obtain straight binary/offset binary output coding by tying COMP BIN (pin 18) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie pin 18 to ground. The pin 18 signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

5. To enable the three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 17) to a logic "0" (low). To disable, connect pin 17 to a logic "1" (high).

6. To meet the guaranteed conversion rate, a maximum start convert pulse is specified. A wider start convert pulse will result in slower conversion rates.

   Figure 2 shows the relationship between the various input signals. The timing shown applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3, Figure 4, and Table 2 for the appropriate full-scale range (FSR). Apply a pulse of 150 nanoseconds to the START CONVERT input (pin 16) at

2. Zero Adjustments
   Apply a precision voltage reference source between the amplifier's analog input and ground. Adjust the output of the reference source per Table 1. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with the pin 18 tied high (straight binary) or between 1111 1111 1111 and 1111 1111 1110 with the pin 18 tied low (complementary binary).

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with pin 18 tied high (offset binary) or between 0111 1111 1111 and 0111 1111 1110 with pin 18 tied low (complementary offset binary).

3. Full-Scale Adjustment
   Set the output of the voltage reference used in step 2 to the value shown in Table 1. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for pin 18 tied high or between 0000 0000 0001 and 0000 0000 0000 for pin 18 tied low.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 3.

Table 1. Zero and Gain Adjust

FSR	ZERO ADJUST + 1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to +10V dc	+1.22mV dc	+9.9963V dc
±5V dc	+1.22mV dc	+4.9963V dc

Table 2. Input Ranges (using external calibration)

INPUT RANGE	R1	R2	UNIT
0 to +10V, ±5V	2	2	K Ohms
0 to +5V, ±2.5V	2	6	K Ohms
0 to +2.5V, ±1.25V	2	14	K Ohms

Table 3. Output Coding

		STRAIGHT BIN.	COMP. BINARY		
UNIPOLAR	INPUT RANGES, V dc	OUTPUT CODING		INPUT RANGE	BIPOLAR
SCALE	0 to +10V	MSB LSB	MSB LSB	±5V dc	SCALE
+FS -1 LSB	+9.9976V	1111 1111 1111	0000 0000 0000	+4.9976V	+FS -1 LSB
7/8 FS	+8.7500V	1110 0000 0000	0001 1111 1111	+3.7500V	+3/4 FS
3/4 FS	+7.5000V	1100 0000 0000	0011 1111 1111	+2.5000V	+1/2 FS
1/2 FS	+5.0000V	1000 0000 0000	0111 1111 1111	0.0000V	0
1/4 FS	2.5000V	0100 0000 0000	1011 1111 1111	-2.5000V	-1/2 FS
1/8 FS	1.2500V	0010 0000 0000	1101 1111 1111	-3.7500V	-3/4 FS
1 LSB	0.0024V	0000 0000 0001	1111 1111 1110	-4.9976V	-FS +1 LSB
0	0.0000V	0000 0000 0000	1111 1111 1111	-5.0000V	-FS
		OFF. BINARY	COMP. OFF. BIN.		

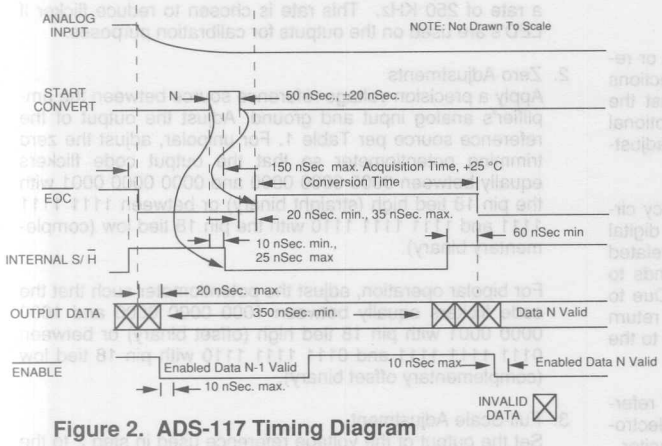


Figure 2. ADS-117 Timing Diagram

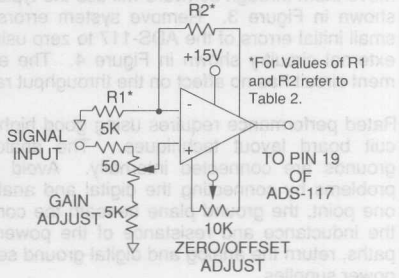


Figure 4. Optional Calibration Circuit

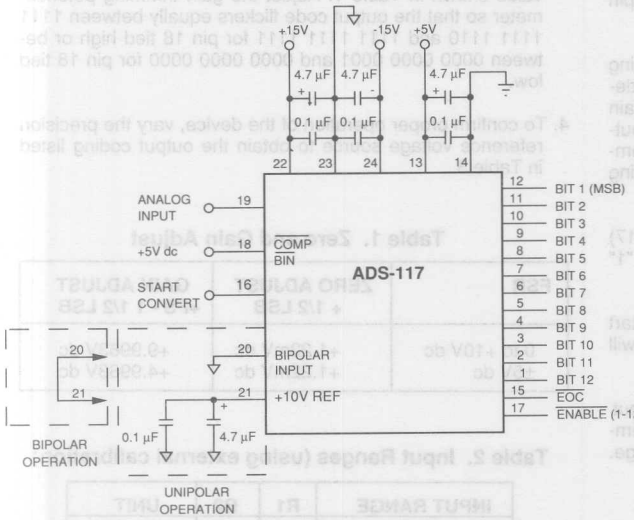


Figure 3. Typical ADS-117 Connection Diagram

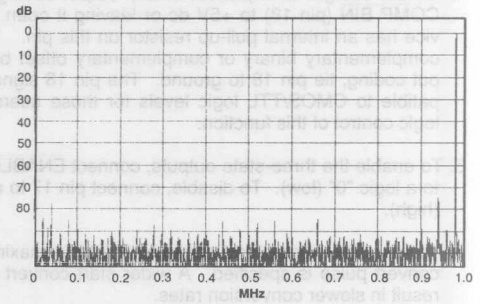
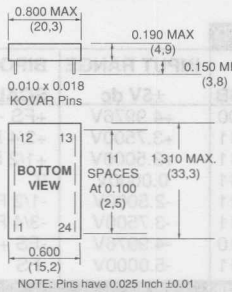


Figure 5. FFT Analysis of ADS-117

MECHANICAL DIMENSIONS INCHES (MM)



ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	SEAL
ADS-117MC	0 °C to +70 °C	Hermetic
ADS-117MM	-55 °C to +125 °C	Hermetic
ADS-EVAL1	Evaluation board (without ADS-117)	

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required.

For availability of MIL-STD-883 versions of the ADS-117, contact DATEL.

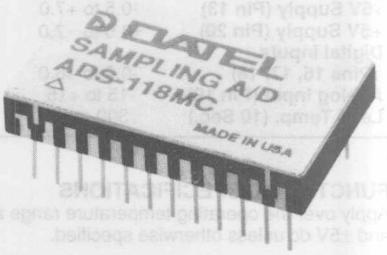
ADS-118

12-Bit, 5.0 MHz, Low-Power Sampling A/D Converter

PRELIMINARY PRODUCT DATA

FEATURES

- **12-Bit resolution**
- **Internal Sample/Hold**
- **5.0 MHz minimum throughput**
- **Functionally complete**
- **Small 24-pin DIP**
- **Low-power, 2.3 Watts**
- **Three-state output buffers**
- **Samples to Nyquist**

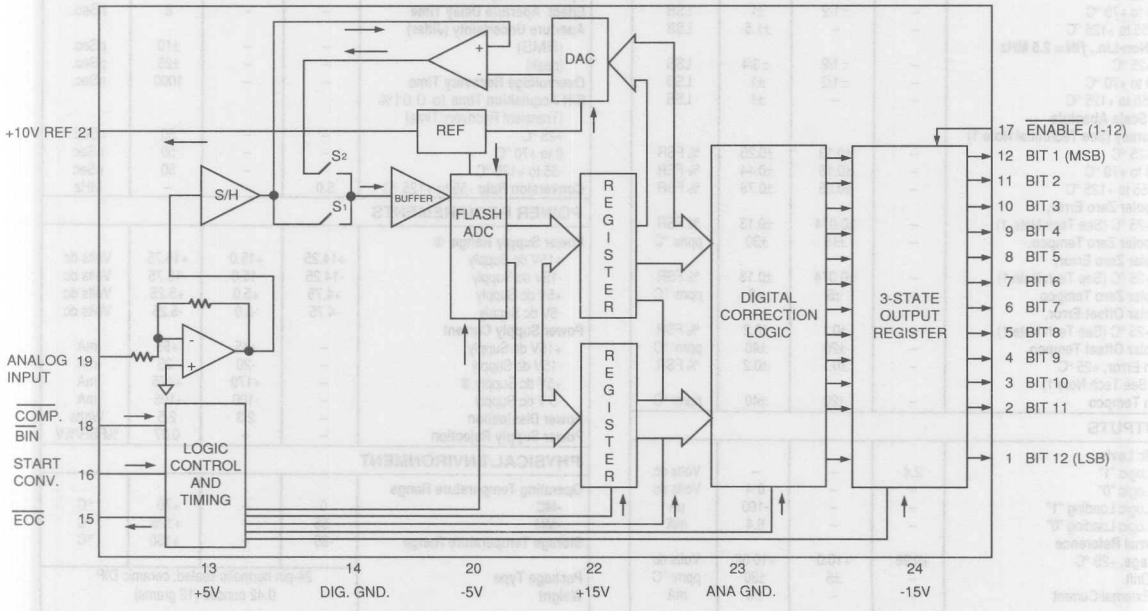


GENERAL DESCRIPTION

DATEL's ADS-118 is a 12-bit, functionally complete, sampling A/D converter that is packaged in a space-saving 24-pin ceramic DIP. A minimum throughput rate of 5.0 MHz is achieved while only dissipating 2.3 Watts. The ADS-118 digitizes signals up to Nyquist.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 OUT (LSB)	13	+5V
2	BIT 11 OUT	14	DIGITAL GROUND
3	BIT 10 OUT	15	EOC
4	BIT 9 OUT	16	START CONVERT
5	BIT 8 OUT	17	ENABLE (1-12)
6	BIT 7 OUT	18	COMP BIN
7	BIT 6 OUT	19	ANALOG INPUT
8	BIT 5 OUT	20	-5V
9	BIT 4 OUT	21	+10V REF
10	BIT 3 OUT	22	+15V
11	BIT 2 OUT	23	ANALOG GROUND
12	BIT 1 OUT (MSB)	24	-15V



ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 22)	0 to +18	Volts dc
-15V Supply (Pin 24)	0 to -18	Volts dc
+5V Supply (Pin 13)	-0.5 to +7.0	Volts dc
+5V Supply (Pin 20)	+0.5 to -7.0	Volts dc
Digital Inputs (Pins 16, 17, 18)	-0.3 to +6.0	Volts dc
Analog Input (Pin 19)	-15 to +15	Volts dc
Lead Temp. (10 Sec.)	300 max	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and ±5V dc unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range				
ADS-118	–	±1	–	Volts dc
(See Table 4 also)	–	–	–	Volts dc
Input Impedance	5.0	10.0	–	M Ohms
Input Capacitance	–	6	15	pf
DIGITAL INPUTS				
Logic Levels				
Logic "1"	2.0	–	–	Volts dc
Logic "0"	–	–	0.8	Volts dc
Logic Loading "1"	–	–	5	µA
Logic Loading "0"	–	–	-200	µA
PERFORMANCE				
No Missing Codes (12 Bits; *f*IN = 2.5 MHz)	Over the Operating Temp. Range.			
Integral Non-Lin., *f*IN = 2.5 MHz				
+25 °C	–	±1/4	±1	LSB
0 to +70 °C	–	±1/2	±1	LSB
-55 to +125 °C	–	–	±1.5	LSB
Diff.Non-Lin., *f*IN = 2.5 MHz				
+25 °C	–	±1/2	±3/4	LSB
0 to +70 °C	–	±1/2	±1	LSB
-55 to +125 °C	–	–	±1	LSB
Full Scale Absolute Accuracy (See Technical Note 1)				
+25 °C	–	±0.13	±0.25	% FSR
0 to +70 °C	–	±0.15	±0.44	% FSR
-55 to +125 °C	–	±0.25	±0.78	% FSR
Unipolar Zero Error, +25 °C (See Tech Note 1)	–	±0.074	±0.13	% FSR
Unipolar Zero Tempco.	–	±15	±30	ppm/ °C
Bipolar Zero Error, +25 °C (See Tech Note 1)	–	±0.074	±0.13	% FSR
Bipolar Zero Tempco	–	±5	±8	ppm/ °C
Bipolar Offset Error, +25 °C (See Tech Note 1)	–	±0.1	±0.2	% FSR
Bipolar Offset Tempco	–	±20	±40	ppm/ °C
Gain Error, +25 °C (See Tech Note 1)	–	±0.1	±0.2	% FSR
Gain Tempco	–	±20	±40	ppm/ °C
OUTPUTS				
Logic Levls				
Logic "1"	2.4	–	–	Volts dc
Logic "0"	–	–	0.4	Volts dc
Logic Loading "1"	–	–	-160	µA
Logic Loading "0"	–	–	6.4	mA
Internal Reference Voltage, +25 °C	+9.98	+10.0	+10.02	Volts dc
Drift.	–	±5	±30	ppm/ °C
External Current	–	–	1.5	mA

OUTPUT CONT.	MIN.	TYP.	MAX.	UNITS
Resolution	12 Bits			
Output Coding (Pin 18 Hi)	Straight binary/offset binary			
(Pin 18 Low)	Complementary binary / Complementary offset binary			
DYNAMIC PERFORMANCE				
In-Band (-0.5 dB)				
DC to 500 KHz	-70	-75	–	FS -dB
500 KHz to 1.0 MHz	-65	-70	–	FS -dB
1.0 MHz to2.5 MHz	-63	-65	–	FS -dB
Total Harm. Distort. (-0.5 dB)				
DC to 500 KHz	-70	-73	–	FS -dB
500 KHz to 1.0 MHz	-63	-68	–	FS -dB
1.0 MHz to 2.5 MHz	-60	-63	–	FS -dB
Signal-to-Noise Ratio (w/o distort., -0.5 dB)				
DC to 500 KHz	-63	-68	–	FS -dB
500KHz to 1.0 MHz	-62	-66	–	FS -dB
1.0 MHz to 2.5 MHz	-60	-62	–	FS -dB
Signal-to-Noise Ratio with distortion, -0.5 dB				
DC to 500 KHz	-65	-66	–	FS -dB
500 KHz to 1.0 MHz	-64	-65	–	FS -dB
1.0 MHz to 2.5 MHz	-63	-65	–	FS -dB
Effective Bits, -0.5 dB				
DC to 500 KHz	10.6	10.8	–	bits
500 KHz to 1.0 MHz	10.3	10.5	–	bits
1.0 MHz to 2.5 MHz	10.3	10.4	–	bits
Two-Tone Intermodulation Distort. (*f*IN = 75 KHz, 105 KHz, Fs = 5 MHz, -7 dB	-74	-81	–	FS -dB
Two-Tone Intermodulation Distort. (*f*IN = 2.3 KHz, 2.5 MHz, Fs = 5 MHz, -0.5 dB)	-60	-63	–	FS -dB
Input Bandwidth				
Small Signal (-20 dB input)	50	65	–	MHz
Full Power (0 dB input)	30	40	–	MHz
Slew Rate	–	250	–	V/ÜSec..
Aperture Delay Time	–	–	10	nSec.
Effect. Aperture Delay Time	–	–	8	nSec.
Aperture Uncertainty (Jitter)				
(RMS)	–	–	±10	pSec.
(peak)	–	–	±25	pSec.
Overvoltage Recovery Time	–	–	1000	nSec.
S/H Acquisition Time to 0.01% (Transient Recovery Time)				
+25 °C	–	–	50	nSec.
0 to +70 °C	–	–	50	nSec
-55 to +125 °C	–	–	50	nSec
Conversion Rate -55 to +125 °C	5.0	–	–	MHz
POWER REQUIREMENTS				
Power Supply Range ①				
+15V dc Supply	+14.25	+15.0	+15.75	Volts dc
-15V dc Supply	-14.25	-15.0	-15.75	Volts dc
+5V dc Supply	+4.75	+5.0	+5.25	Volts dc
-5V dc Supply	-4.75	-5.0	-5.25	Volts dc
Power Supply Current				
+15V dc Supply	–	+45	+55	mA
-15V dc Supply	–	-20	-25	mA
+5V dc Supply ②	–	+170	+175	mA
-5 V dc Supply	–	-100	-105	mA
Power Dissipation	–	2.3	2.5	Watts
Power Supply Rejection	–	–	0.07	%FSR/%V
PHYSICAL/ENVIRONMENT				
Operating Temperature Range				
-MC	0	–	+70	°C
-MM	-55	–	+125	°C
Storage Temperature Range	-65	–	+150	°C
Package Type	24-pin hermetic sealed, ceramic DIP			
Weight	0.42 ounces (12 grams)			

① For ±12V, +5V operation, contact DATEL

② +5V power usage at 1 TTL logic loading per data output bit.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

TECHNICAL NOTES

1. Applications which are unaffected by endpoint errors or remove them through software will use the typical connections shown in Figure 3. Remove system errors or adjust the small initial errors of the ADS-118 to zero using the optional external circuitry shown in Figures 4a and 4b. The external adjustment circuit has no affect on the throughput rate.

2. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital grounds are connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

3. Bypass the analog and digital supplies and the +10V reference (pin 21) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 21) to analog ground (pin 23).

4. Obtain straight binary/offset binary output coding by tying COMP BIN (pin 18) to +5V dc open. To obtain complementary binary or complementary offset binary output coding, tie pin 18 to ground. The pin 18 signal is compatible with CMOS/TTL logic levels for those users desiring logic control of this function.

5. To enable the three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 17) to a logic "0" (low). To disable, connect pin 17 to a logic "1" (high).

6. Figure 2 shows the relationship between the various input signals. The timing shown applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3 and Figure 4 for the appropriate full-scale range (FSR). Apply a pulse of 45 nanoseconds to the START CONVERT input (pin 16) at a rate of 250 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments
   Apply a precision voltage reference source between the amplifier's analog input and ground. Adjust the output of the reference source per Table 1 for bipolar zero adjustment (zero +1/2 LSB).

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with COMP BIN (pin 18) tied high (offset binary) or between 0111 1111 1111 and 0111 1111 1110 with COMP BIN (pin 18) tied low (complementary offset binary).

3. Full-Scale Adjustment
   Set the output of the voltage reference used in step 2 to the value shown in Table 1 for the bipolar gain adjustment (+FS -1 1/2 LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for COMP BIN (pin 18) tied high or between 0000 0000 0001 and 0000 0000 0000 for COMP BIN (pin 18) tied low.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 2.

Table 1. Zero and Gain Adjust, Bipolar Operation

BIPOLAR FSR	ZERO ADJUST 0 + 1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
±1V dc	±244µV dc	+0.99926V dc

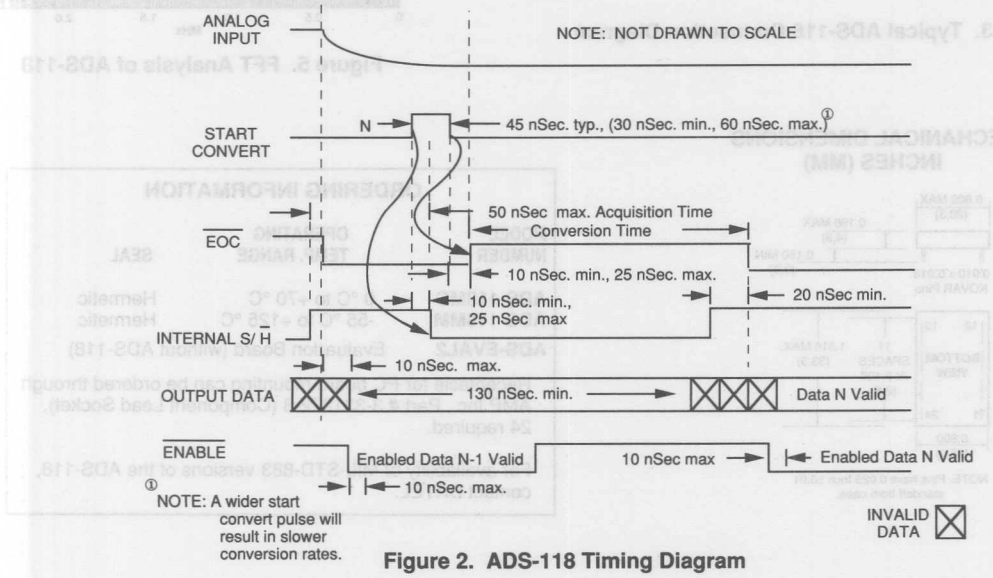


Figure 2. ADS-118 Timing Diagram

Table 2. Output Coding for Bipolar Operation

BIPOLAR SCALE	INPUT RANGE (Volts dc) ±1V	OUTPUT CODING OFFSET BINARY MSB	LSB	COMP. OFFSET BINARY MSB	LSB
+FS -1 LSB	+0.99952V	1111	1111 1111	0000	0000 0000
+3/4 FS	+0.7500V	1110	0000 0000	0001	1111 1111
+1/2 FS	+0.5000V	1100	0000 0000	0011	1111 1111
0	0.0000V	1000	0000 0000	0111	1111 1111
-1/2 FS	-0.5000V	0100	0000 0000	1011	1111 1111
-3/4 FS	-0.7500V	0010	0000 0000	1101	1111 1111
-FS +1 LSB	-0.99952V	0000	0000 0001	1111	1111 1110
-FS	-1.0000V	0000	0000 0000	1111	1111 1111

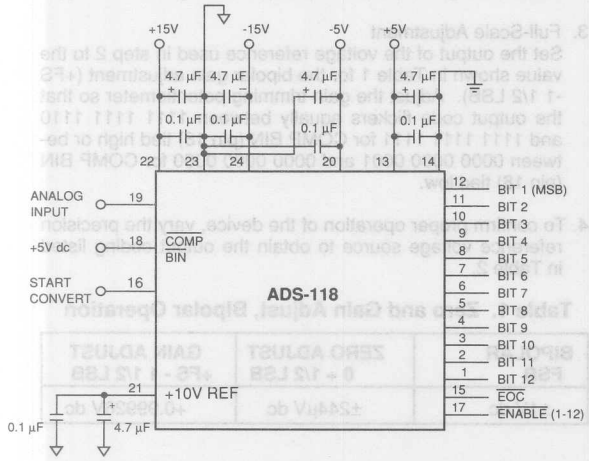


Figure 3. Typical ADS-118 Connection Diagram

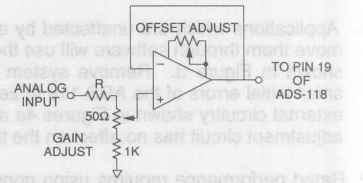


Figure 4a. Optional Bipolar Calibration Circuit

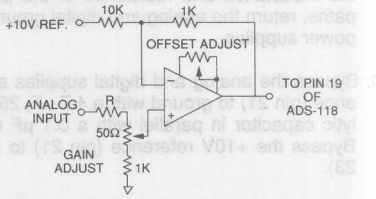


Figure 4b. Optional Unipolar Calibration Circuit

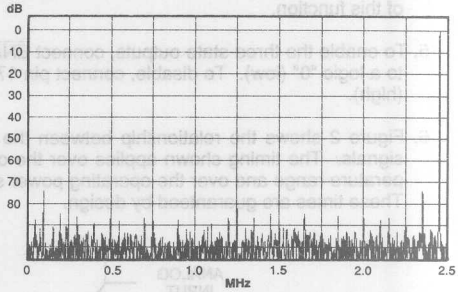
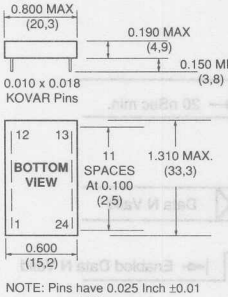


Figure 5. FFT Analysis of ADS-118

MECHANICAL DIMENSIONS INCHES (MM)



NOTE: Pins have 0.025 Inch ±0.01 standoff from case.

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	SEAL
ADS-118MC	0 °C to +70 °C	Hermetic
ADS-118MM	-55 °C to +125 °C	Hermetic
ADS-EVAL2	Evaluation Board (without ADS-118)	

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required.

For availability of MIL-STD-883 versions of the ADS-118, contact DATEL.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

FEATURES

- **12-Bit resolution**
- **Internal Sample/Hold amplifier**
- **20 MHz minimum throughput**
- **Samples up to Nyquist**
- **Functionally Complete**
- **Small 40-pin DIP**
- **Low-power, 4.2 Watts**
- **Three-State output buffers**
- **High input bandwidth**
- **Overflow pin**

GENERAL DESCRIPTION

DATEL's ADS-120 is a 12-bit, functionally complete, sampling A/D converter packaged in a small 40-pin DIP. A 20 MHz minimum throughput rate in digitizing sinusoidal signals is achieved while only dissipating 4.2 Watts.

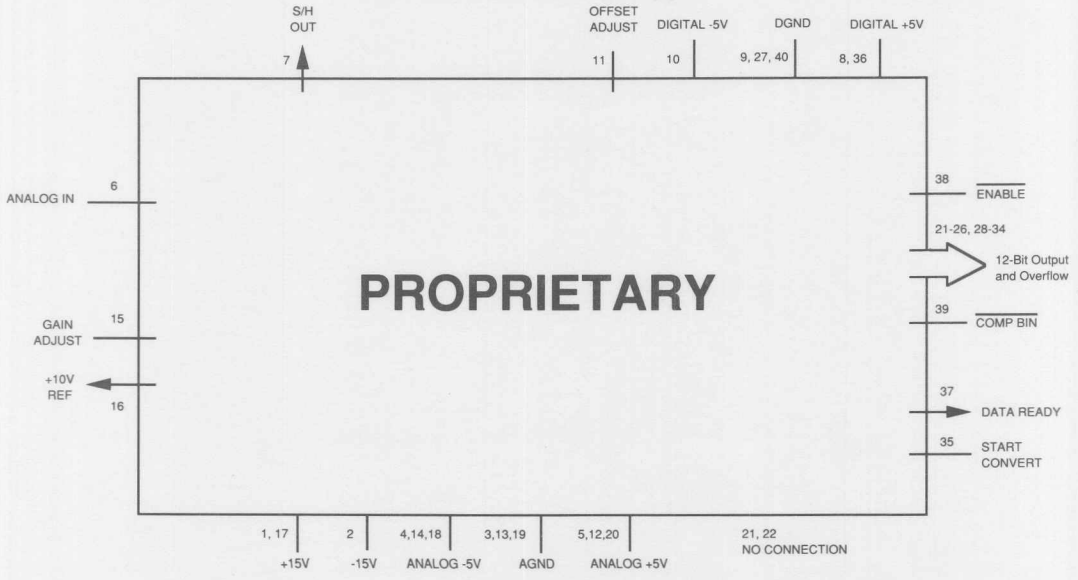
The ADS-120 is offered in the commercial 0 to +70 °C and military -55 to +125 °C operating temperature range.

APPLICATIONS

- **Spectrum analysis**
- **Imaging**
- **Radar**
- **Medical Instrumentation**
- **High-speed Data Acquisition Systems**

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+15V	40	DIGITAL GROUND
2	-15V	39	COMP BIN
3	ANALOG GROUND	38	ENABLE
4	ANALOG -5V	37	DATA READY
5	ANALOG +5V	36	DIGITAL +5V
6	ANALOG INPUT	35	START CONVERT
7	S/H OUT	34	OVERFLOW
8	DIGITAL +5V	33	BIT 1 (MSB)
9	DIGITAL GROUND	32	BIT 2 OUT
10	DIGITAL -5V	31	BIT 3 OUT
11	OFFSET ADJUST	30	BIT 4 OUT
12	ANALOG +5V	29	BIT 5 OUT
13	ANALOG GROUND	28	BIT 6 OUT
14	ANALOG -5V	27	DIGITAL GROUND
15	GAIN ADJUST	26	BIT 7 OUT
16	+10V REFERENCE	25	BIT 8 OUT
17	+15V SUPPLY	24	BIT 9 OUT
18	ANALOG -5V	23	BIT 10 OUT
19	ANALOG GROUND	22	BIT 11 OUT
20	ANALOG +5V	21	BIT 12 OUT (LSB)



Contact DATEL for up-to-date information on products covered by "Advanced" and "Preliminary" product data sheets.

Dial
1-800-233-2765
for
Applications Assistance

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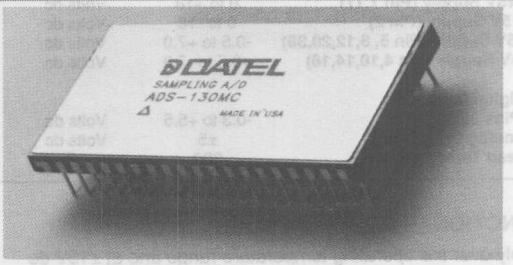
ADS-130
12-Bit, 10 MHz Sampling A/D Converter

FEATURES

- 12-Bit resolution
- Internal Sample/Hold amplifier
- 10 MHz minimum throughput
- Samples up to Nyquist
- Functionally Complete
- Small 40-pin DIP
- Low-power, 3.85 Watts
- Three-State output buffers
- High input bandwidth
- Overflow pin
- No missing codes



GENERAL DESCRIPTION

DATEL's ADS-130 is a 12-bit, functionally complete, sampling A/D converter packaged in a small 40-pin DIP. A 10 MHz minimum throughput rate in digitizing sinusoidal signals is achieved while only dissipating 3.85 Watts.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+15V	40	DIGITAL GROUND
2	-15V	39	COMP BIN
3	ANALOG GROUND	38	ENABLE
4	ANALOG -5V	37	DATA READY
5	ANALOG +5V	36	DIGITAL +5V
6	ANALOG INPUT	35	START CONVERT
7	S/H OUT	34	OVERFLOW
8	DIGITAL +5V	33	BIT 1 (MSB)
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14	ANALOG -5V	27	DIGITAL GROUND
15	GAIN ADJUST	26	BIT 7 OUT
16	+10V REFERENCE	25	BIT 8 OUT
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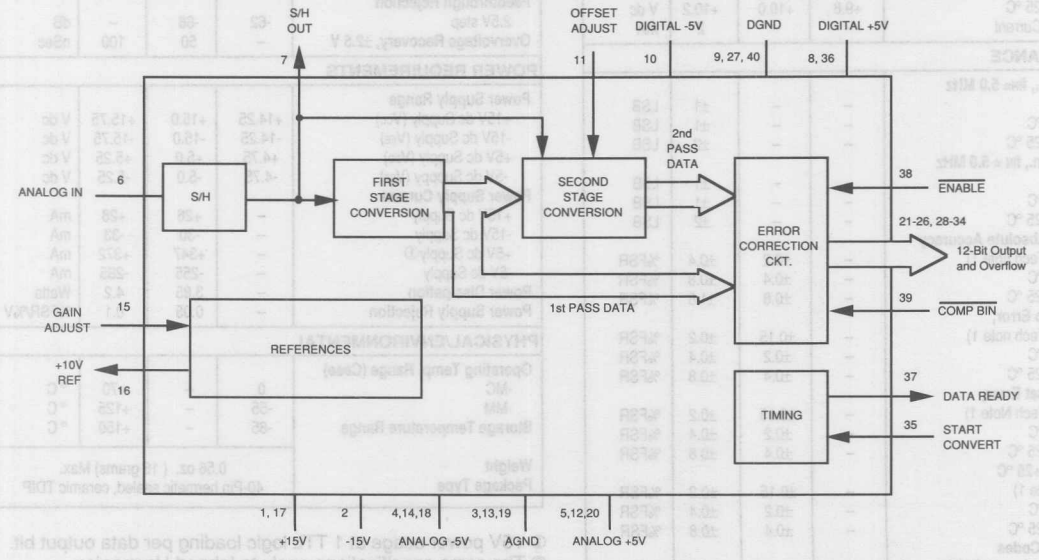
18	ANALOG -5V	23	BIT 10 OUT
19	ANALOG GROUND	22	BIT 11 OUT
20	ANALOG +5V	21	BIT 12 OUT (LSB)



ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 1,17)	0 to +18	Volts dc
-15V Supply (Pin 2)	0 to -18	Volts dc
+5V Supply (Pin 5, 8,12,20,36)	-0.5 to +7.0	Volts dc
-5V Supply (Pin 4,10,14,18)	+0.5 to -7.0	Volts dc
Digital Inputs (Pins 35,38,39)	-0.3 to +5.5	Volts dc
Analog Input (Pin 6)	±5	Volts dc
Lead Temp. (10 Sec.)	300	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and ±5V dc unless otherwise specified.

INPUTS	MIN	TYP	MAX	UNITS
ANALOG				
Input Voltage Range	–	±1.25	–	V dc
Input Impedance	50	160	–	KOhm
Input Capacitance	–	2.5	10	pF
DIGITAL				
Logic Level "1"	2.0	–	–	V dc
Logic Level "0"	–	–	0.8	V dc
Logic Loading "1"	–	–	5.0	µA
Logic Loading "0"	–	–	-200	µA
OUTPUTS				
Resolution	12 Bits			
Output Coding (Pin 39 HI)	Offset Binary			
(Pin 39 Low)	Complementary Offset Binary			
Logic Level "1"	2.4	–	–	V dc
Logic Level "0"	–	–	0.4	V dc
Logic Loading "1"	–	–	-160	µA
Logic Loading "0"	–	–	6.4	mA
Internal V_{REF}, (pin 16)				
+25 °C	+9.9	+10.0	+10.1	V dc
0 to +70 °C	+9.9	+10.0	+10.1	V dc
-55 to +125 °C	+9.8	+10.0	+10.2	V dc
External Current	–	–	2	mA
PERFORMANCE				
Int. Non-Lin., f_{IN}= 5.0 MHz				
+25 °C	–	–	±1	LSB
0 to +70 °C	–	–	±1	LSB
-55 to +125 °C	–	–	±2	LSB
Diff. Non-Lin., f_{IN} = 5.0 MHz				
+25 °C	–	–	±1	LSB
0 to +70 °C	–	–	±1	LSB
-55 to +125 °C	–	–	±2	LSB
Full Scale Absolute Accuracy				
+25 °C (Tech note 1)	–	±0.2	±0.4	%FSR
0 to +70 °C	–	±0.4	±0.8	%FSR
-55 to +125 °C	–	±0.8	±1.6	%FSR
Bipolar Zero Error,				
+25 °C (Tech note 1)	–	±0.15	±0.2	%FSR
0 to +70 °C	–	±0.2	±0.4	%FSR
-55 to +125 °C	–	±0.4	±0.8	%FSR
Bipolar Offset Error,				
+25 °C (Tech Note 1)	–	±0.15	±0.2	%FSR
0 to +70 °C	–	±0.2	±0.4	%FSR
-55 to +125 °C	–	±0.4	±0.8	%FSR
Gain Error, +25 °C				
(Tech Note 1)	–	±0.15	±0.2	%FSR
0 to +70 °C	–	±0.2	±0.4	%FSR
-55 to +125 °C	–	±0.4	±0.8	%FSR
No Missing Codes				
(12 Bits, at f_{IN} = 2.5 MHz)				

DYNAMIC PERFORMANCE	MIN	TYP	MAX	UNITS
Conversion Rate				
(Changing Inputs),+25 °C	10	–	–	MHz
0 to +70 °C	10	–	–	MHz
-55 to +125 °C	10	–	–	MHz
Total Harm. Distort.(-0.5 dB)				
DC to 500 KHz	-68	-70	–	FS, -dB
500 KHz to 2.5 MHz	-65	-67	–	FS, -dB
2.5 MHz to 5 Mhz	-65	-67	–	FS, -dB
Signal-to-Noise Ratio				
(w/o distortion, -0.5 dB)				
DC to 500 KHz	-67	-70	–	FS, -dB
500 KHz to 2.5 MHz	-65	-69	–	FS, -dB
2.5 MHz to 5 Mhz	-65	-69	–	FS, -dB
Signal-to-Noise Ratio				
and Distortion (-0.5 dB)				
DC to 500 KHz	-65	-66	–	FS, -dB
500 KHz to 2.5 MHz	-63	-65	–	FS, -dB
2.5 MHz to 5 Mhz	-63	-65	–	FS, -dB
Spurious Free Dynamic Range				
DC to 500 KHz (-0.5 dB)②	-69	-70	–	FS, -dB
500 KHz to 2.5 MHz	-66	-67	–	FS, -dB
2.5 MHz to 5 Mhz	-66	-67	–	FS, -dB
Effective Bits				
DC to 500 KHz	10.6	11.0	–	Bits
500 KHz to 2.5 MHz	10.2	10.5	–	Bits
2.5 MHz to 5 Mhz	10.0	10.2	–	Bits
Two-tone Intermodulation Distortion (f_{IN} =2.2 MHz,				
2.3 MHz, Fs = 8 MHz)	-72	-75	–	dB
Input Bandwidth				
Small Signal (-20 dB input)	50	65	–	MHz
Full Power (0 dB input)	30	40	–	MHz
Slew Rate	175	200	–	V/µSec
Aperture Delay Time	–	5	7	nSec
Aperture Uncertainty	–	5	7	psec
S/H Acquisition Time				
to 0.01% FS (2.5V step)				
+25 °C	–	30	50	nSec
0 to +70 °C	–	30	50	nSec
-55 to +125 °C	–	50	70	nSec
Feedthrough Rejection				
2.5V step	-62	-66	–	dB
Overvoltage Recovery, ±2.5 V	–	50	100	nSec
POWER REQUIREMENTS				
Power Supply Range				
+15V dc Supply (V_{CC})	+14.25	+15.0	+15.75	V dc
-15V dc Supply (V_{EE})	-14.25	-15.0	-15.75	V dc
+5V dc Supply (V_{DD})	+4.75	+5.0	+5.25	V dc
-5V dc Supppy (V_{SS})	-4.75	-5.0	-5.25	V dc
Power Supply Current				
+15V dc Supply	–	+26	+28	mA
-15V dc Supply	–	-30	-33	mA
+5V dc Supply①	–	+347	+372	mA
-5V dc Supply	–	-255	-285	mA
Power Dissipation	–	3.85	4.2	Watts
Power Supply Rejection	–	0.05	0.1	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range (Case)				
-MC	0	–	+70	°C
-MM	-55	–	+125	°C
Storage Temperature Range	-65	–	+150	°C
Weight	0.56 oz. (16 grams) Max.			
Package Type	40-Pin hermetic sealed, ceramic TDIP			

① +5V power usage at 1 TTL logic loading per data output bit.
② The same specifications apply to Inband Harmonics.

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TECHNICAL NOTES

1. Use external potentiometers to remove system errors or to reduce the small initial errors to zero. Use a 20K trimming potentiometer for gain adjustment with the wiper tied to pin 15 (tie pin 15 to ANALOG GROUND for operation without adjustments). Use a 20K trimming potentiometer with the wiper tied to pin 11 for zero/offset adjustment (tie pin 11 to ANALOG GROUND for operation without adjustment).

2. Rated performance requires using good high-frequency circuit board layout techniques. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter.

   In most cases, users will use a single +5V supply for both analog +5V and digital +5V (applicable for the -5V supply also). Should users have separate supplies the difference between the analog and digital supply should be within ±100 mV to avoid performance degradation.

   Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies. This prevents contamination of the analog ground by noisy digital ground currents.

3. Bypass all the analog and digital power supply pins with a 2.2 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor to their respective analog and digital grounds. Use of chip capacitors is recommended.

4. Obtain offset binary output coding by tying $\overline{\text{COMP BIN}}$ (pin 39) to +5V dc. To obtain complementary offset binary output coding, tie pin 39 to ground. The pin 39 signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

5. To obtain three-state outputs, connect the $\overline{\text{ENABLE}}$ pin (pin 38) to a logic "1" (high). Otherwise, connect pin 38 to a logic "0" (low).

6. The ADS-130 guarantees it's specified throughput rate over the temperature range when the START CONVERT pulse of 10 nS minimum, 90 nS maximum is provided at the specified rate. Start convert pulses greater than 90 nanoseconds will result in slower throughput rates.

7. The ADS-130 is capable of digitizing sinusoidal input frequencies up to the Nyquist frequency. The acquisition time for pulse or dc level signals is 50 nS maximum over the 0 to +70 °C temperature range. Acquisition time is 70 nSec. maximum from -55 °C to +125 °C.

8. The specifications listed in Figure 2 (timing diagram) apply over the full operating temperature range unless otherwise specified.

9. The OVERFLOW pin goes high for signals greater than +full scale (no overflow flag given for signals greater than -FS). The OVERFLOW pin is a three-state output and is enabled by pin 38.

10. The ADS-130 has a one pipeline delay in obtaining output data. Refer to the Timing Diagram in Figure 3.

11. The ADS-130 goes into the hold mode on the rising edge of the start convert pulse.

CALIBRATION PROCEDURE

1. Connect the converter per Figure 2.
Apply a pulse of 10 nS typical to the START CONVERT input (pin 35) at a rate of 500 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments
Apply a precision voltage reference source between the analog input (pin 6) and analog ground. Adjust the output of the reference source per Table 2 for the bipolar zero adjustment (zero +1/2 LSB). Adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with COMP BIN (pin 39) tied high (offset binary) or between 0111 1111 1111 and 0111 1111 1110 with pin 39 tied low (complementary offset binary).

3. Full-Scale Adjustment
Set the output of the voltage reference used in step 2 to the value shown in Table 2 for the bipolar gain adjustment (+FS -1 1/2 LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 with pin 39 tied high or between 0000 0000 0000 and 0000 0000 0001 with pin 39 tied low.

To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 3.

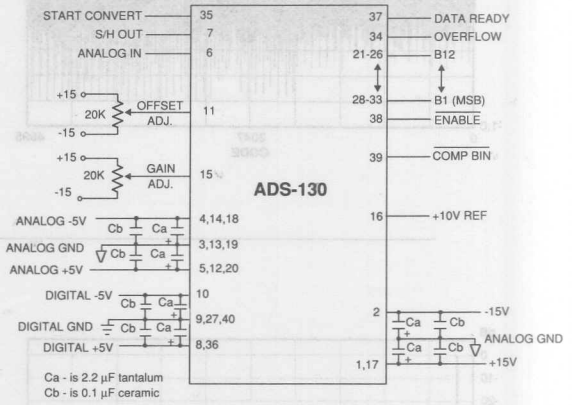
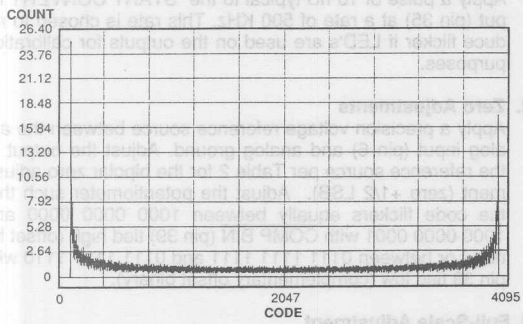


Figure 2. Typical ADS-130 Connection Diagram

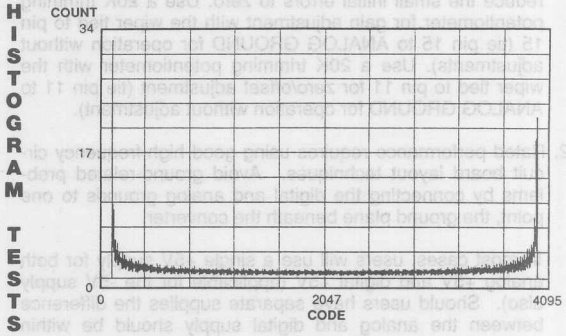
Table 2. Zero and Gain Adjust

FSR	ZERO ADJUST 0 + 1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
±1.25Vdc	+305 µV dc	+1.249085V dc

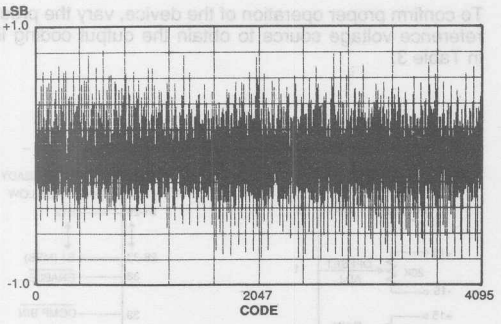
FIN = 180 KHz

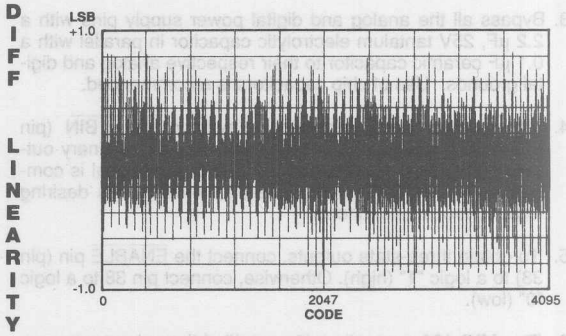


FIN = 949 KHz

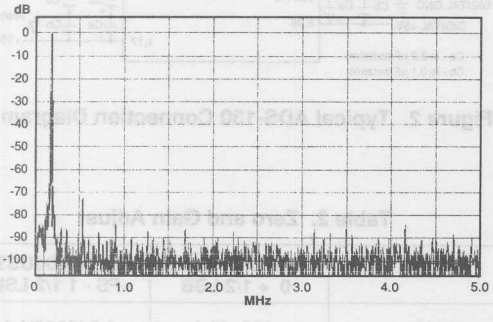


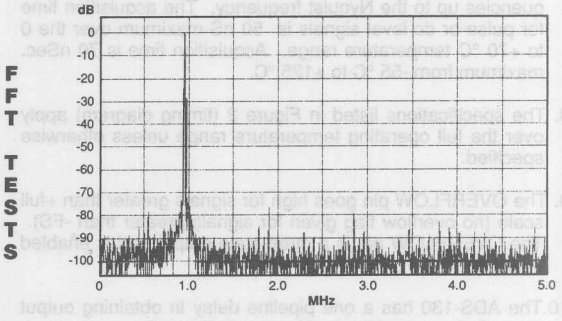
HISTOGRAM TESTS





DIFF LINEARITY





FFT TESTS

NOTE: FCLOCK = 10 MHz for all presentations

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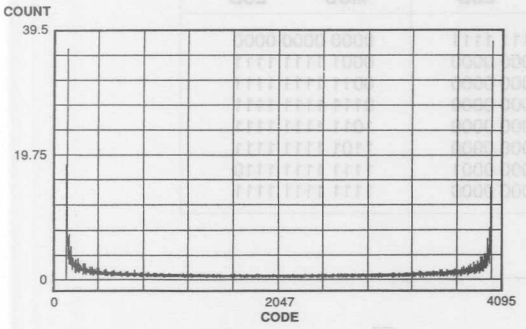
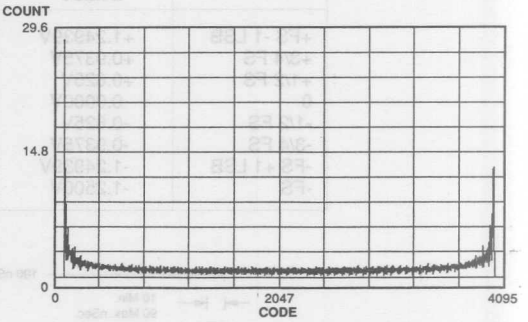
HISTOGRAM TESTS

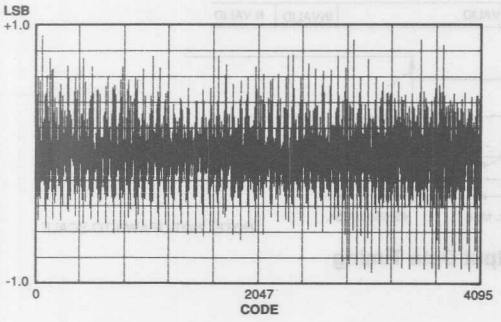
FIN = 1.89 MHz

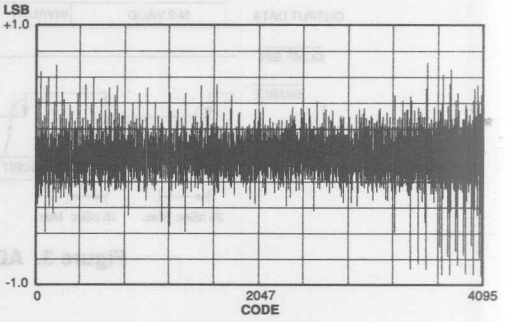


FIN = 4.85 MHz

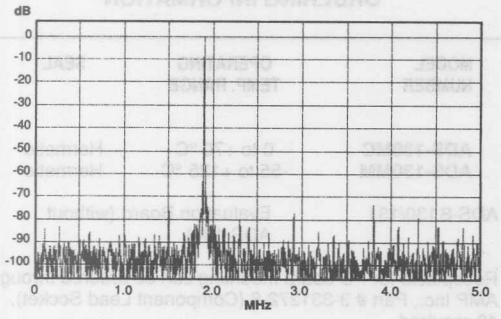


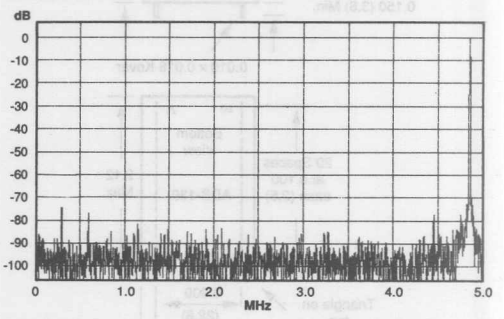
DIFF LINEARITY





FFT TESTS





NOTE: FCLOCK = 10 MHz for all presentations

	±1.25V	MSB LSB	MSB LSB
+FS -1 LSB	+1.24939V	1111 1111 1111	0000 0000 0000
+3/4 FS	+0.9375V	1110 0000 0000	0001 1111 1111
+1/2 FS	+0.625V	1100 0000 0000	0011 1111 1111
0	0.0000V	1000 0000 0000	0111 1111 1111
-1/2 FS	-0.625V	0100 0000 0000	1011 1111 1111
-3/4 FS	-0.9375V	0010 0000 0000	1101 1111 1111
-FS +1 LSB	-1.24939V	0000 0000 0001	1111 1111 1110
-FS	-1.2500V	0000 0000 0000	1111 1111 1111

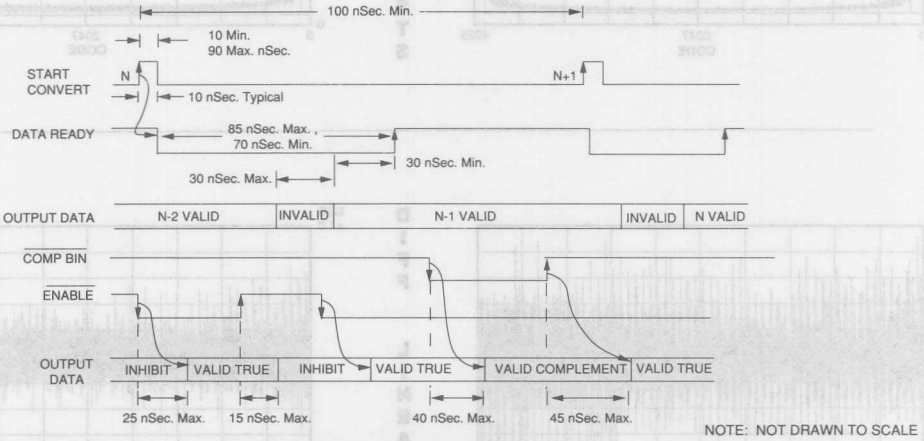
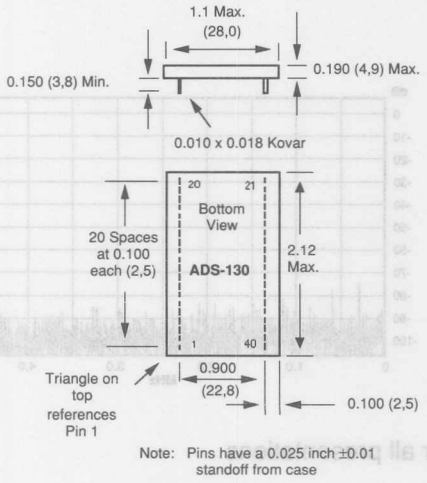


Figure 3. ADS-130 Output Data Timing

MECHANICAL DIMENSIONS INCHES (mm)



Note: Pins have a 0.025 inch ±0.01 standoff from case

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	SEAL
ADS-130MC	0 to +70 °C	Hermetic
ADS-130MM	-55 to +125 °C	Hermetic
ADS-B130/131	Evaluation Board (without ADS-130)	

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 40 required.

For availability of MIL-STD-883B versions, contact DATEL.

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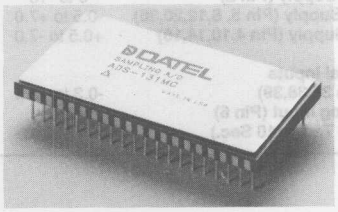
ADS-131
12-Bit, 5.0 MHz Sampling A/D Converter

FEATURES

- 12-Bit resolution
- Internal Sample/Hold amplifier
- 5.0 MHz minimum throughput
- Samples up to Nyquist
- Functionally Complete
- Small 40-pin DIP
- Low-power, 3.65 Watts
- Three-State output buffers
- High input bandwidth
- Overflow pin
- No missing codes

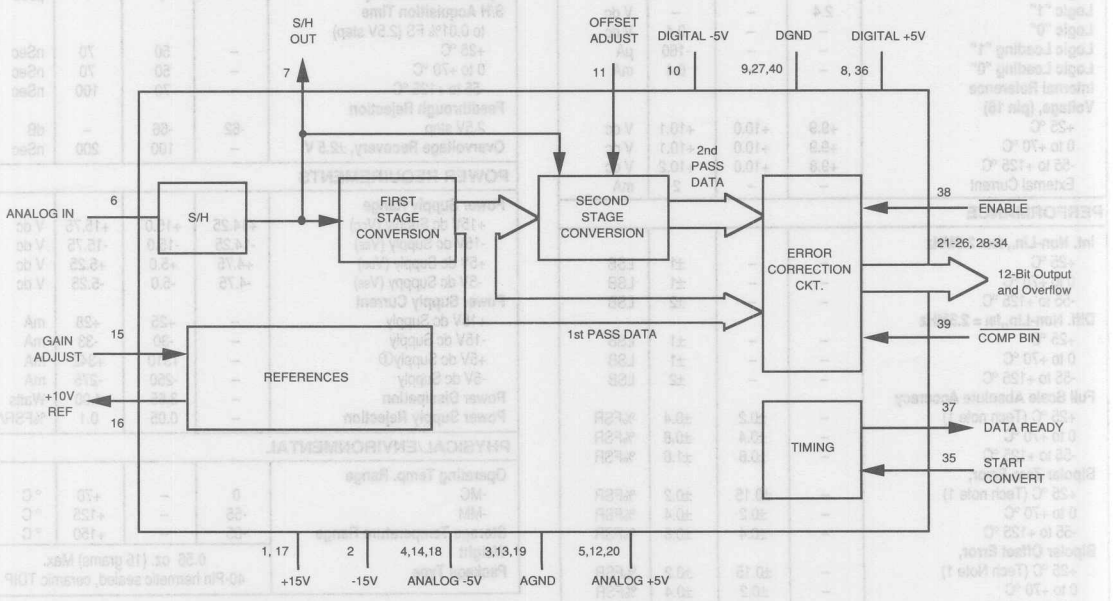


GENERAL DESCRIPTION

DATEL's ADS-131 is a 12-bit, functionally complete, sampling A/D converter packaged in a small 40-pin DIP. A 5.0 MHz minimum throughput rate in digitizing sinusoidal signals is achieved while only dissipating 3.65 Watts.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+15V	40	DIGITAL GROUND
2	-15V	39	COMP BIN
3	ANALOG GROUND	38	ENABLE
4	ANALOG -5V	37	DATA READY
5	ANALOG +5V	36	DIGITAL +5V
6	ANALOG INPUT	35	START CONVERT
7	S/H OUT	34	OVERFLOW
8	DIGITAL +5V	33	BIT 1 (MSB)
9	DIGITAL GROUND	32	BIT 2 OUT
10	DIGITAL -5V	31	BIT 3 OUT
11	OFFSET ADJUST	30	BIT 4 OUT
12	ANALOG +5V	29	BIT 5 OUT
13	ANALOG GROUND	28	BIT 6 OUT
14	ANALOG -5V	27	DIGITAL GROUND
15	GAIN ADJUST	26	BIT 7 OUT
16	+10V REFERENCE	25	BIT 8 OUT
17	+15V SUPPLY	24	BIT 9 OUT
18	ANALOG -5V	23	BIT 10 OUT
19	ANALOG GROUND	22	BIT 11 OUT
20	ANALOG +5V	21	BIT 12 OUT (LSB)



ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 1,17)	0 to +18	Volts dc
-15V Supply (Pin 2)	0 to -18	Volts dc
+5V Supply (Pin 5, 8,12,20,36)	-0.5 to +7.0	Volts dc
-5V Supply (Pin 4,10,14,18)	+0.5 to -7.0	Volts dc
Digital Inputs (Pins 35,38,39)	-0.3 to +5.5	Volts dc
Analog Input (Pin 6)	±5	Volts dc
Lead Temp.(10 Sec.)	300	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and ±5V dc unless otherwise specified.

INPUTS	MIN	TYP	MAX	UNITS
Analog				
Input Voltage Range	–	±1.25	–	V dc
Input Impedance	50	160	–	KOhm
Input Capacitance	–	2.5	10	pF
Digital				
Logic Levels				
Logic "1"	2.0	–	–	V dc
Logic "0"	–	–	0.8	V dc
Logic Loading "1"	–	–	5.0	µA
Logic Loading "0"	–	–	-200	µA
OUTPUTS				
Resolution				
Output Coding				
(Pin 39 HI)				
(Pin 39 Low)				
Logic Levels				
Logic "1"	2.4	–	–	V dc
Logic "0"	–	–	0.4	V dc
Logic Loading "1"	–	–	-160	µA
Logic Loading "0"	–	–	6.4	mA
Internal Reference Voltage, (pin 16)				
+25 °C	+9.9	+10.0	+10.1	V dc
0 to +70 °C	+9.9	+10.0	+10.1	V dc
-55 to +125 °C	+9.8	+10.0	+10.2	V dc
External Current	–	–	2	mA
PERFORMANCE				
Int. Non-Lin., f_{IN}= 2.5MHz				
+25 °C	–	–	±1	LSB
0 to +70 °C	–	–	±1	LSB
-55 to +125 °C.	–	–	±2	LSB
Diff. Non-Lin.,f_{IN} = 2.5MHz				
+25 °C	–	–	±1	LSB
0 to +70 °C	–	–	±1	LSB
-55 to +125 °C	–	–	±2	LSB
Full Scale Absolute Accuracy				
+25 °C (Tech note 1)	–	±0.2	±0.4	%FSR
0 to +70 °C	–	±0.4	±0.8	%FSR
-55 to +125 °C	–	±0.8	±1.6	%FSR
Bipolar Zero Error,				
+25 °C (Tech note 1)	–	±0.15	±0.2	%FSR
0 to +70 °C	–	±0.2	±0.4	%FSR
-55 to +125 °C	–	±0.4	±0.8	%FSR
Bipolar Offset Error,				
+25 °C (Tech Note 1)	–	±0.15	±0.2	%FSR
0 to +70 °C	–	±0.2	±0.4	%FSR
-55 to +125 °C	–	±0.4	±0.8	%FSR

A/D PERF. CONT.	MIN	TYP	MAX	UNITS
Gain Error, +25 °C				
(Tech Note 1)	–	±0.15	±0.2	%FSR
0 to +70 °C	–	±0.2	±0.4	%FSR
-55 to +125 °C	–	±0.4	±0.8	%FSR
No Missing Codes (12 Bits, at f_{IN} = 2.5 MHz)	Over Operating Temperature Range			
DYNAMIC PERFORMANCE				
Conversion Rate				
(Changing Inputs),+25 °C	5.0	–	–	MHz
0 to +70 °C	5.0	–	–	MHz
-55 to +125 °C	5.0	–	–	MHz
Total Harm. Distort.(-0.5 dB)				
DC to 500 KHz	-68	-70	–	FS, -dB
500 KHz to 2.5 MHz	-65	-67	–	FS, -dB
Signal-to-Noise Ratio (w/o distortion, -0.5 dB)				
DC to 500 KHz	-67	-70	–	FS, -dB
500 KHz to 2.5 MHz	-65	-69	–	FS, -dB
Signal-to-Noise Ratio and Distortion (-0.5 dB)				
DC to 500 KHz	-65	-66	–	FS, -dB
500 KHz to 2.5 MHz	-63	-65	–	FS, -dB
Spurious Free Dynamic Range②				
DC to 500 KHz	-68	-70	–	FS, -dB
500 KHz to 2.5 MHz	-65	-67	–	FS, -dB
Effective Bits				
DC to 500 KHz	10.6	11.0	–	bits
500 KHz to 2.5 MHz	10.2	10.5	–	bits
Two-tone Intermodulation Distortion (f_{IN} =2.2 MHz, 2.3 MHz, Fs = 5 MHz)	-72	-75	–	dB
Input Bandwidth				
Small Signal (-20 dB input)	50	65	–	MHz
Full Power (0 dB input)	30	40	–	MHz
Slew Rate	75	100	–	V/µSec
Aperture Delay Time	–	5	7	nSec
Aperture Uncertainty	–	5	7	psec
S/H Acquisition Time to 0.01% FS (2.5V step)				
+25 °C	–	50	70	nSec
0 to +70 °C	–	50	70	nSec
-55 to +125 °C	–	70	100	nSec
Feedthrough Rejection 2.5V step	-62	-66	–	dB
Overvoltage Recovery, ±2.5 V	–	100	200	nSec
POWER REQUIREMENTS				
Power Supply Range				
+15V dc Supply (V_{CC})	+14.25	+15.0	+15.75	V dc
-15V dc Supply (V_{EE})	-14.25	-15.0	-15.75	V dc
+5V dc Supply (V_{DD})	+4.75	+5.0	+5.25	V dc
-5V dc Supppy (V_{SS})	-4.75	-5.0	-5.25	V dc
Power Supply Current				
+15V dc Supply	–	+25	+28	mA
-15V dc Supply	–	-30	-33	mA
+5V dc Supply①	–	+310	+342	mA
-5V dc Supply	–	-250	-275	mA
Power Dissipation	–	3.65	4.00	Watts
Power Supply Rejection	–	0.05	0.1	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range				
-MC	0	–	+70	°C
-MM	-55	–	+125	°C
Storage Temperature Range	-65	–	+150	°C
Weight	0.56 oz. (16 grams) Max.			
Package Type	40-Pin hermetic sealed, ceramic TDIP			

① +5V power usage at 1 TTL logic loading per data output bit.
② The same specifications apply to Inband Harmonics.

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1. Use external potentiometers to remove system errors or to reduce the small initial errors to zero. Use a 20K trimming potentiometer for gain adjustment with the wiper tied to pin 15 (tie pin 15 to ANALOG GROUND for operation without adjustments). Use a 20K trimming potentiometer with the wiper tied to pin 11 for zero/offset adjustment (tie pin 11 to ANALOG GROUND for operation without adjustment).

2. Rated performance requires using good high-frequency circuit board layout techniques. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter.

   In most cases, users will use a single +5V supply for both analog +5V and digital +5V (applicable for the -5V supply also). Should users have separate supplies the difference between the analog and digital supply should be within ±100 mV to avoid performance degradation.

   Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies. This prevents contamination of the analog ground by noisy digital ground currents.

3. Bypass all the analog and digital power supply pins with a 2.2 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor to their respective analog and digital grounds. Use of chip capacitors is recommended.

4. Obtain offset binary output coding by tying $\overline{\text{COMP BIN}}$ (pin 39) to +5V dc. To obtain complementary offset binary output coding, tie pin 39 to ground. The pin 39 signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

5. To obtain three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 38) to a logic "1" (high). Otherwise, connect pin 38 to a logic "0" (low).

6. The ADS-131 guarantees it's specified throughput rate over the temperature range when the START CONVERT pulse of 10 nS minimum, 190 nS maximum is provided at the specified rate. Start convert pulses greater than 190 nanoseconds will result in slower throughput rates.

7. The ADS-131 is capable of digitizing sinusoidal input frequencies up to the Nyquist frequency. The acquisition time for pulse or dc level signals is 70 nS maximum over the 0 to +70 °C temperature range. Acquisition time is 100 nSec. maximum from -55 °C to +125 °C.

8. The specifications listed in Figure 3 (timing diagram) apply over the full operating temperature range unless otherwise specified.

9. The OVERFLOW pin goes high for signals greater than +full scale (no overflow flag given for signals greater than -FS). The $\overline{\text{OVERFLOW}}$ pin is a three-state output and is enabled by the $\overline{\text{ENABLE}}$ line (pin 38).

10. The ADS-131 has a one pipeline delay in obtaining output data. Refer to the Timing Diagram in Figure 3.

11. ADS-131 goes into the hold mode on the rising edge of the start convert pulse.

1. **Connect the converter per Figure 2.**
   Apply a pulse of 10 nS typical to the START CONVERT input (pin 35) at a rate of 500 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. **Zero Adjustments**
   Apply a precision voltage reference source between the analog input (pin 6) and analog ground. Adjust the output of the reference source per Table 2 for the bipolar zero adjustment (zero +1/2 LSB). Adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with $\overline{\text{COMP BIN}}$ (pin 39 tied high (offset binary) or between 0111 1111 1111 and 0111 1111 1110 with pin 39 tied low (complementary offset binary).

3. **Full-Scale Adjustment**
   Set the output of the voltage reference used in step 2 to the value shown in Table 2 for the bipolar gain adjustment (+FS -1 1/2 LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 with $\overline{\text{COMP BIN}}$ (pin 39) tied high or between 0000 0000 0000 and 0000 0000 0001 with pin 39 tied low.

   To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 3.

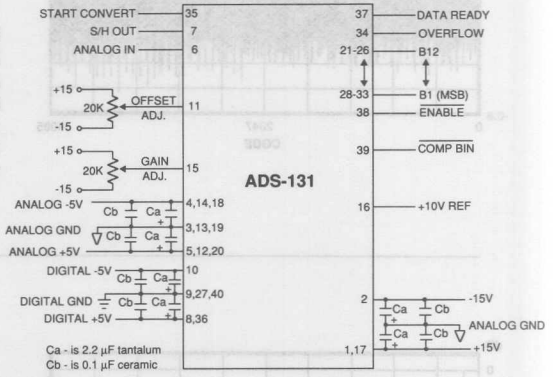


Figure 2. Typical ADS-131 Connection Diagram

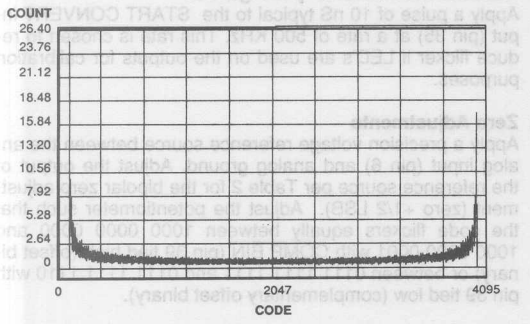
Table 2. Zero and Gain Adjust

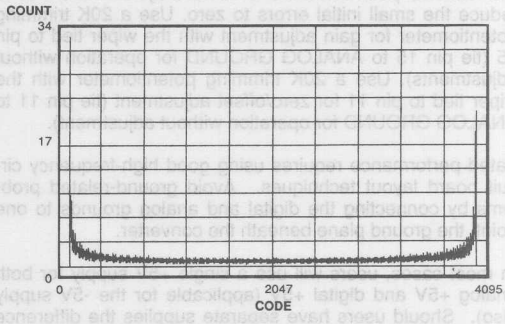
FSR	ZERO ADJUST 0 + 1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
±1.25Vdc	+305 µV dc	+1.249085V dc

FIN = 95 KHz

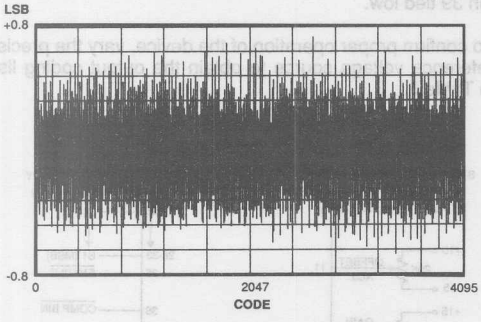
FIN =495 KHz

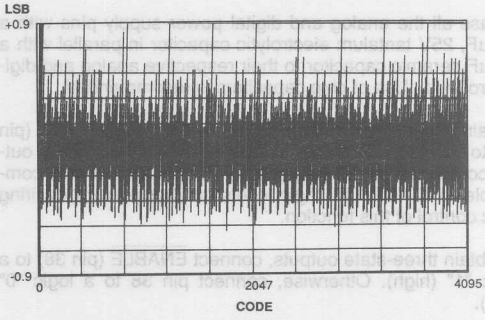
HISTOGRAM TESTS



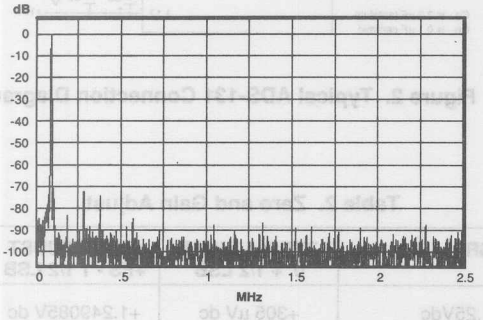


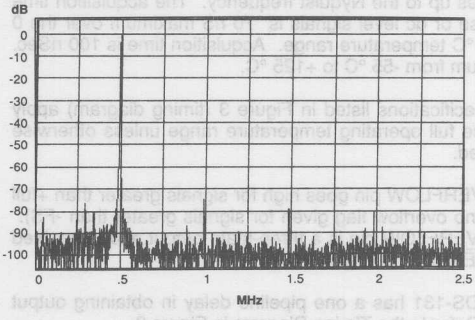
DIFF LINEARITY





FFT TESTS





NOTE: FCLOCK = 5 MHz for all presentations

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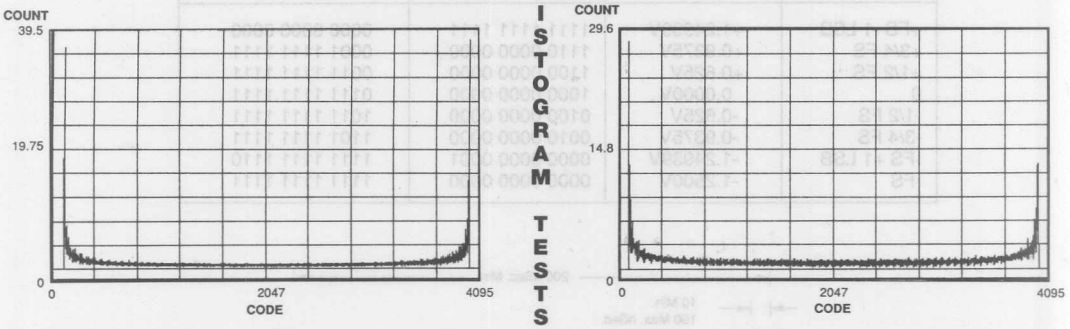
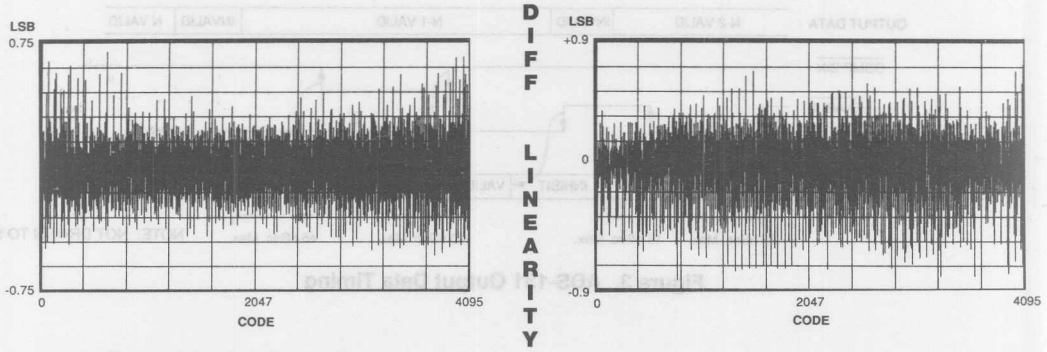
FIN = 985 KHz **FIN = 2.45 MHz**

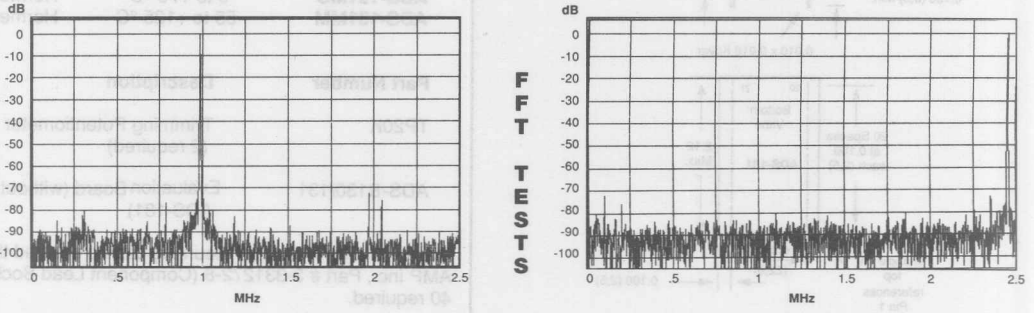
HISTOGRAM TESTS



DIFF LINEARITY



FFT TESTS



NOTE: FCLOCK = 5 MHz for all presentations

Table 3. Output Coding for Bipolar Operation

BIPOLAR SCALE	INPUT RANGE (Volts dc) ±1.25V	OUTPUT CODING OFFSET BINARY MSB LSB	OUTPUT CODING COMP OFF. BINARY MSB LSB
+FS -1 LSB	+1.24939V	1111 1111 1111	0000 0000 0000
+3/4 FS	+0.9375V	1110 0000 0000	0001 1111 1111
+1/2 FS	+0.625V	1100 0000 0000	0011 1111 1111
0	0.0000V	1000 0000 0000	0111 1111 1111
-1/2 FS	-0.625V	0100 0000 0000	1011 1111 1111
-3/4 FS	-0.9375V	0010 0000 0000	1101 1111 1111
-FS +1 LSB	-1.24939V	0000 0000 0001	1111 1111 1110
-FS	-1.2500V	0000 0000 0000	1111 1111 1111

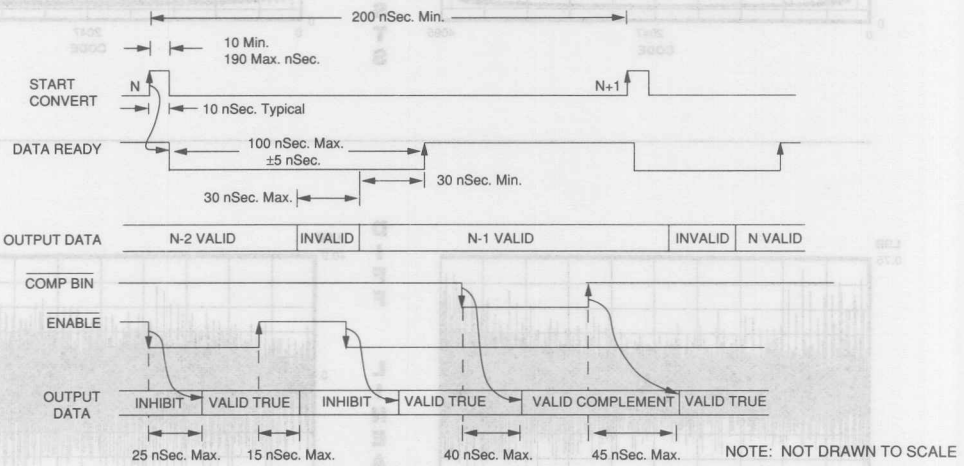
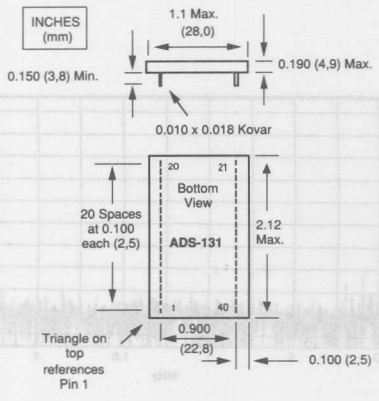


Figure 3. ADS-131 Output Data Timing

MECHANICAL DIMENSIONS INCHES (mm)



Note: Pins have a 0.025 inch ±0.01 standoff from case

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	SEAL
ADS-131MC	0 to +70 °C	Hermetic
ADS-131MM	-55 to +125 °C	Hermetic

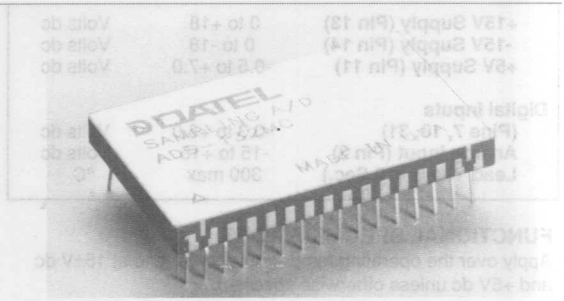
Part Number	Description
TP20K	Trimming Potentiometer (2 required)
ADS-B130/131	Evaluation Board (without ADS-131)

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 40 required.

For availability of MIL-STD-883B versions, contact DATEL.

FEATURES

- 12-Bit resolution
- Internal Sample/Hold
- 2.0 MHz minimum throughput
- Functionally complete
- Small 32-pin DIP
- Low-power, 2.9 Watts
- Three-state output buffers
- Samples up to Nyquist
- No -5V supply required

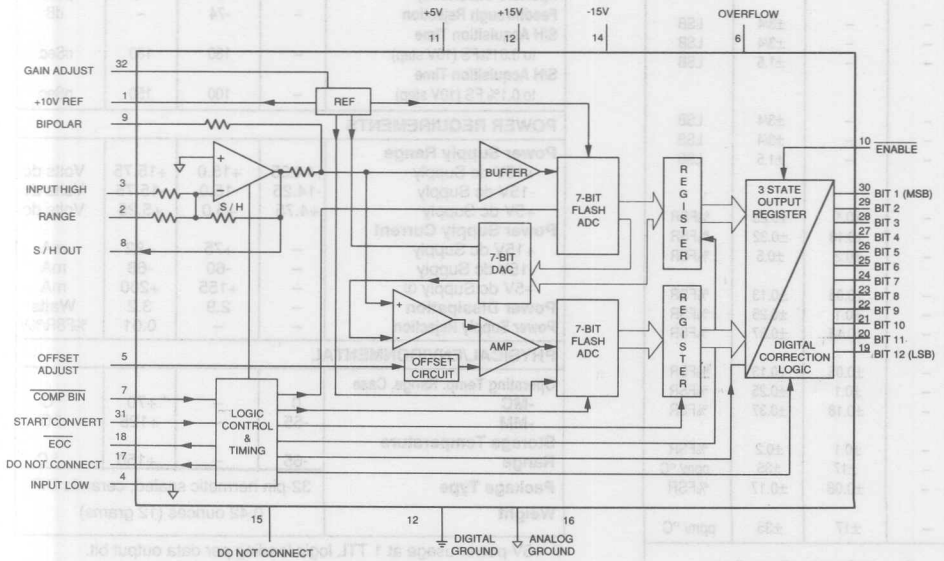


GENERAL DESCRIPTION

DATEL's ADS-132 is a 12-bit, functionally complete, sampling A/D converter that is packaged in a small 32-pin ceramic DIP. The ADS-132 digitizes sinusoidal signals at a 2.0 MHz minimum throughput rate while dissipating only 2.9 Watts.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+10V REF. OUT	17	DO NOT CONNECT
2	RANGE	18	$\overline{EOC}$
3	INPUT HIGH	19	BIT 12 OUT (LSB)
4	INPUT LOW	20	BIT 11 OUT
5	OFFSET ADJUST	21	BIT 10 OUT
6	OVERFLOW	22	BIT 9 OUT
7	$\overline{COMP. BIN}$	23	BIT 8 OUT
8	S/H OUT	24	BIT 7 OUT
9	BIPOLAR	25	BIT 6 OUT
10	$\overline{ENABLE}$ (1 - 12)	26	BIT 5 OUT
11	+5	27	BIT 4 OUT
12	DIGITAL GROUND	28	BIT 3 OUT
13	+15V	29	BIT 2 OUT
14	-15V	30	BIT 1 OUT (MSB)
15	DO NOT CONNECT	31	START CONVERT
16	ANALOG GROUND	32	GAIN ADJUST



ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 13)	0 to +18	Volts dc
-15V Supply (Pin 14)	0 to -18	Volts dc
+5V Supply (Pin 11)	-0.5 to +7.0	Volts dc
Digital Inputs (Pins 7, 10, 31)	-0.3 to +6.0	Volts dc
Analog Input (Pin 3)	-15 to +15	Volts dc
Lead Temp. (10 Sec.)	300 max	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at 15±V dc and +5V dc unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range				
ADS-132	–	0 to -5	–	Volts dc
(See Table 1 also)	–	0 to -10	–	Volts dc
	–	0 to -20	–	Volts dc
	–	0 to +10	–	Volts dc
	–	±5	–	Volts dc
	–	±10	–	Volts dc
Input Impedance				
Input Ranges:				
(0 to -10, -20, +10, ±10)	800	1,000	–	Ohms
(0 to -5, ±5V)	400	500	–	Ohms
Input Capacitance	–	2	–	pf
DIGITAL INPUTS				
Logic Levels				
Logic "1"	2.0	–	–	Volts dc
Logic "0"	–	–	0.8	Volts dc
Logic Loading "1"	–	–	5.0	µA
Logic Loading "0"	–	–	-200	µA
PERFORMANCE				
Integral Non-Linearity @FIN=1MHz				
+25 °C	–	–	±3/4	LSB
0 °C to +70 °C	–	–	±3/4	LSB
-55 °C to +125 °C	–	–	±1.5	LSB
Differential Non-Linearity @FIN=1MHz				
+25 °C	–	–	±3/4	LSB
0 °C to +70 °C	–	–	±3/4	LSB
-55 °C to +125 °C	–	–	±1.5	LSB
Full Scale Absolute Accuracy (See Tech Note 1)				
+25 °C.	–	±0.1	±0.25	%FSR
0 °C to +70 °C	–	±0.13	±0.32	%FSR
-55 °C to +125 °C	–	±0.2	±0.5	%FSR
Unipolar Zero Error				
+25 °C (See Tech Note 1)	–	±0.05	±0.13	%FSR
0 °C to +70 °C	–	±0.1	±0.25	%FSR
-55 °C to +125 °C	–	±0.18	±0.37	%FSR
Bipolar Zero Error				
+25 °C (See Tech Note 1)	–	±0.05	±0.13	%FSR
0 °C to +70 °C	–	±0.1	±0.25	%FSR
-55 °C to +125 °C	–	±0.18	±0.37	%FSR
Bipolar Offset Error, +25 °C (See Tech Note 1)	–	±0.1	±0.2	%FSR
Bipolar Offset Tempco	–	±17	±35	ppm/ °C
Gain Error, +25 °C (See Tech Note 1)	–	±0.08	±0.17	%FSR
Gain Tempco	–	±17	±35	ppm/ °C
No Missing Codes (12 Bits)	Over the Operating Temp. Range.			

OUTPUTS	MIN.	TYP.	MAX.	UNITS
Resolution	12 Bits			
Output Coding	Straight binary/offset binary Complementary binary/Complementary offset binary			
Logic Levels				
Logic "1"	2.4	–	–	Volts dc
Logic "0"	–	–	0.4	Volts dc
Logic Loading "1"	–	–	-160	µA
Logic Loading "0"	–	–	4.8	mA
Internal Reference Voltage, +25 °C	+9.98	+10.0	+10.02	Volts dc
Drift	–	±5	±30	ppm/ °C
External Current	–	–	2	mA
DYNAMIC PERFORMANCE				
Conversion Rate, 12-Bits	2	–	–	MHz
Total Harm. Distort. (-0.5 dB)				
DC to 100 KHz	-72	-80	–	FS,-dB
100 KHz to 500 KHz	-70	-75	–	FS,-dB
500 KHz to 1 MHz	-67	-71	–	FS, -dB
Signal to Noise Ratio (w/o distort., -0.5 dB)				
DC to 100 KHz	-70	-72	–	FS,-dB
100 KHz to 500 KHz	-68	-70	–	FS, -dB
500 KHz to 1 MHz	-66	-68	–	FS, -dB
Signal-to-Noise Ratio (with distort., -0.5 dB)				
DC to 100 KHz	-68	-70	–	FS, -dB
100 KHz to 500 KHz	-66	-68	–	FS, -dB
500 KHz to 1 MHz	-65	-67	–	FS, -dB
Effective Bits, -0.5 dB				
DC to 100 KHz	11.0	11.25	–	Bits
100 KHz to 500 KHz	10.7	11.1	–	Bits
500 KHz to 1 MHz	10.4	11.0	–	Bits
Two-Tone Intermodulation Distort. (*f*in = 490 KHz, 480 KHz, Fs = 2 MHz, -0.5 dB	-67	-70	–	FS, -dB
Input Bandwidth				
Small Signal (-20 dB input)	16	–	–	MHz
Full Power (0 dB input)	8	–	–	MHz
Slew Rate	–	300	–	V/µSec.
Aperture Delay Time	–	6	–	nSec.
Aperture Uncertainty	–	5	40	pSec.
Feedthrough Rejection	–	-74	–	dB
S/H Acquisition Time to 0.01%FS (10V step)	–	160	180	nSec.
S/H Acquisition Time to 0.1% FS (10V step)	–	100	150	nSec.
POWER REQUIREMENTS				
Power Supply Range				
+15V dc Supply	+14.25	+15.0	+15.75	Volts dc
-15V dc Supply	-14.25	-15.0	-15.75	Volts dc
+5V dc Supply	+4.75	+5.0	+5.25	Volts dc
Power Supply Current				
+15V dc Supply	–	+75	+82	mA
-15V dc Supply	–	-60	-68	mA
+5V dc Supply ①	–	+155	+200	mA
Power Dissipation	–	2.9	3.2	Watts
Power Supply Rejection	–	–	0.01	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range, Case				
-MC	0	–	+70	°C
-MM	-55	–	+125	°C
Storage Temperature Range	-65	–	+150	°C
Package Type	32-pin hermetic sealed, ceramic DIP			
Weight	0.42 ounces (12 grams)			

① +5V power usage at 1 TTL logic loading per data output bit.

Specifications subject to change without notice.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

TECHNICAL NOTES

1. Use external potentiometers to remove system errors or the small initial errors to zero. Use a 20K trimming potentiometer for gain adjustment with the wiper tied to pin 32 (ground pin 32 for operation without adjustments). Use a 20K trimming potentiometer with the wiper tied to pin 5 for zero/offset adjustment (leave pin 5 open for operation without adjustment). See Figure 3.

2. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

3. Bypass the analog and digital supplies and the +10V reference (pin 1) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 1) to analog ground (pin 16).

4. To enable the three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 10) to a logic "0" (low). To disable, connect $\overline{\text{ENABLE}}$ (pin 10) to a logic "1" (high).

5. The ADS-132 is in the sample mode when the internal S/$\overline{\text{H}}$ CONTROL pin is high (S/H is in the high-state on power-up). The START CONVERT pulse should be given at a time delay equal to the desired acquisition time minus the 10 nanosecond delay from START CONVERT high to S/H CONTROL low. This assures the sample-hold has the minimum required acquisition time for the particular application mode.

6. Upon going into the hold mode there will be a 85 nanosecond maximum delay before $\overline{\text{EOC}}$ goes high and the A/D conversion begins. This consists for the remaining 50 nanoseconds of the START CONVERT (10 nanoseconds is part of the acquisition time) and a 20 nanosecond maximum delay from START CONVERT low to $\overline{\text{EOC}}$ high. The hold mode settling time requirement is met during this time.

7. Figure 2 shows the relationship between the various input signals. The timing shown applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3, and **Tables 1 and 4** for the appropriate full-scale range (FSR). Apply a pulse of 60 nanoseconds minimum to the START CONVERT input (pin 31) at a rate of 500 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments
   Apply a precision voltage reference source between the amplifier's analog input and ground. Adjust the output of the reference source per **Table 2**. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 (straight binary) or between 1111 1111 1111 and 1111 1111 1110 (complementary binary).

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 (offset binary) or between 0111 1111 1111 and 0111 1111 1110 (complementary offset binary).

3. Full-Scale Adjustment
   Set the output of the voltage reference used in step 2 to the value shown in **Table 2**. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 (offset binary) or between 0000 0000 0001 and 0000 0000 0000 (complementary offset binary).

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in **Table 3**.

Table 1. ADS-132 Input Range Selection

INPUT RANGE	INPUT PIN	TIE TOGETHER
0 to -5V dc	Pin 3	Pin 8 to Pin 9, Pin 2 to Pin 3
0 to -10V dc	Pin 3	Pin 8 to Pin 9
0 to +10V dc	Pin 3	Pin 8 to Pin 9, Pin 2 to EXT.-10V Reference *
0 to -20V dc	Pin 3	Pin 1 to Pins 2 & 9
±5V dc	Pin 3	Pin 1 to Pin 9, Pin 2 to Pin 3
±10V dc	Pin 3	Pin 1 to Pin 9

* EXT -10V REF may be referenced to pin 1, EXT +10V REF

Table 2. Zero and Gain Adjust

FSR	ZERO ADJUST + 1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to -5V dc	-0.61 mV	-4.9982V dc
0 to -10V dc	-1.22 mV	-9.9963V dc
0 to +10 V dc	+1.22 mV	+9.9963V dc
0 to -20V dc	-2.44 mV	-19.9927V dc
±5V dc	+1.22mV dc	+4.9963V dc
±10V dc	+2.44 mV dc	+9.9927V dc

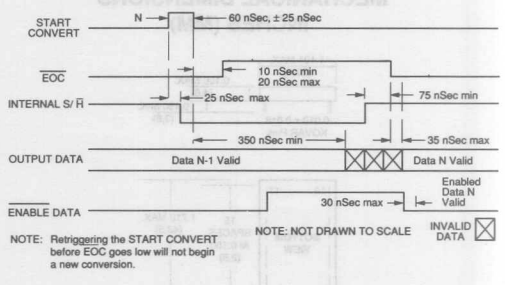


Figure 2. ADS-132 Timing Diagram

Table 3. Output Coding

					STRAIGHT BIN. COMP. BINARY						
UNIPOLAR	INPUT RANGES, V dc				OUTPUT CODING				INPUT RANGE		BIPOLAR
SCALE	0 to +10V	0 to -5V	0 to -10V	0 to -20V	MSB	LSB	MSB	LSB	±5V dc	±10V dc	SCALE
+FS -1 LSB	+9.9976V	-4.998V	-9.9976V	-19.9951V	1111	1111 1111	0000	0000 0000	+4.9976V	+9.9951V	+FS -1 LSB
7/8 FS	+8.7500V	-4.375V	-8.750V	-17.500V	1110	0000 0000	0001	1111 1111	+3.7500V	+7.5000V	+3/4 FS
3/4 FS	+7.5000V	-3.750V	-7.500V	-15.00V	1100	0000 0000	0011	1111 1111	-2.5000V	+5.0000V	+1/2 FS
1/2 FS	+5.0000V	-2.500V	-5.000V	-10.00V	1000	0000 0000	0111	1111 1111	0.0000V	0.0000V	0
1/4 FS	+2.5000V	-1.250V	-2.500V	-5.000V	0100	0000 0000	1011	1111 1111	-2.5000V	-5.0000V	-1/2 FS
1/8 FS	+1.2500V	-0.625V	-1.250V	-2.500V	0010	0000 0000	1101	1111 1111	-3.7500V	-7.5000V	-3/4 FS
1 LSB	+0.0024V	-0.0012V	-0.0024V	-0.0049V	0000	0000 0001	1111	1111 1110	-4.9976V	-9.9951V	-FS +1 LSB
0	0.0000V	0.0000V	0.000V	0.000V	0000	0000 0000	1111	1111 1111	-5.0000V	-10.000V	-FS
					OFF. BINARY		COMP. OFF. BIN.				

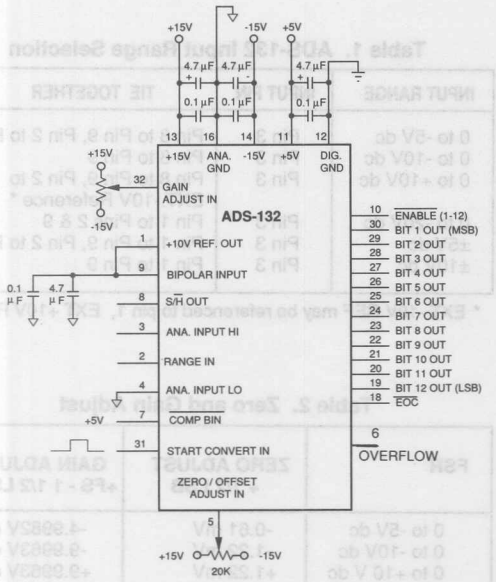
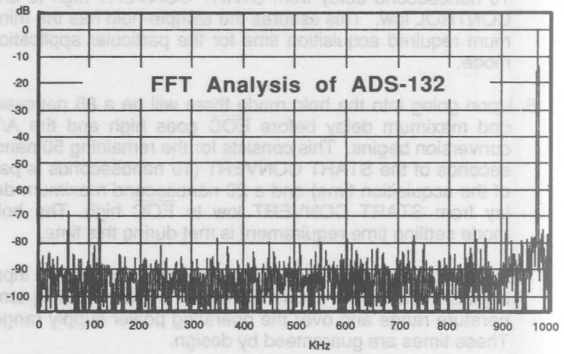


Figure 3. Typical ADS-132 Connection Diagram, ±10V dc

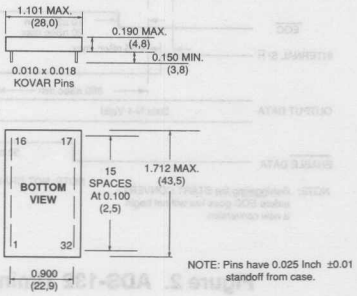
Table 4. COMP BIN (Pin 7) Connection

INPUT RANGE	COMPLEMENTARY BINARY	
	BINARY	
	Pin 7 logic state*	
0 to +10V	Low	High
0 to -5V	High	Low
0 to -10V	High	Low
0 to -20V	High	Low
±5V	Low	High
±10V	Low	High

* For logic state low connect to +5V. For logic state high leave open.



MECHANICAL DIMENSIONS INCHES (MM)



ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	SEAL
ADS-132MC	0 °C to +70 °C	Hermetic
ADS-132MM	-55 °C to +125 °C	Hermetic

Receptacle for PC board mounting can be ordered through AMP Inc., Part #3-331272-8 (Component Lead Socket), 24 required.

ADS-EVAL1 Evaluation Board (without ADS-132)

For availability of MIL-STD-883 versions, contact DATEL.

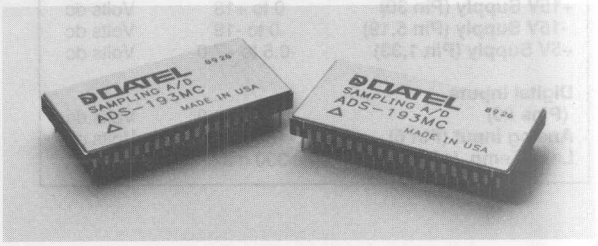
DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

ADS-193

12-Bit, 1.0 MHz, Low-Power Sampling A/D Converter

FEATURES

- **12-Bit resolution**
- **Internal Sample/Hold**
- **1.0 MHz minimum throughput**
- **Functionally complete**
- **Low-power, 1.3 Watts**
- **Samples to Nyquist**



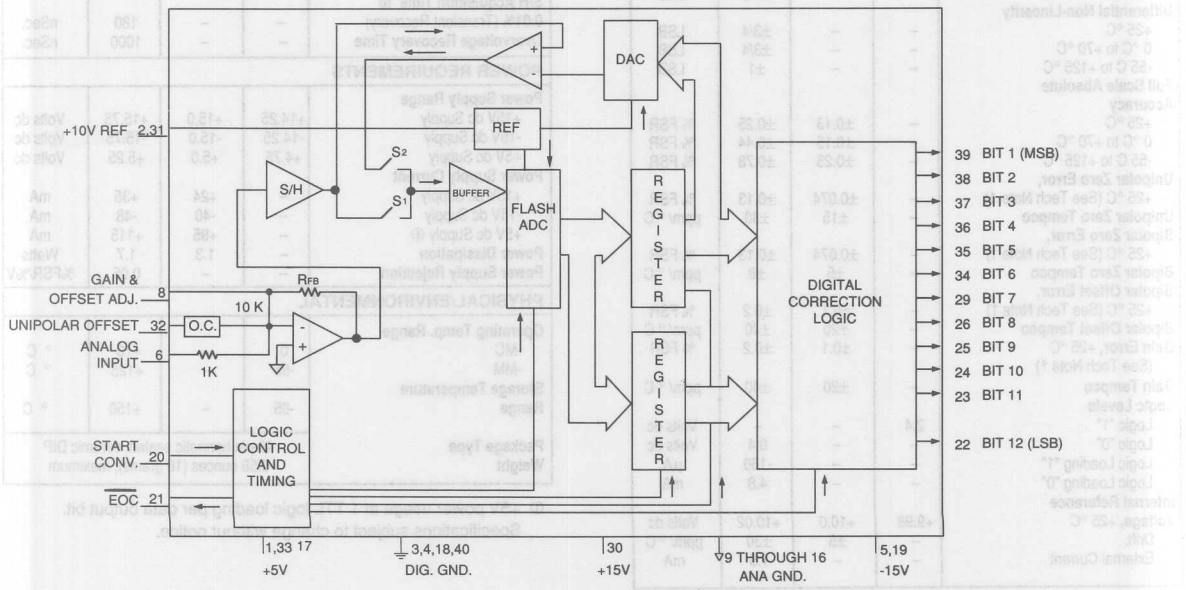
GENERAL DESCRIPTION

DATEL's ADS-193 is a 12-bit, functionally complete, sampling A/D converter that is packaged in a 40-pin ceramic DIP. A minimum throughput rate of 1.0 MHz is achieved while only dissipating 1.3 Watts. The ADS-193 digitizes signals up to Nyquist.

Typical applications include spectrum, transient, vibration and waveform analysis. This device is also ideally suited for radar, sonar, video digitization, medical instrumentation and high-speed data acquisition systems. For information on high reliability screening, contact DATEL.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+5V	40	DIGITAL GROUND
2	+10 V REFERENCE	39	BIT 1 OUT (MSB)
3	DIGITAL GROUND	38	BIT 2 OUT
4	DIGITAL GROUND	37	BIT 3 OUT
5	-15V	36	BIT 4 OUT
6	ANALOG INPUT	35	BIT 5 OUT
7	DO NOT CONNECT	34	BIT 6 OUT
8	GAIN OFFSET ADJ.	33	+5V
9	ANALOG GROUND	32	UNIPOLAR OFFSET
10	ANALOG GROUND	31	+10V REFERENCE
11	ANALOG GROUND	30	+15V
12	ANALOG GROUND	29	BIT 7 OUT
13	ANALOG GROUND	28	NO CONNECTION
14	ANALOG GROUND	27	NO CONNECTION
15	ANALOG GROUND	26	BIT 8 OUT
16	ANALOG GROUND	25	BIT 9 OUT
17	+5V	24	BIT 10 OUT
18	DIGITAL GROUND	23	BIT 11 OUT
19	-15V	22	BIT 12 OUT (LSB)
20	START CONVERT	21	EOC



ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 30)	0 to +18	Volts dc
-15V Supply (Pin 5,19)	0 to -18	Volts dc
+5V Supply (Pin 1,33)	-0.5 to +7.0	Volts dc
Digital Inputs (Pins 20)	-0.3 to +6.0	Volts dc
Analog Input (Pin 6)	-15 to +15	Volts dc
Lead Temp. (10 Sec.)	300 max	° C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and +5V dc unless otherwise specified..

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range	–	0 to -5	–	Volts dc
	–	±2.5	–	Volts dc
Input Impedance	950	1,000	1,050	Ohms
Input Capacitance	–	6	15	pf
DIGITAL INPUTS				
Logic Levels				
Logic "1"	2.0	–	–	Volts dc
Logic "0"	–	–	0.8	Volts dc
Logic Loading "1"	–	–	5.0	µA
Logic Loading "0"	–	–	-200	µA
A/D PERFORMANCE				
No Missing Codes (12 Bits; fin=500 KHz)	Over the Operating Temp. Range.			
Integral Non-Linearity				
+25 °C	–	±1/4	±3/4	LSB
0 °C to +70 °C	–	±1/4	±3/4	LSB
-55 C to +125 °C	–	–	±1.5	LSB
Differential Non-Linearity				
+25 °C	–	–	±3/4	LSB
0 °C to +70 °C	–	–	±3/4	LSB
-55 C to +125 °C	–	–	±1	LSB
Full Scale Absolute Accuracy				
+25 °C	–	±0.13	±0.25	% FSR
0 °C to +70 °C	–	±0.15	±0.44	% FSR
-55 C to +125 °C	–	±0.25	±0.78	% FSR
Unipolar Zero Error,				
+25 °C (See Tech Note 1)	–	±0.074	±0.13	% FSR
Unipolar Zero Tempco	–	±15	±30	ppm/ ° C
Bipolar Zero Error,				
+25 °C (See Tech Note 1)	–	±0.074	±0.13	% FSR
Bipolar Zero Tempco	–	±5	±8	ppm/ ° C
Bipolar Offset Error,				
+25 °C (See Tech Note 1)	–	±0.1	±0.2	% FSR
Bipolar Offset Tempco	–	±20	±40	ppm/ ° C
Gain Error, +25 °C (See Tech Note 1)	–	±0.1	±0.2	% FSR
Gain Tempco	–	±20	±40	ppm/ ° C
Logic Levels				
Logic "1"	2.4	–	–	Volts dc
Logic "0"	–	–	0.4	Volts dc
Logic Loading "1"	–	–	-160	µA
Logic Loading "0"	–	–	4.8	mA
Internal Reference Voltage, +25 °C	+9.98	+10.0	+10.02	Volts dc
Drift.	–	±5	±30	ppm/ ° C
External Current	–	–	1.5	mA

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Resolution	12 Bits			
Output Coding	Complementary binary Complementary offset binary			
PERFORMANCE				
Conversion Rate	1.0	–	–	MHz
In-Band Harmonics (-0.5dB)				
DC to 100 KHz	-76	-81	–	FS-dB
100 KHz to 500 KHz	-70	-75	–	FS-dB
Total Harm. Distort. (-0.5dB)				
DC to 100 KHz	-75	-78	–	FS-dB
100 KHz to 500 KHz	-68	-73	–	FS-dB
Signal-to-Noise Ratio (w/o distortion, -0.5dB)				
DC to 100 KHz	-68	-72	–	FS-dB
100 KHz to 500 KHz	-67	-71	–	FS-dB
Signal-to-Noise Ratio & distortion, -0.5dB				
DC to 100 KHz	-66	-70	–	FS-dB
100 KHz to 500 KHz	-66	-70	–	FS-dB
Effective Bits, -0.5dB				
DC to 100 KHz	11.0	11.25	–	Bits
100 KHz to 500 KHz	10.6	11.0	–	Bits
Two-Tone Intermodulation Distortion (*f*IN=75, 105 KHz				
Fs=1 MHz, -7dB	-80	-88	–	FS-dB
Two-Tone Intermodulation Dist. (*f*IN=480 KHz, 490				
KHz, Fs=1 MHz, (-0.5dB)	-65	-68	–	FS-dB
Input Bandwidth				
Small Signal (-20dB)	7.5	10	–	MHz
Full Power (0dB)	5	8	–	MHz
Slew Rate	–	150	–	V/µSec.
Aperture Delay Time	–	–	20	nSec.
Effect. Aperture Delay Time	–	–	16	nSec.
Aperture Uncertainty (Jitter)				
(rms)	–	–	±15	pSec.
(peak)	–	–	±50	pSec.
S/H Acquisition Time to 0.01% (Transient Recovery)	–	–	180	nSec.
Overvoltage Recovery Time	–	–	1000	nSec.
POWER REQUIREMENTS				
Power Supply Range				
+15V dc Supply	+14.25	+15.0	+15.75	Volts dc
-15V dc Supply	-14.25	-15.0	-15.75	Volts dc
+5V dc Supply	+4.75	+5.0	+5.25	Volts dc
Power Supply Current				
+15V dc Supply	–	+24	+35	mA
-15V dc Supply	–	-40	-48	mA
+5V dc Supply ①	–	+95	+115	mA
Power Dissipation	–	1.3	1.7	Watts
Power Supply Rejection	–	–	0.05	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range				
-MC	0	–	+70	° C
-MM	-55	–	+125	° C
Storage Temperature Range	-65	–	+150	° C
Package Type	40-pin hermetic sealed, ceramic DIP			
Weight	0.56 ounces (16 grams), maximum			

① +5V power usage at 1 TTL logic loading per data output bit.

Specifications subject to change without notice.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

TECHNICAL NOTES

1. Use external potentiometers as shown in Figure 3 to adjust the offset and gain errors to zero. For operation without adjustment, leave pin 8 open.

2. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital grounds are connected internally. Avoid ground-related problems by connecting the digital analog grounds to one point, the ground plane beneath the converter.

   Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

3. Bypass the analog and digital supplies to ground with a 10 µF, 25V tantalum electrolytic capacitor. Bypass the +10V reference (pin 2 and 31) to analog ground (pin 16) with a 0.1 µF ceramic capacitor.

4. For unipolar, 0 to -5V FSR, connect pins 31 and 32. For bipolar, ±2.5V FSR, connect pin 32 to analog ground and connect pin 31 to a 0.1 µF ceramic capacitor only.

5. Pins 27 and 28 are no connection pins. Connecting pins 27 and 28 together is acceptable.

TIMING

Figure 2 shows the relationship between the various input signals. The timing shown applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3 for the appropriate full-scale range (FSR). Apply a pulse of 200 nanoseconds minimum to the START CONVERT input (pin 20) at a rate of 250 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments
   Apply a precision voltage reference source between the amplifier's analog input and ground. Adjust the output of the reference source per Table 2. Adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 for unipolar.

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001.

3. Full-Scale Adjustment
   Set the output of the voltage reference used in step 2 to the value shown in Table 2. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 3.

Table 2. Zero and Gain Adjust

FSR	ZERO ADJUST + 1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to -5V dc	-0.61mV dc	-4.9982V
±2.5V dc	+0.61 mV	-2.4982V

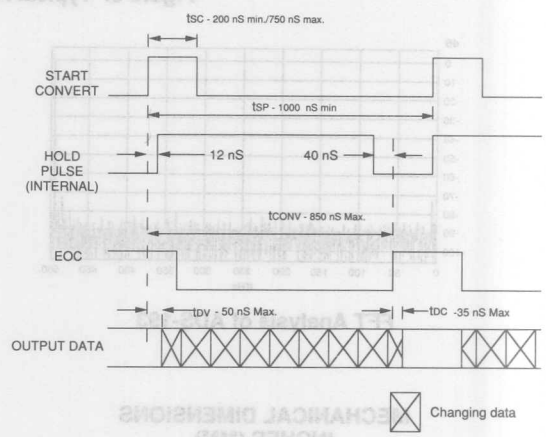


Figure 2. ADS-193 Timing Diagram

Table 3. Output Coding

		COMP. BINARY		
UNIPOLAR	INPUT RANGE, V dc	OUTPUT CODING	INPUT RANGE	BIPOLAR
SCALE	0 to -5V	MSB LSB	±2.5V dc	SCALE
+FS -1 LSB	-4.998V	1111 1111 1111	-2.4988V	+FS -1 LSB
7/8 FS	-4.375V	1110 0000 0000	-1.8750V	+3/4 FS
3/4 FS	-3.750V	1100 0000 0000	-1.2500V	+1/2 FS
1/2 FS	-2.500V	1000 0000 0000	0.0000V	0
1/4 FS	-1.250V	0100 0000 0000	+1.2500V	-1/2 FS
1/8 FS	-0.625V	0010 0000 0000	+1.8750V	-3/4 FS
1 LSB	-0.0012V	0000 0000 0001	+2.4988V	-FS +1 LSB
0	0.000V	0000 0000 0000	+2.5000V	-FS
		COMP. OFF. BIN.		

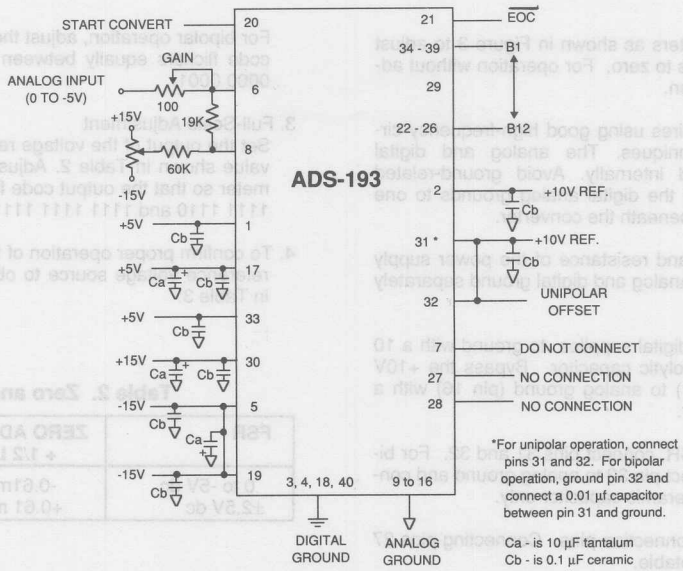
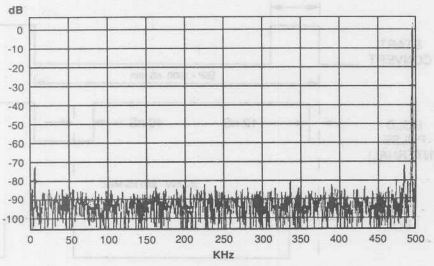
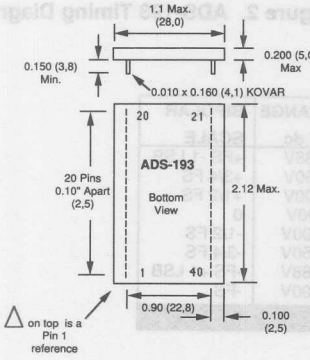


Figure 3. Typical ADS-193 Connection Diagram



FFT Analysis of ADS-193

MECHANICAL DIMENSIONS INCHES (MM)



ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	SEAL
ADS-193MC	0 °C to +70 °C	Hermetic
ADS-193MM	-55 °C to +125 °C	Hermetic
ADS-EVAL1	Evolution Board (without ADS-193)	

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 40 required.

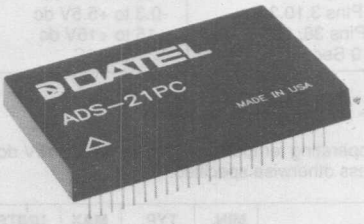
For availability of MIL-STD-883 versions, contact DATEL.

ADS-21PC

Low-Power, 12-Bit, 1.3 MHz Sampling A/D Converter

FEATURES

- **12-Bit resolution**
- **1.3 MHz throughput rate**
- **S/H included**
- **Single 46-pin DIP**



GENERAL DESCRIPTION

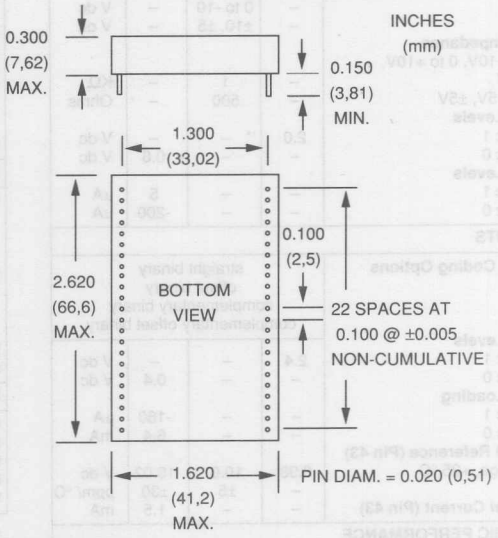
DATEL's ADS-21PC Sampling Converter combines a 12-bit A/D and a S/H in one space-saving package. Designed and manufactured at DATEL's modern, certified hybrid assembly facility using state-of-the-art integrated circuits, the ADS-21PC provides the highest quality and performance for signal processing applications.

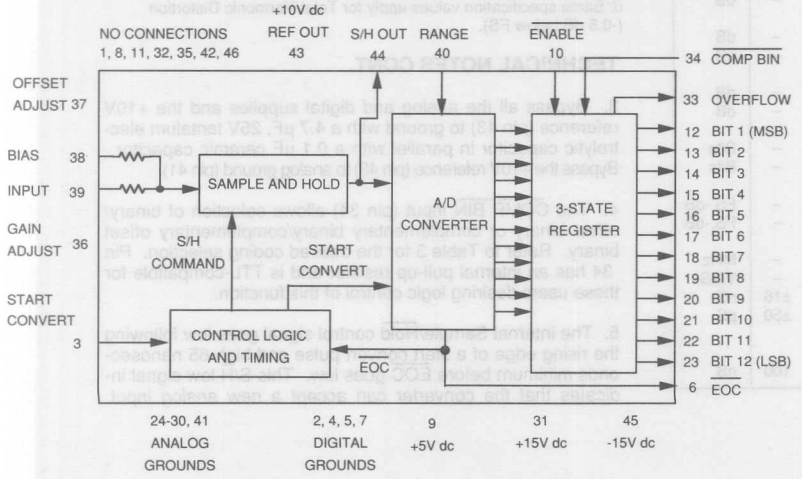
TECHNICAL NOTES

1. Use external potentiometers to remove system errors or the small initial errors to zero. Use a 20K trimming potentiometer for gain adjustment with the wiper tied to pin 36 (ground pin 36 for operation without adjustments). Use a 20K trimming potentiometer with the wiper tied to pin 37 for zero/offset adjustment (leave pin 37 open for operation without adjustment).

2. Rated performance requires using good high frequency circuit board layout techniques. The analog and digital grounds are connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies. This prevents contamination of the analog ground by noisy digital ground currents.

MECHANICAL DIMENSIONS





INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	N/C	24	ANA GND
2	DIG GND	25	ANA GND
3	START CONVERT	26	ANA GND
4	DIG GND	27	ANA GND
5	DIG GND	28	ANA GND
6	EOC	29	ANA GND
7	DIG GND	30	ANA GND
8	N/C	31	+15V
9	+5V	32	N/C
10	ENABLE	33	OVERFLOW
11	N/C	34	COMP BIN
12	BIT 1 (MSB)	35	N/C
13	BIT 2	36	GAIN ADJUST
14	BIT 3	37	OFFSET ADJUST
15	BIT 4	38	BIAS
16	BIT 5	39	ANALOG INPUT
17	BIT 6	40	RANGE
18	BIT 7	41	ANA GND
19	BIT 8	42	N/C
20	BIT 9	43	+10V REF OUT
21	BIT 10	44	S/H OUT
22	BIT 11	45	-15V
23	BIT 12 (LSB)	46	N/C

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS
+15V Supply (Pin 31)	-0.3 to +18V dc
-15V Supply (Pin 45)	+0.3 to -18V dc
+5V Supply (Pin 9)	-0.5 to +7V dc
Digital Inputs (Pins 3,10,34)	-0.3 to +5.5V dc
Analog Input (Pins 38, 39)	-15 to +15V dc
Lead Temp. (10 Sec.)	300 °C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and +5V dc unless otherwise specified.

INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Ranges	–	0 to +10	–	V dc
	–	0 to -5V	–	V dc
	–	0 to -10	–	V dc
	–	±10, ±5	–	V dc
Input Impedance				
0 to -10V, 0 to +10V, ±10V	–	1	–	KΩ
0 to -5V, ±5V	–	500	–	Ohms
Logic Levels				
Logic 1	2.0	–	–	V dc
Logic 0	–	–	0.8	V dc
Logic Levels				
Logic 1	–	–	5	µA
Logic 0	–	–	-200	µA
OUTPUTS				
Output Coding Options	straight binary offset binary complementary binary complementary offset binary			
Logic Levels				
Logic 1	2.4	–	–	V dc
Logic 0	–	–	0.4	V dc
Logic Loading				
Logic 1	–	–	-160	µA
Logic 0	–	–	6.4	mA
Internal Reference (Pin 43)				
Voltage, +25 °C	9.98	10.0	10.02	V dc
Drift	–	±5	±30	ppm/ °C
External Current (Pin 43)	–	–	1.5	mA
DYNAMIC PERFORMANCE				
Feedthrough Rejection	–	-74	–	dB
SNR w/o distortion, -0.5 dB				
dc to 100 kHz	-69.0	-71	–	dB
100 KHz to 500 KHz	-67	-70	–	dB
SNR with distortion, -0.5 dB				
dc to 100 kHz	-68.0	-71	–	dB
100 KHz to 500 KHz	-66	-70	–	dB
Effective Bits				
dc to 100 kHz	11	11.5	–	Bits
100 KHz to 500 KHz	10.7	11.3	–	Bits
Inband Harmonics ①				
dc to 100 KHz	-72	-80	–	FS -dB
100 to 500 KHz	-70	-75	–	FS,-dB
Frequency Response				
Small Signal (-3 dB)	–	16	–	MHz
Slew Rate	–	300	–	V/µS
Aperture Delay Time	–	–	±16	nS
Aperture Uncertainty (Jitter)	–	–	±50	pS
Settling Time				
10V to ±0.01% FS (±1mV)	–	60	100	nS

DYNAMIC PERFORM. CONT.	MIN	TYP	MAX	UNITS
Acquisition Time				
10V step to ±1.0 mV (0.01% FS)				
+25 °C	–	145	180	nS
0 to +70 °C	–	165	220	nS
PERFORMANCE, ±10V RANGE				
Integral Nonlinearity				
0 to +70 °C	–	–	±0.0125	%FSR±1/2LSB
Differential Nonlinearity				
0 to +70 °C	–	–	±0.0125	%FSR±1/2LSB
FS Absol. Accuracy				
+25 °C	–	±5	±12	LSB
0 to +70 °C	–	±6	±15	LSB
Unipolar Zero Error				
+25 °C	–	±2	±5	LSB
Unipolar Zero Tempco	–	±13	±25	ppm/ °C
Bipolar Zero Error	–	–	±5	LSB
Bipolar Zero Tempco	–	±13	±25	ppm/ °C
Bipolar Offset Error				
+25 °C	–	±2	±8	LSB
Bipolar Offset Tempco	–	±17	±40	ppm/ °C
Gain Error, +25 °C	–	±3	±8	LSB
Gain Tempco	–	±18	±40	ppm/ °C
Throughput Rate				
+25 °C	1.3	–	–	MHz
0 to +70 °C	1.1	–	–	MHz
No Missing Codes (12 bits)	Over the operating temp. range.			
POWER SUPPLY REQUIREMENTS				
Power Supply Range				
+15V dc Supply	+14.25	+15	+15.75	V dc
-15V dc Supply	-14.25	-15	-15.75	V dc
+5V dc Supply	+4.75	+5	+5.25	V dc
Power Supply Current				
+15V Supply	–	+50	+65	mA
-15V Supply	–	-65	-72	mA
+5V Supply*	–	+80	+95	mA
Power Dissipation	–	2.1	2.5	Watts
Power Supply Rejection	–	0.01	0.05	%FSR/%V
PHYSICAL-ENVIRONMENTAL				
Operating Temp. Range	0	–	+70	°C
Storage Temp. Range	-65	–	+125	°C
Package Type	46-pin DIP			
Pins	0.010 x 0.018 copper alloy			
Weight	1.25 Oz. (35 g) max.			

*+5V power usage at 1 TTL logic loading per data output bit.

① Same specification values apply for Total Harmonic Distortion (-0.5 dB below FS).

TECHNICAL NOTES CONT.

3. Bypass all the analog and digital supplies and the +10V reference (pin 43) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 43) to analog ground (pin 41).

4. The $\overline{\text{COMP BIN}}$ input (pin 34) allows selection of binary/offset binary or complementary binary/complementary offset binary. Refer to Table 3 for the desired coding selection. Pin 34 has an internal pull-up resistor and is TTL-compatible for those users desiring logic control of this function.

5. The internal Sample/$\overline{\text{Hold}}$ control signal goes low following the rising edge of a start convert pulse and high 65 nanoseconds minimum before $\overline{\text{EOC}}$ goes low. This S/H low signal indicates that the converter can accept a new analog input.

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Table 1. Input Connections

Input Voltage Range	Connect Input Pin 38 to	Connect Pin 40 (Range) to
0 to -5V	39	44
0 to -10V	–	44
0 to +10V	Ext. -10V Ref.*	44
±5V	39	43
±10V	–	43

*May be referenced to +10V Ref. (Pin 43)

Table 2. Zero and Gain Adjust

FSR	Zero Adjust +1/2 LSB	Gain Adjust +FS - 1 1/2 LSB
0 to -5V	-0.61 mV	-4.9982V
0 to -10V	-1.22 mV	-9.9963V
0 to +10V	+1.22 mV	+9.9963V
±10V dc	+2.44 mV	+9.9927V dc
±5V dc	+1.22 mV	+4.9963V dc

CALIBRATION PROCEDURE

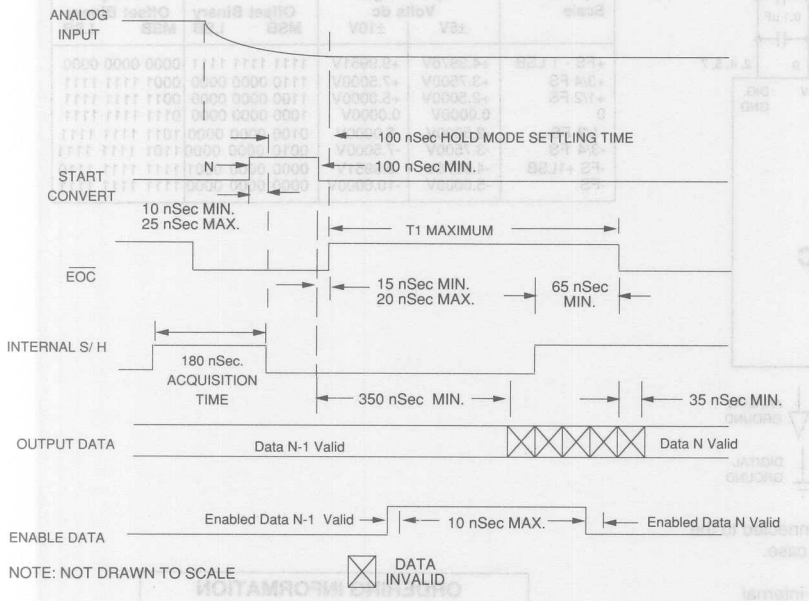
1. Connect the converter per Figure 3 and Tables 1 and 3 for the appropriate full-scale range (FSR) and coding options. Apply a pulse of 100 nanoseconds minimum to the START CONVERT input (pin 3) at a rate of 500 KHz. This rate chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustment
Apply a precision voltage reference source between the analog input (pin 39) and ground (pin 24). Adjust the output of the reference source per Table 2. For Unipolar operation adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 or between 1111 1111 1111 and 1111 1111 1110. Refer to Table 4.

For bipolar operation, adjust the potentiometer until the displayed code flickers equally between 1000 0000 0000 and 1000 0000 0001 or between 0111 1111 1111 and 0111 1111 1110. Refer to Table 5.

3. Full-Scale Adjustment
Set the output of the voltage reference used in step 2 to the value shown in Table 2. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 or between 0000 0000 0001 and 0000 0000 0000 depending on the output coding selected.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Tables 4 and 5.



T1 Values

	Temperature +25 °C	Temperature 0 to +70 °C
Conversion Time	530 nSec.	590 nSec.

NOTE: Timing cited is guaranteed by design and applies over the operating temperature and power supply ranges.

Table 3. Input Range/Output Selection

Input Voltage Range	Binary/ Offset Binary Connect Pin 34 to	Comp. Binary/ Comp.Offset Binary Connect Pin 34 to
0 to -5V	–	2,4,5,7
0 to -10V	–	2,4,5,7
0 to +10V	2,4,5,7	–
±5V	2,4,5,7	–
±10V	2,4,5,7	–

Table 4. Output Coding for Unipolar Operation

Unipolar Scale	Input Ranges Volts dc			Output Coding Straight Binary		Comp. Binary	
	0 to -5V	0 to -10V	0 to +10V	MSB	LSB	MSB	LSB
+FS - 1LSB	-4.998V	-9.9976V	+9.9976V	1111	1111 1111	0000	0000 0000
7/8 FS	-4.375V	-8.750V	+8.750V	1110	0000 0000	0001	1111 1111
3/4 FS	-3.750V	-7.500V	+7.500V	1100	0000 0000	0011	1111 1111
1/2 FS	-2.500V	-5.00V	+5.00V	1000	0000 0000	0111	1111 1111
1/4 FS	-1.250V	-2.500V	+2.500V	0100	0000 0000	1011	1111 1111
1/8 FS	-0.625V	-1.250V	+1.250V	0010	0000 0000	1101	1111 1111
1 LSB	-0.0012V	-0.0024V	+0.0024V	0000	0000 0001	1111	1111 1110
0	0.0000V	0.0000V	0.0000V	0000	0000 0000	1111	1111 1111

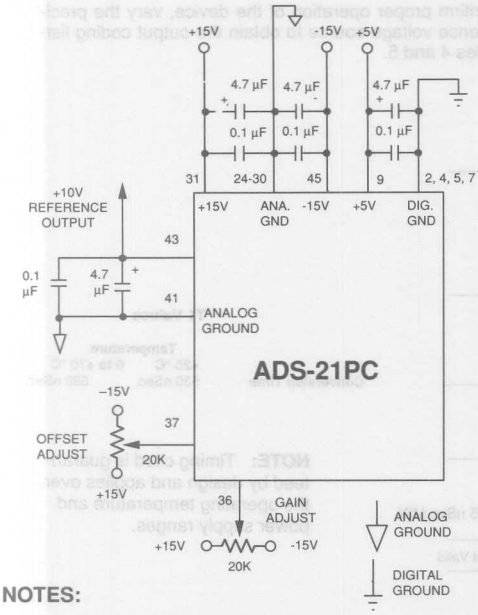


Table 5. Output Coding for Bipolar Operation

Bipolar Scale	Input Ranges Volts dc		Output Coding Offset Binary		Comp. Offset Binary	
	±5V	±10V	MSB	LSB	MSB	LSB
+FS - 1 LSB	+4.9976V	+9.9951V	1111	1111 1111	0000	0000 0000
+3/4 FS	+3.7500V	+7.5000V	1110	0000 0000	0001	1111 1111
+1/2 FS	+2.5000V	+5.0000V	1100	0000 0000	0011	1111 1111
0	0.0000V	0.0000V	1000	0000 0000	0111	1111 1111
-1/2 FS	-2.5000V	-5.0000V	0100	0000 0000	1011	1111 1111
-3/4 FS	-3.7500V	-7.5000V	0010	0000 0000	1101	1111 1111
-FS +1LSB	-4.9976V	-9.9951V	0000	0000 0001	1111	1111 1110
-FS	-5.0000V	-10.0000V	0000	0000 0000	1111	1111 1111

NOTES:

1. Pins 2, 4, 5, 7, 24-30, and 41 must be connected to the ground plane as close as possible to the case.
2. Pins 1, 8, 11, 32, 35, 42, and 46 have no internal connections.

Figure 3.
Typical ADS-21PC Connections

ORDERING INFORMATION	
MODEL NO.	TEMP. RANGE
ADS-21PC	0 to +70 °C

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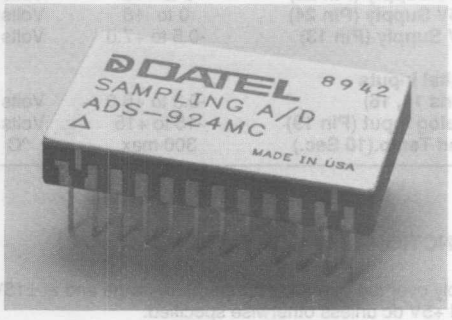
ADS-924

14-Bit, 300 KHz, Low-Power Sampling A/D Converter

FEATURES

- **14-Bit resolution**
- **Internal Sample/Hold**
- **300 KHz minimum throughput**
- **Functionally complete**
- **Small 24-pin DIP**
- **Low-power, 1.4 Watts**
- **Three-state output buffers**

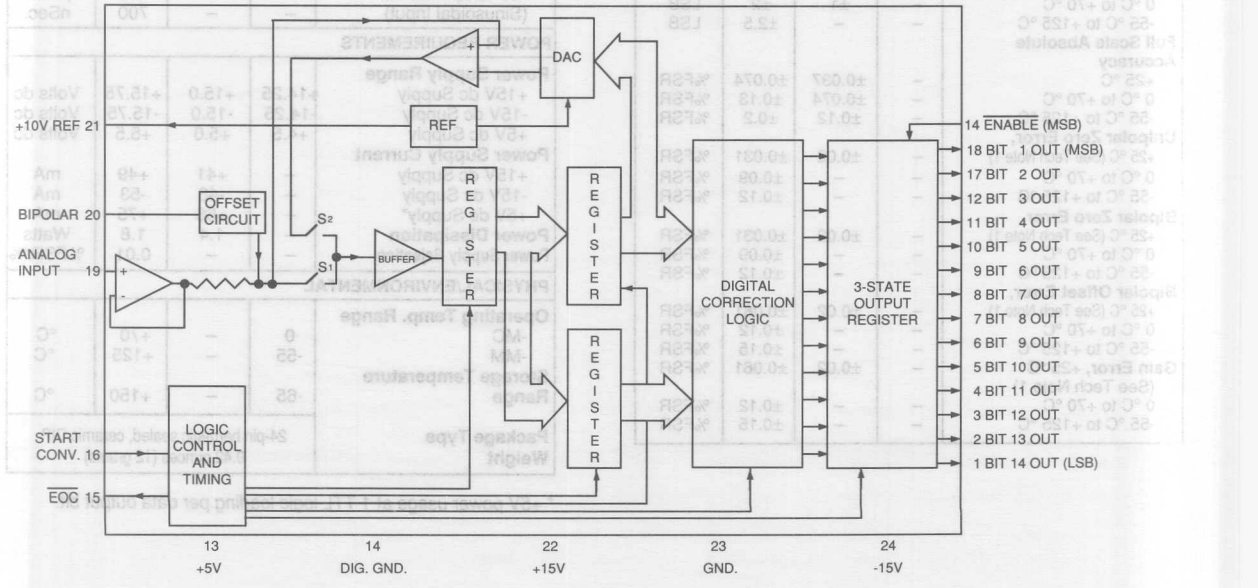


GENERAL DESCRIPTION

DATEL's ADS-924 is a 14-bit, functionally complete, sampling A/D converter that is packaged in a space-saving 24-pin ceramic DIP. A minimum throughput rate of 300 KHz is achieved while only dissipating 1.4 Watts.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 14 OUT (LSB)	13	+5V
2	BIT 13 OUT	14	$\overline{\text{ENABLE}}$
3	BIT 12 OUT	15	$\overline{\text{EOC}}$
4	BIT 11 OUT	16	START CONVERT
5	BIT 10 OUT	17	BIT 2 OUT
6	BIT 9 OUT	18	BIT 1 (MSB)
7	BIT 8 OUT	19	ANALOG INPUT
8	BIT 7 OUT	20	BIPOLAR
9	BIT 6 OUT	21	+10V REF
10	BIT 5 OUT	22	+15V
11	BIT 4 OUT	23	GROUND
12	BIT 3 OUT	24	-15V



PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 22)	0 to +18	Volts dc
-15V Supply (Pin 24)	0 to -18	Volts dc
+5V Supply (Pin 13)	-0.5 to +7.0	Volts dc
Digital Inputs (Pins 14, 16)	-0.3 to +6.0	Volts dc
Analog Input (Pin 19)	-15 to +15	Volts dc
Lead Temp.(10 Sec.)	300 max	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and +5V dc unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range				
ADS-924	–	±5	–	Volts dc
(See Table 4 also)	–	0 to +10	–	Volts dc
Input Impedance	5.0	15.0	–	M Ohms
Input Capacitance	–	3	5	pf
DIGITAL INPUTS				
Logic Levels				
Logic "1"	2.0	–	–	Volts dc
Logic "0"	–	–	0.8	Volts dc
Logic Loading "1"	–	–	5	µA
Logic Loading "0"	–	–	-200	µA
PERFORMANCE				
Integral Non-Linearity				
+25 °C (see Tech Notes)	–	±1/2	±1	LSB
0 °C to +70 °C	–	±1	±2	LSB
-55 °C to +125 °C	–	–	±3	LSB
Differential Non-Linearity				
+25 °C	–	±1/2	±1	LSB
0 °C to +70 °C	–	±1	±2	LSB
-55 °C to +125 °C	–	–	±2.5	LSB
Full Scale Absolute Accuracy				
+25 °C	–	±0.037	±0.074	%FSR
0 °C to +70 °C	–	±0.074	±0.13	%FSR
-55 °C to +125 °C	–	±0.12	±0.2	%FSR
Unipolar Zero Error,				
+25 °C (See Tech Note 1)	–	±0.02	±0.031	%FSR
0 °C to +70 °C	–	–	±0.09	%FSR
-55 °C to +125 °C	–	–	±0.12	%FSR
Bipolar Zero Error,				
+25 °C (See Tech Note 1)	–	±0.02	±0.031	%FSR
0 °C to +70 °C	–	–	±0.09	%FSR
-55 °C to +125 °C	–	–	±0.12	%FSR
Bipolar Offset Error,				
+25 °C (See Tech Note 1)	–	±0.02	±0.061	%FSR
0 °C to +70 °C	–	–	±0.12	%FSR
-55 °C to +125 °C	–	–	±0.15	%FSR
Gain Error, +25 °C (See Tech Note 1)	–	±0.02	±0.061	%FSR
0 °C to +70 °C	–	–	±0.12	%FSR
-55 °C to +125 °C	–	–	±0.15	%FSR

OUTPUTS	MIN.	TYP.	MAX.	UNITS
No Missing Codes				
(14 Bits)		at +25 °C		
(13 Bits)		over 0 to 70 °C temp. range		
(12 Bits)		over -55 to +125 °C temp. range		
Logic Levels				
Logic "1"	2.4	–	–	Volts dc
Logic "0"	–	–	0.4	Volts dc
Logic Loading "1"	–	–	-160	µA
Logic Loading "0"	–	–	6.4	mA
Internal Reference Voltage, +25 °C	+9.98	+10.0	+10.02	Volts dc
Drift	–	±5	±30	ppm/ °C
External Current	–	–	1.5	mA
Resolution		14 Bits		
Output Coding		Straight binary/offset binary		
DYNAMIC PERFORMANCE				
Conversion Time				
+25 °C	300	–	–	KHz
0 °C to +70 °C	300	–	–	KHz
-55 °C to +125 °C	300	–	–	KHz
Total Harmonic Distortion				
DC to 100 KHz at Vin<2.5V p-p				
+25 °C	-72	-76	–	dB
-55 °C to +125 °C	-70	-72	–	dB
DC to 40 KHz at Vin = 10V p-p				
+25 °C	-72	-76	–	dB
-55 °C to +125 °C	-70	-72	–	dB
Slew Rate	–	90	–	V/µSec.
Aperture Delay Time	–	20	–	nSec.
Aperture Uncertainty	–	±100	–	pSec.
S/H Acquisition Time to 0.006% (10V step)				
+25 °C	–	–	1.2	µSec.
0 °C to +70 °C	–	–	1.35	µSec.
-55 °C to +125 °C	–	–	1.5	µSec.
(Sinusoidal Input)	–	–	700	nSec.
POWER REQUIREMENTS				
Power Supply Range				
+15V dc Supply	+14.25	+15.0	+15.75	Volts dc
-15V dc Supply	-14.25	-15.0	-15.75	Volts dc
+5V dc Supply	+4.5	+5.0	+5.5	Volts dc
Power Supply Current				
+15V dc Supply	–	+41	+49	mA
-15V dc Supply	–	-46	-53	mA
+5V dc Supply*	–	+66	+75	mA
Power Dissipation	–	1.4	1.8	Watts
Power Supply Rejection	–	–	0.01	%FSR/%
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range				
-MC	0	–	+70	°C
-MM	-55	–	+125	°C
Storage Temperature Range	-65	–	+150	°C
Package Type		24-pin hermetic sealed, ceramic DIP		
Weight		0.42 ounces (12 grams)		

* +5V power usage at 1 TTL logic loading per data output bit.

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1. Applications which are unaffected by endpoint errors or remove them through software will use the typical connections shown in Figure 3. Remove system errors or adjust the small initial errors of the ADS-924 to zero using the optional external circuitry shown in Figure 4. The external adjustment circuit has no affect on the throughput rate.

2. Bypass the analog and digital supplies and the +10V reference (pin 21) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 21) to analog ground (pin 23).

3. The ADS-924 exhibits up to 2.0 LSB's of peak-to-peak noise. Digital signal processing (DSP) applications will average this noise.

4. To obtain three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 14) to a logic "0" (low). Otherwise, connect $\overline{\text{ENABLE}}$ (pin 14) to a logic "1" (high).

TIMING

Figure 2 shows the relationship between the various input signals. The timing shown applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

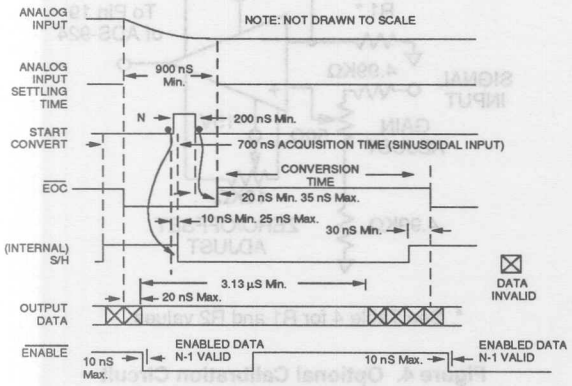


Figure 2. ADS-924 Timing Diagram

Table 2. Input Range Selection

INPUT RANGE	INPUT PIN	TIE TOGETHER
±5V dc	Pin 19	Pin 20 to Pin 21
0 to +10V dc	Pin 19	Pin 20 to Ground

Table 3. Zero and Gain Adjust

FSR	ZERO ADJUST +1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to +10V dc	+300µV dc	+9.9991V dc
±5V dc	+300µV dc	+4.9991V dc

(using external calibration)

INPUT RANGE	R1	R2	UNIT
0 to +10V, ±5V	2	2	K Ohms
0 to +5V, ±2.5V	1.65	4.99	K Ohms
0 to +2.5V, ±1.25V	715	4990	K Ohms

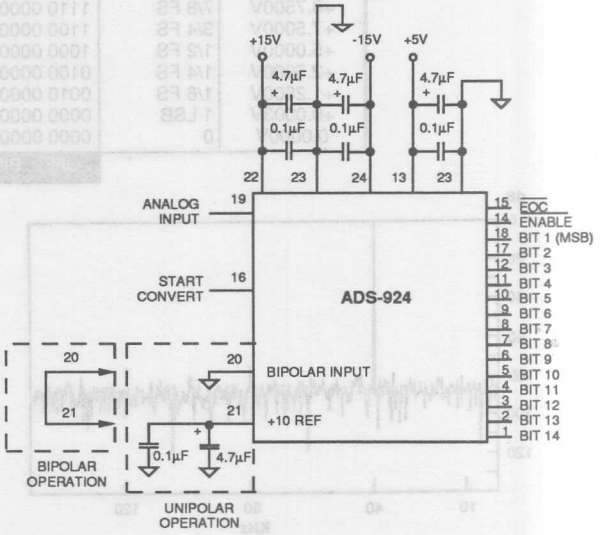


Figure 3. Typical Input Connections for the ADS-924

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3, Figure 4, and Table 2 for the appropriate full-scale range (FSR). Apply a pulse of 200 nanoseconds minimum to the START CONVERT input (pin 16) at a rate of 250 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments
   Apply a precision voltage reference source between the amplifier's analog input and ground. Adjust the output of the reference source per Table 3. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 00 0000 0000 0000 and 00 0000 0000 0001.

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 10 0000 0000 0000 and 10 0000 0000 0001.

3. Full-Scale Adjustment
   Set the output of the voltage reference used in step 2 to the value shown in Table 3. Adjust the gain trimming potentiometer so that the output code flickers equally between 11 1111 1111 1110 and 11 1111 1111 1111.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 5.

Table 6. Output Coding

		STRAIGHT BIN. COMP. BINARY			
INPUT RANGE	UNIPOLAR	OUTPUT CODING		BIPOLAR	INPUT
0 to +10V	SCALE	MSB LSB	MSB LSB	SCALE	RANGES
+9.99939V	+FS -1 LSB	1111 1111 1111	0000 0000 0000	+FS -1 LSB	+4.99939V
+8.7500V	7/8 FS	1110 0000 0000	0001 1111 1111	+3/4 FS	+3.7500V
+7.5000V	3/4 FS	1100 0000 0000	0011 1111 1111	+1/2 FS	+2.5000V
+5.0000V	1/2 FS	1000 0000 0000	0111 1111 1111	0	0.0000V
+2.5000V	1/4 FS	0100 0000 0000	1011 1111 1111	-1/2 FS	-2.5000V
+1.2500V	1/8 FS	0010 0000 0000	1101 1111 1111	-3/4 FS	-3.7500V
+0.0003V	1 LSB	0000 0000 0001	1111 1111 1110	-FS + 1 LSB	-4.99939V
0.0000V	0	0000 0000 0000	1111 1111 1111	-FS	-5.0000V
		OFF. BINARY COMP. OFF. BIN.			

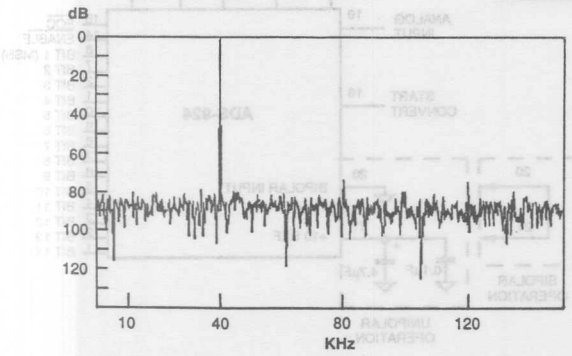
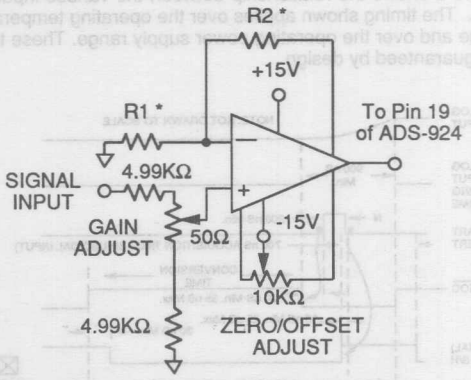


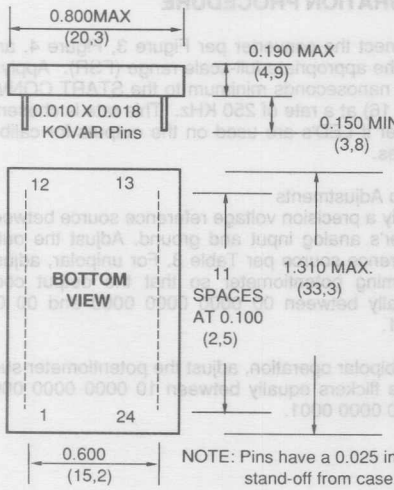
Figure 5. FFT Analysis of ADS-924



* See Table 4 for R1 and R2 values.

Figure 4. Optional Calibration Circuit

MECHANICAL DIMENSIONS
INCHES (MM)



NOTE: Pins have a 0.025 inch, ±0.01 stand-off from case.

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	SEAL
ADS-924MC	0 °C to +70 °C	Hermetic
ADS-924MM	-55 °C to +125 °C	Hermetic

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required.

For availability of MIL-STD-883B versions, contact DATEL.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

ADS-928
High Resolution Sampling A/D Converter

FEATURES

- **14-Bit resolution**
- **500 KHz sampling rate**
- **Functionally complete**
- **Small 32-pin DIP**
- **Low-power, 3.1 Watts**
- **Three-state output buffers**
- **Samples up to Nyquist**

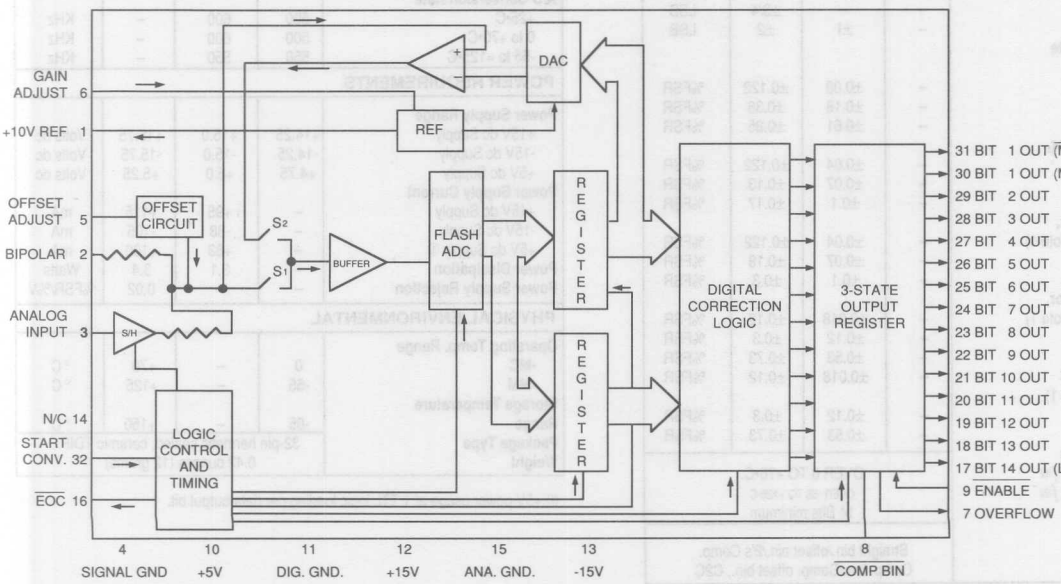
GENERAL DESCRIPTION

DATEL's ADS-928 is a 14-bit, 500 KHz sampling rate, functionally complete A/D converter. The ADS-928 samples up to Nyquist with no missing codes.

Packaged in a small 32-pin DIP, power requirements are ±15 volts and +5 volts with 3.1 Watts power dissipation.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+10V REF. OUT	17	BIT 14 OUT (LSB)
2	BIPOLAR	18	BIT 13 OUT
3	ANALOG INPUT	19	BIT 12 OUT
4	SIGNAL GROUND	20	BIT 11 OUT
5	OFFSET ADJUST	21	BIT 10 OUT
6	GAIN ADJUST	22	BIT 9 OUT
7	OVERFLOW	23	BIT 8 OUT
8	COMP. BIN	24	BIT 7 OUT
9	ENABLE	25	BIT 6 OUT
10	+5V	26	BIT 5 OUT
11	DIGITAL GROUND	27	BIT 4 OUT
12	+15V	28	BIT 3 OUT
13	-15V	29	BIT 2 OUT
14	NO CONNECTION	30	BIT 1 OUT (MSB)
15	ANALOG GROUND	31	BIT 1 OUT (MSB)
16	EOC	32	START CONVERT



ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 12)	-0.3 to +18	Volts dc
-15V Supply (Pin 13)	+0.3 to -18	Volts dc
+5V Supply (Pin 10)	-0.3 to +7.0	Volts dc
Digital Inputs (Pins 8, 9, 32)	-0.3 to +7.0	Volts dc
Analog Input (Pin 3)	±25	Volts
Lead Temp. (10 Sec.)	300 max	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and +5V dc unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range				
	–	0 to -10	–	Volts
	–	±5	–	Volts
Input Impedance	4.9	5	–	K Ohms
Input Capacitance	–	7	15	pf
DIGITAL INPUTS				
Logic Levels				
Logic "1"	2.0	–	–	Volts dc
Logic "0"	–	–	0.8	Volts dc
Logic Loading "1"	–	–	5.0	µA
Logic Loading "0"	–	–	-200	µA
PERFORMANCE				
Int. Non-Lin. @ f_{IN} = 250 KHz				
+25 °C	–	±1/2	±3/4	LSB
0 to +70 °C	–	±3/4	±1	LSB
-55 to +125 °C	–	±1	±2	LSB
Diff. Non-Lin. @ f_{IN} = 250 KHz				
+25 °C	–	–	±1/2	LSB
0 to +70 °C	–	–	±3/4	LSB
-55 to +125 °C	–	±1	±2	LSB
Full Scale Absolute Accuracy				
+25 °C.	–	±0.08	±0.122	%FSR
0 to +70 °C	–	±0.18	±0.36	%FSR
-55 to +125 °C	–	±0.61	±0.85	%FSR
Unipolar Zero Error,				
+25 °C	–	±0.04	±0.122	%FSR
0 to +70 °C	–	±0.07	±0.13	%FSR
-55 to +125 °C	–	±0.1	±0.17	%FSR
Bipolar Zero Error,				
+25 °C (Tech Note 1)	–	±0.04	±0.122	%FSR
0 to +70 °C	–	±0.07	±0.18	%FSR
-55 to +125 °C	–	±0.1	±0.3	%FSR
Bipolar Offset Error,				
+25 °C (Tech Note 1)	–	±0.018	±0.12	%FSR
0 to +70 °C	–	±0.12	±0.3	%FSR
-55 to +125 °C	–	±0.53	±0.73	%FSR
Gain Error, +25 °C (See Tech Note 1)	–	±0.018	±0.12	%FSR
0 to +70 °C	–	±0.12	±0.3	%FSR
-55 to +125 °C	–	±0.53	±0.73	%FSR
No Missing Codes	OVER 0 TO +70•C.			
14 Bits @ 250 KHz f_{IN}				
13 Bits @ 250 KHz f_{IN}	OVER -55 TO +125•C			
Resolution	14 Bits minimum			
Output Coding				
(Pin 8 Hi)	Straight bin./offset bin./2's Comp.			
(Pin 8 Low)	Comp. bin./Comp. offset bin., C2C			

OUTPUTS	MIN.	TYP.	MAX.	UNITS
Logic Levels				
Logic "1"	2.4	–	–	Volts dc
Logic "0"	–	–	0.4	Volts dc
Logic Loading "1"	–	–	-160	µA
Logic Loading "0"	–	–	6.4	mA
Internal Reference Voltage, +25 °C	+9.98	+10.0	+10.02	Volts dc
Drift	–	±13	±30	ppm/ °C
External Current	–	–	2	mA
DYNAMIC PERFORMANCE				
Total Harm. Distort. (-0.5 dB)				
DC to 100 KHz	-83	-88	–	FS - dB
100 KHz to 250 KHz	-78	-82	–	FS - dB
Signal-to-Noise Ratio (w/o distortion, -0.5 dB)				
DC to 100 KHz	-82	-88	–	FS - dB
100 KHz to 250 KHz	-78	-84	–	FS - dB
Signal-to-Noise Ratio & distortion, -0.5 dB				
DC to 100 KHz	-77	-80	–	FS - dB
100 KHz to 250 KHz	-72	-75	–	FS - dB
Effective Bits, -0.5 dB				
DC to 100 KHz	12.5	13.2	–	Bits
100 KHz to 250 KHz	12.0	12.3	–	Bits
Two-tone Intermodulation Distortion (f_{IN} = 100 KHz, 240 KHz, Fs=500 KHz, -0.5 dB)	-92	–	–	FS - dB
Input Bandwidth				
Small Signal (-20 dB input)	6	–	–	MHz
Full Power (0 dB input)	1.75	–	–	MHz
Feedthrough Rejection @ f_{IN} = 250 KHz	-90	–	–	dB
Slew Rate	80	90	–	V/µSec.
Aperture Delay Time	–	±20	±25	nSec.
Aperture Uncertainty	–	–	±100	pSec.
S/H Acquisition Time (to 0.01%FS (10V step)	–	680	750	nSec.
Overvoltage Recovery, ±12V	–	600	1000	nSec.
A/D Conversion Rate				
+25•C	500	600	–	KHz
0 to +70•C	500	600	–	KHz
-55 to =125•C	550	550	–	KHz
POWER REQUIREMENTS				
Power Supply Range				
+15V dc Supply	+14.25	+15.0	+15.75	Volts dc
-15V dc Supply	-14.25	-15.0	-15.75	Volts dc
+5V dc Supply	+4.75	+5.0	+5.25	Volts dc
Power Supply Current				
+15V dc Supply	–	+95	+115	mA
-15V dc Supply	–	-88	-105	mA
+5V dc Supply ①	–	+83	+100	mA
Power Dissipation	–	3.1	3.4	Watts
Power Supply Rejection	–	–	0.02	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range				
-MC	0	–	+70	°C
-MM	-55	–	+125	°C
Storage Temperature Range	-65	–	+150	°C
Package Type	32-pin hermetic sealed, ceramic TDIP			
Weight	0.42 ounces (12 grams)			

① +5V power usage at 1 TTL logic loading per data output bit.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

TECHNICAL NOTES

1. Use external potentiometers to remove system errors or the small initial errors to zero. Use a 20K trimming potentiometer for gain adjustment with the wiper tied to pin 6 (ground pin 6 for operation without adjustments). Use a 20K trimming potentiometer with the wiper tied to pin 5 for zero/offset adjustment (connect pin 5 to pin 15, analog ground for operation without adjustment).

2. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

3. Bypass the analog and digital supplies and the +10V reference (pin 1) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 1) to analog ground (pin 15).

4. Obtain straight binary/offset binary output coding by tying COMP BIN (pin 8) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie the COMP BIN pin to ground. The COMP BIN signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

5. To enable the three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 9) to a logic "0" (low). To disable, connect ENABLE (pin 9) to a logic "1" (high).

6. The 200 nSec. minimum START CONVERT pulse width assures the hold mode settling time requirements are met.

7. The specifications listed in Figure 2 (timing diagram) apply over the full operating temperature range unless otherwise specified.

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3, and Table 1 for the appropriate full-scale range (FSR). Apply a pulse of 200 nanoseconds minimum to the START CONVERT input (pin 32) at a rate of 200 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

Table 1. Input Connections

INPUT RANGE	INPUT PIN	TIE TOGETHER
0 to -10V	Pin 3	Pins 2 and 4
±5V	Pin 3	Pins 1 and 2

Table 2. Zero and Gain Adjust

FSR	ZERO ADJUST +1/2 LSB	GAIN ADJUST FS - 1/2 LSB
0 to -10V	-305 µV	-9.999085V
±5V	-305 µV	-4.999085V

2. Zero Adjustments
   Apply a precision voltage reference source between the analog input (pin 3) and signal ground (pin 4). Adjust the output of the reference source per Table 2.

   For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 00 0000 0000 0000 and 00 0000 0000 0001 with the COMP BIN (pin 8) tied high (straight binary) or between 11 1111 1111 1111 and 11 1111 1111 1110 with the COMP BIN (pin 8) tied low (complementary binary).

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 10 0000 0000 0000 and 10 0000 0000 0001 with COMP BIN (pin 8) tied high (offset binary) or between 01 1111 1111 1111 and 01 1111 1111 1110 with COMP BIN (pin 8) tied low (complementary offset binary).

   Two's complement coding requires use of the MSB (pin 31) with COMP BIN (pin 8) tied high, adjusting the potentiometer such that the code flickers between 00 0000 0000 0000 and 00 0000 0000 0001.

3. Full-Scale Adjustment
   Set the output of the voltage reference used in step 2 to the value shown in Table 2.

   Adjust the gain trimming potentiometer so that the output code flickers equally between 11 1111 1111 1110 and 11 1111 1111 1111 for COMP BIN (pin 8) tied high (straight binary) or between 00 0000 0000 0000 and 00 0000 0000 0001 for COMP BIN tied low (complementary binary).

   Two's complement coding requires use of the MSB (pin 31) with the COMP BIN (pin 8) tied high, adjusting the gain trimming potentiometer so that the output code flickers equally between 01 1111 1111 1110 and 01 1111 1111 1111.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 3.

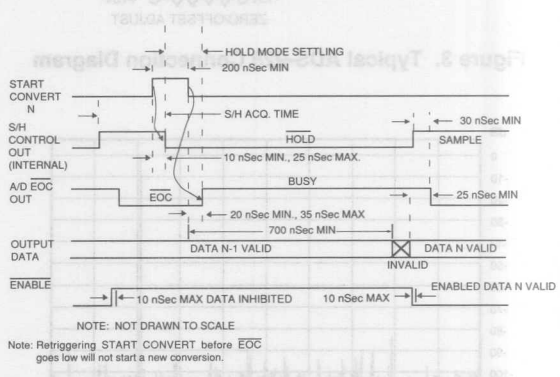


Figure 2. ADS-928 Timing Diagram

UNIPOLAR	INPUT RANGES, V dc	OUTPUT CODING						INPUT RANGE	BIPOLAR
SCALE	0 to -10V	MSB	LSB	MSB	LSB	MSB	LSB	±5V dc	SCALE
FS -1 LSB	-9.999390	11 1111 1111 1111		00 0000 0000 0000		01 1111 1111 1111		-4.99939	+FS -1 LSB
7/8 FS	-8.750000	11 1000 0000 0000		00 0111 1111 1111		01 1000 0000 0000		-3.75000	+3/4 FS
3/4 FS	-7.500000	11 0000 0000 0000		00 1111 1111 1111		01 0000 0000 0000		-2.50000	+1/2 FS
1/2 FS	-5.000000	10 0000 0000 0000		01 1111 1111 1111		00 0000 0000 0000		0.00000	0
1/4 FS	-2.500000	01 0000 0000 0000		10 1111 1111 1111		10 0000 0000 0000		+2.50000	-1/2 FS
1/8 FS	-1.250000	00 1000 0000 0000		11 0111 1111 1111		10 1000 0000 0000		+3.75000	-3/4 FS
1 LSB	-0.000610	00 0000 0000 0001		11 1111 1111 1110		10 0000 0000 0001		+4.99939	-FS +1 LSB
0	0.000000	00 0000 0000 0000		11 1111 1111 1111		10 00000000 0000		+5.00000	-FS
		OFF BINARY		COMP OFF. BIN.		TWO'S COMP.			

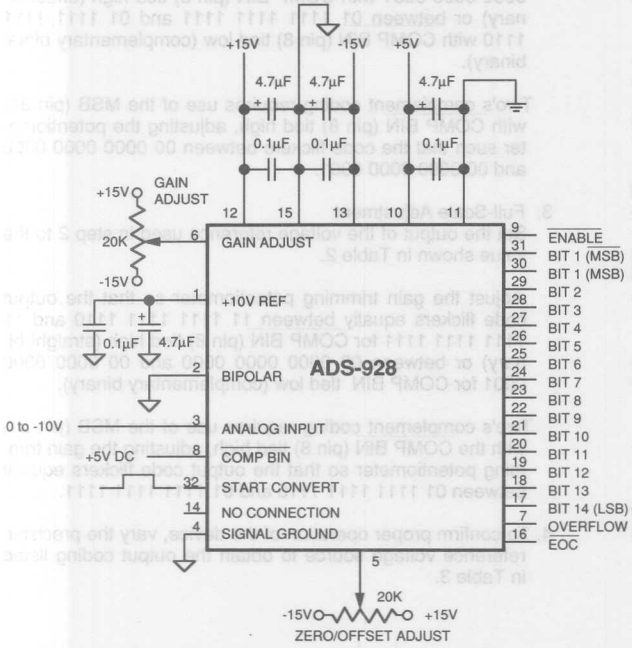


Figure 3. Typical ADS-928 Connection Diagram

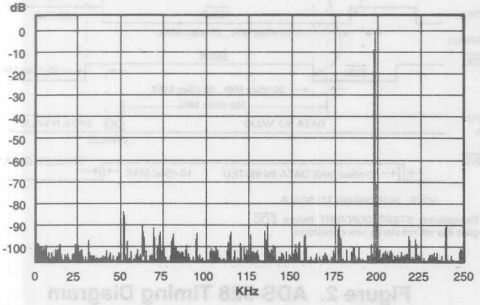
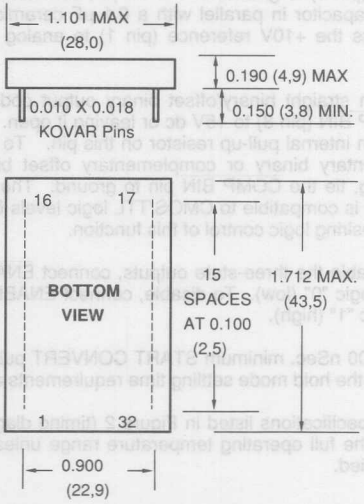


Figure 4. FFT Analysis of ADS-928

MECHANICAL DIMENSIONS INCHES (MM)



NOTE: Pins have a 0.025 inch, ±0.01 stand-off from case.

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	SEAL
ADS-928MC	0 °C to +70 °C	Hermetic
ADS-928MM	-55 °C to +125 °C	Hermetic
ADS-EVAL1	Evaluation Board (without ADS-928)	

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 32 required.

For availibility of MIL-STD-883B versions, contact DATEL.

DATEL

ADVANCED PRODUCT DATA

ADS-930

16-Bit, 500 KHz, High Resolution Sampling A/D Converter

FEATURES

- **16-Bit resolution**
- **500 KHz sampling rate**
- **Functionally complete**
- **Internal S/H**
- **Small 40-pin DIP**
- **Low-power, 2.1 Watts**
- **Three-state output buffers**
- **Samples up to Nyquist**
- **16 word FIFO memory**

GENERAL DESCRIPTION

DATEL's ADS-930 is a 16-bit, 500 KHz sampling rate, functionally complete A/D converter with internal FIFO. The ADS-930 samples up to Nyquist with no missing codes.

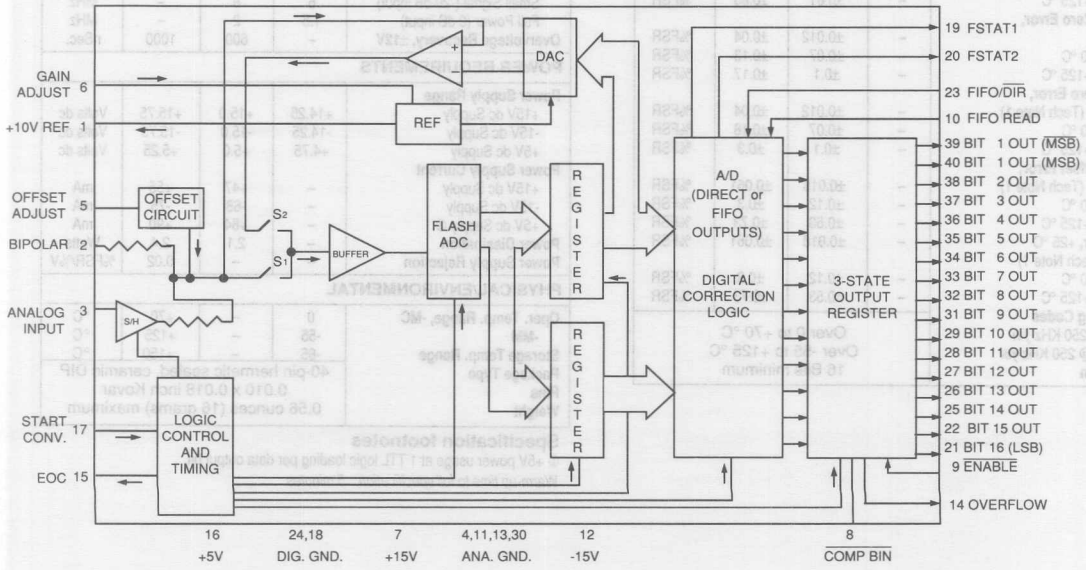
Packaged in a small 40-pin TDIP, power requirements are ±15 Volts and +5 Volts with 2.1 Watts power dissipation.

APPLICATIONS

- **Spectroscopy**
- **Spectrum analysis**
- **Imaging**
- **Radar**
- **Medical instrumentation**
- **High-speed data acquisition systems**

I/O CONNECTIONS

Pin	Function	Pin	Function
1	+10V REFERENCE	21	BIT 16 OUT (LSB)
2	BIPOLAR	22	BIT 15 OUT
3	ANALOG INPUT	23	FIFO/DIR
4	ANALOG GROUND	24	DIGITAL GROUND
5	OFFSET ADJUST	25	BIT 14 OUT
6	GAIN ADJUST	26	BIT 13 OUT
7	+15V	27	BIT 12 OUT
8	COMP BIN	28	BIT 11 OUT
9	ENABLE	29	BIT 10 OUT
10	FIFO READ	30	ANALOG GROUND
11	ANALOG GROUND	31	BIT 9 OUT
12	-15V	32	BIT 8 OUT
13	ANALOG GROUND	33	BIT 7 OUT
14	OVERFLOW	34	BIT 6 OUT
15	EOC	35	BIT 5 OUT
16	+5V	36	BIT 4 OUT
17	START CONVERT	37	BIT 3 OUT
18	DIGITAL GROUND	38	BIT 2 OUT
19	FSTAT1	39	BIT 1 OUT (MSB)
20	FSTAT 2	40	BIT 1 OUT (MSB)



ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply	-0.3 to +18	Volts dc
-15V Supply	+0.3 to -18	Volts dc
+5V Supply	-0.3 to +7.0	Volts dc
Digital Inputs	-0.3 to +7.0	Volts dc
Analog Input	±25	Volts
Lead Temp. (10 Sec.)	300 max	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and +5V dc unless otherwide specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range	–	0 to +10	–	Volts
	–	0 to -10	–	Volts
	–	±5, ±10	–	Volts
Input Impedance	1.9	2	–	K Ohms
Input Capacitance	–	7	15	pf
DIGITAL INPUTS				
Logic Levels				
Logic "1"	2.0	–	–	Volts dc
Logic "0"	–	–	0.8	Volts dc
Logic Loading "1"	–	–	2.5	µA
Logic Loading "0"	–	–	-100	µA
PERFORMANCE				
Int. Non-Lin. @ f_{IN} = 250 KHz				
+25 °C	–	±1	±1 1/2	LSB
0 to +70 °C	–	TBD	TBD	LSB
-55 to +125 °C	–	TBD	TBD	LSB
Diff. Non-Lin. @ f_{IN} = 250 KHz				
+25 °C	–	±1	±1 1/2	LSB
0 to +70 °C	–	TBD	TBD	LSB
-55 to +125 °C	–	TBD	TBD	LSB
Full Scale Absolute Accuracy				
+25 °C.	–	±0.04	±0.07	%FSR
0 to +70 °C	–	±0.18	±0.36	%FSR
-55 to +125 °C	–	±0.61	±0.85	%FSR
Unipolar Zero Error,				
+25 °C	–	±0.012	±0.04	%FSR
0 to +70 °C	–	±0.07	±0.13	%FSR
-55 to +125 °C	–	±0.1	±0.17	%FSR
Bipolar Zero Error,				
+25 °C (Tech Note 1)	–	±0.012	±0.04	%FSR
0 to +70 °C	–	±0.07	±0.18	%FSR
-55 to +125 °C	–	±0.1	±0.3	%FSR
Bipolar Offset Error,				
+25 °C (Tech Note 1)	–	±0.018	±0.061	%FSR
0 to +70 °C	–	±0.12	±0.3	%FSR
-55 to +125 °C	–	±0.53	±0.73	%FSR
Gain Error, +25 °C	–	±0.018	±0.061	%FSR
(See Tech Note 1)				
0 to +70 °C	–	±0.12	±0.3	%FSR
-55 to +125 °C	–	±0.53	±0.73	%FSR
No Missing Codes	Over 0 to +70 °C			
15 Bits @ 250 KHz f_{IN}	Over -55 to +125 °C			
TBD Bits @ 250 KHz f_{IN}				
Resolution	16 Bits minimum			

OUTPUTS	MIN.	TYP.	MAX.	UNITS
Output Coding	Straight bin./offset bin./2's Comp.			
(Pin Hi)	Comp. bin./Comp. offset bin.,C2C			
(Pin Low)				
Logic Levels				
Logic "1"	2.4	–	–	Volts dc
Logic "0"	–	–	0.4	Volts dc
Logic Loading "1"	–	–	-160	µA
Logic Loading "0"	–	–	6.4	mA
Internal Reference				
Voltage (+5V), +25 °C	+4.98	+5.0	+5.02	Volts dc
Drift	–	±25	±30	ppm/ °C
External Current	–	–	5	mA
Internal Reference				
Voltage (-10V), +25 °C	-9.98	-10.0	-10.02	Volts dc
Drift	–	±13	±30	ppm/ °C
External Current	–	–	-5	mA
DYNAMIC PERFORMANCE				
Total Harm. Distort. (-0.5 dB)				
DC to 100 KHz	-89	-95	–	FS - dB
100 KHz to 250 KHz	-83	-88	–	FS - dB
Signal-to-Noise Ratio				
(w/o distortion, -0.5 dB)				
DC to 100 KHz	-90	-95	–	FS - dB
100 KHz to 250 KHz	-87	-89	–	FS - dB
Signal-to-Noise Ratio				
& distortion, -0.5 dB				
DC to 100 KHz	-82	-87	–	FS - dB
100 KHz to 250 KHz	-78	-80	–	FS - dB
Effective Bits, -0.5 dB				
DC to 100 KHz	14	14.5	–	Bits
100 KHz to 250 KHz	13	13.5	–	Bits
Two-tone Intermodulation				
Distort. (f_{IN} = 100 KHz, 240 KHz,				
Fs=500 KHz, -0.5 dB)	TBD	–	–	FS - dB
Slew Rate	90	100	–	V/µSec.
Aperture Delay Time	–	–	±10	nSec.
Aperture Uncertainty	–	–	±100	pSec.
S/H Acquisition Time				
(to 0.01%FS (10V step)	–	480	600	nSec.
Feedthrough Rejection				
@ f_{IN} = 250 KHz	-96	–	–	dB
A/D Conversion Rate				
+25 °C	500	–	–	KHz
0 to +70 °C	500	–	–	KHz
-55 to +125 °C	500	–	–	KHz
Input Bandwidth				
Small Signal (-20 dB input)	6	8	–	MHz
Full Power (0 dB input)	1.5	2	–	MHz
Overvoltage Recovery, ±12V	–	600	1000	nSec.
POWER REQUIREMENTS				
Power Supply Range				
+15V dc Supply	+14.25	+15.0	+15.75	Volts dc
-15V dc Supply	-14.25	-15.0	-15.75	Volts dc
+5V dc Supply	+4.75	+5.0	+5.25	Volts dc
Power Supply Current				
+15V dc Supply	–	+47	+55	mA
-15V dc Supply	–	-68	-75	mA
+5V dc Supply ①	–	+84	+90	mA
Power Dissipation	–	2.1	2.4	Watts
Power Supply Rejection	–	–	0.02	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Oper. Temp. Range, -MC	0	–	+70	°C
-MM	-55	–	+125	°C
Storage Temp. Range	-65	–	+150	°C
Package Type	40-pin hermetic sealed, ceramic DIP			
Pins	0.010 x 0.018 inch Kovar			
Weight	0.56 ounces (16 grams) maximum			

Specification footnotes

① +5V power usage at 1 TTL logic loading per data output bit.

Warm-up time to full specification: 5 minutes

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

DATEL

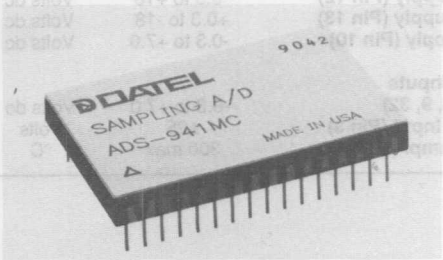
PRELIMINARY PRODUCT DATA

ADS-941

14-Bit, 1.0 MHz, High Resolution Sampling A/D Converter

FEATURES

- **14-Bit resolution**
- **1.0 MHz minimum throughput**
- **Internal Sample/Hold**
- **Functionally complete**
- **Small 32-pin DIP**
- **Low-power, 2.8 Watts**
- **Three-state output buffers**
- **Samples up to Nyquist**



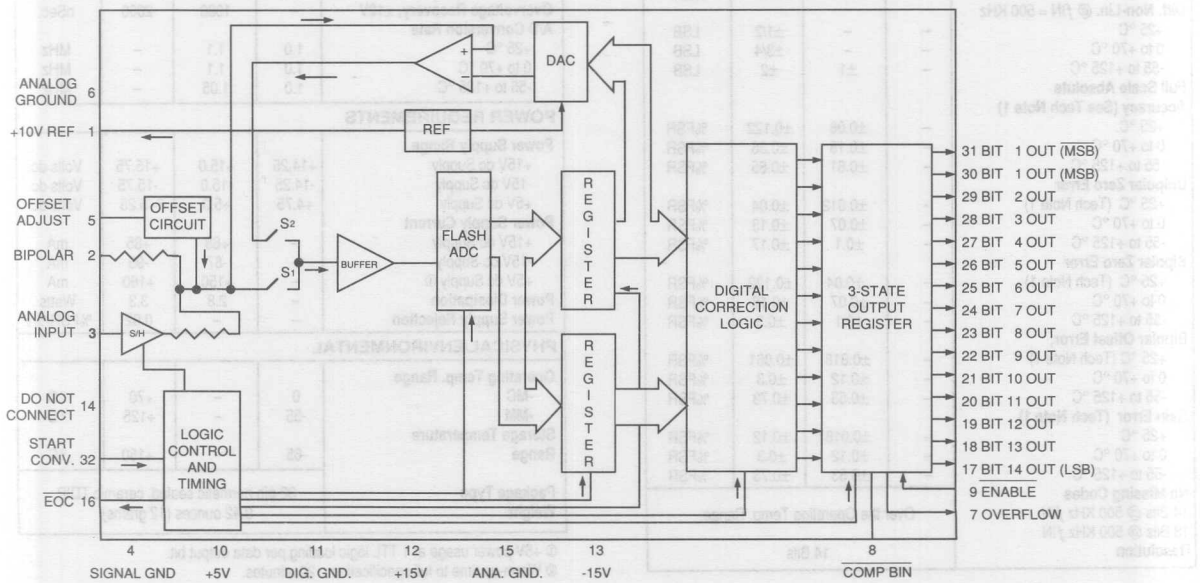
GENERAL DESCRIPTION

DATEL's ADS-941 is a 14-bit, 1.0 MHz sampling rate, functionally complete A/D converter. The ADS-941 samples up to Nyquist with no missing codes.

Packaged in a small 32-pin DIP, power requirements are ±15 volts and +5 volts with 2.8 Watts power dissipation.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+10V REF. OUT	17	BIT 14 OUT (LSB)
2	BIPOLAR	18	BIT 13 OUT
3	ANALOG INPUT	19	BIT 12 OUT
4	SIGNAL GROUND	20	BIT 11 OUT
5	OFFSET ADJUST	21	BIT 10 OUT
6	ANALOG GROUND	22	BIT 9 OUT
7	OVERFLOW	23	BIT 8 OUT
8	COMP. BIN	24	BIT 7 OUT
9	ENABLE	25	BIT 6 OUT
10	+5V	26	BIT 5 OUT
11	DIGITAL GROUND	27	BIT 4 OUT
12	+15V	28	BIT 3 OUT
13	-15V	29	BIT 2 OUT
14	NO CONNECTION	30	BIT 1 OUT (MSB)
15	ANALOG GROUND	31	BIT 1 OUT (MSB)
16	EOC	32	START CONVERT



ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 12)	-0.3 to +18	Volts dc
-15V Supply (Pin 13)	+0.3 to -18	Volts dc
+5V Supply (Pin 10)	-0.3 to +7.0	Volts dc
Digital Inputs (Pins 8, 9, 32)	-0.3 to +7.0	Volts dc
Analog Input (Pin 3)	±25	Volts
Lead Temp. (10 Sec.)	300 max	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating range and at ±15V dc and +5V dc unless otherwise specified.②

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range				
	–	0 to +10	–	Volts
	–	±5	–	Volts
Input Impedance	2.2	2.5	–	K Ohms
Input Capacitance	–	7	15	pf
DIGITAL INPUTS				
Logic Levels				
Logic "1"	2.0	–	–	Volts dc
Logic "0"	–	–	0.8	Volts dc
Logic Loading "1"	–	–	5.0	µA
Logic Loading "0"	–	–	-200	µA
PERFORMANCE				
Int. Non-Lin. @ *f*IN = 500 KHz				
+25 °C	–	±1/2	±3/4	LSB
0 to +70 °C	–	±3/4	±1	LSB
-55 to +125 °C	–	±1	±2	LSB
Diff. Non-Lin. @ *f*IN = 500 KHz				
+25 °C	–	–	±1/2	LSB
0 to +70 °C	–	–	±3/4	LSB
-55 to +125 °C	–	±1	±2	LSB
Full Scale Absolute Accuracy (See Tech Note 1)				
+25 °C.	–	±0.08	±0.122	%FSR
0 to +70 °C	–	±0.18	±0.36	%FSR
-55 to +125 °C	–	±0.61	±0.85	%FSR
Unipolar Zero Error				
+25 °C (Tech Note 1)	–	±0.012	±0.04	%FSR
0 to +70 °C	–	±0.07	±0.13	%FSR
-55 to +125 °C	–	±0.1	±0.17	%FSR
Bipolar Zero Error				
+25 °C (Tech Note 1)	–	±0.04	±0.122	%FSR
0 to +70 °C	–	±0.07	±0.18	%FSR
-55 to +125 °C	–	±0.1	±0.3	%FSR
Bipolar Offset Error,				
+25 °C (Tech Note 1)	–	±0.018	±0.061	%FSR
0 to +70 °C	–	±0.12	±0.3	%FSR
-55 to +125 °C	–	±0.53	±0.73	%FSR
Gain Error (Tech Note 1)				
+25 °C	–	±0.018	±0.12	%FSR
0 to +70 °C	–	±0.12	±0.3	%FSR
-55 to +125 °C	–	±0.53	±0.73	%FSR
No Missing Codes	Over the Operating Temp. Range.			
14 Bits @ 500 KHz *f*IN				
13 Bits @ 500 KHz *f*IN				
Resolution	14 Bits			

OUTPUTS	MIN.	TYP.	MAX.	UNITS
Output Coding				
(Pin 8 Hi)	Straight bin./offset bin./2's Comp.			
(Pin 8 Low)	Comp. bin./Comp. offset bin., C2C			
Logic Levels				
Logic "1"	2.4	–	–	Volts dc
Logic "0"	–	–	0.4	Volts dc
Logic Loading "1"	–	–	-160	µA
Logic Loading "0"	–	–	6.4	mA
Internal Reference				
Voltage, +25 °C	+9.98	+10.0	+10.02	Volts dc
Drift	–	±13	±30	ppm/ °C
External Current	–	–	5	mA
PERFORMANCE				
Slew Rate	180	200	–	V/µSec.
Aperture Delay Time	–	–	±12	nSec.
Aperture Uncertainty	–	–	±100	pSec.
S/H Acquisition Time				
(to 0.006%FS (10V step)	–	250	300	nSec.
Total Harm. Distort. (-0.5 dB)				
DC to 100 KHz	-82	-90	–	FS - dB
100 KHz to 500 KHz	-77	-85	–	FS - dB
Signal-to-Noise Ratio				
(w/o distortion, -0.5 dB)				
DC to 100 KHz	-82	-90	–	FS - dB
100 KHz to 500 KHz	-77	-85	–	FS - dB
Signal-to-Noise Ratio				
& distortion, -0.5 dB				
DC to 100 KHz	-74	-78	–	FS - dB
100 KHz to 500 KHz	-69	-73	–	FS - dB
Effective Bits, -0.5 dB				
DC to 100 KHz	12.4	13.1	–	Bits
100 KHz to 500 KHz	11.8	12.3	–	Bits
Two-tone Intermodulation Distortion (fIN = 100 KHz,				
240 KHz, Fs=1.0 MHz, -0.5 dB)	-92	–	–	FS - dB
Input Bandwidth				
Small Signal (-20 dB input)	6	–	–	MHz
Full Power (0 dB input)	1.75	–	–	MHz
Feedthrough Rejection				
@ fIN = 500 KHz	-87	–	–	dB
Overvoltage Recovery, ±12V	–	1000	2000	nSec.
A/D Conversion Rate				
+25 °C	1.0	1.1	–	MHz
0 to +70 °C	1.0	1.1	–	MHz
-55 to +125 °C	1.0	1.05	–	MHz
POWER REQUIREMENTS				
Power Supply Range				
+15V dc Supply	+14.25	+15.0	+15.75	Volts dc
-15V dc Supply	-14.25	-15.0	-15.75	Volts dc
+5V dc Supply	+4.75	+5.0	+5.25	Volts dc
Power Supply Current				
+15V dc Supply	–	+68	+85	mA
-15V dc Supply	–	-87	-95	mA
+5V dc Supply ①	–	+150	+160	mA
Power Dissipation	–	2.8	3.3	Watts
Power Supply Rejection	–	–	0.02	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range				
-MC	0	–	+70	°C
-MM	-55	–	+125	°C
Storage Temperature Range	-65	–	+150	°C
Package Type	32-pin hermetic sealed, ceramic TDIP			
Weight	0.42 ounces (12 grams)			

① +5V power usage at 1 TTL logic loading per data output bit.
② Warm-up time to full specification: 20 minutes.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

TECHNICAL NOTES

1. Use external potentiometers to remove system errors or the small initial errors to zero. Use a 200 Ω trimming potentiometer in series with the analog input for gain adjustment. Use a short in place of the gain adjustment trim pot for operation without adjustments. Use a 20K trimming potentiometer with the wiper tied to pin 5 for zero/offset adjustment (connect pin 5 to pin 15, analog ground for operation without adjustment).

2. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

3. Bypass the analog and digital supplies and the +10V reference (pin 1) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 1) to analog ground (pin 15).

4. Obtain straight binary/offset binary output coding by tying COMP BIN (pin 8) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie the COMP BIN pin to ground. The COMP BIN signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

5. To enable the three-state outputs, connect ENABLE (pin 9) to a logic "0" (low). To disable, connect ENABLE (pin 9) to a logic "1" (high).

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3, and Table 1 for the appropriate full-scale range (FSR). Apply a pulse of 50 nanoseconds minimum to the START CONVERT input (pin 32) at a rate of 200 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

Table 1. Input Connections

INPUT RANGE	INPUT PIN	TIE TOGETHER
0 to -10V	Pin 3	Pins 2 and 4
±5V	Pin 3	Pins 1 and 2

Table 2. Zero and Gain Adjust

FSR	ZERO ADJUST +1/2 LSB	GAIN ADJUST FS - 1/2 LSB
0 to +10V	-305 µV	-9.999085V
±5V	-305 µV	-4.999085V

2. Zero Adjustments
Apply a precision voltage reference source between the analog input (pin 3) and signal ground (pin 4). Adjust the output of the reference source per Table 2.

For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 00 0000 0000 0000 and 00 0000 0000 0001 with the COMP BIN (pin 8) tied low (straight binary) or between 11 1111 1111 1111 and 11 1111 1111 1110 with the pin 8 tied high (complementary binary).

For bipolar operation, adjust the potentiometer such that the code flickers equally between 10 0000 0000 0000 and 10 0000 0000 0001 with pin 8 tied high (offset binary) or between 01 1111 1111 1111 and 01 1111 1111 1110 with pin 8 tied low (complementary offset binary).

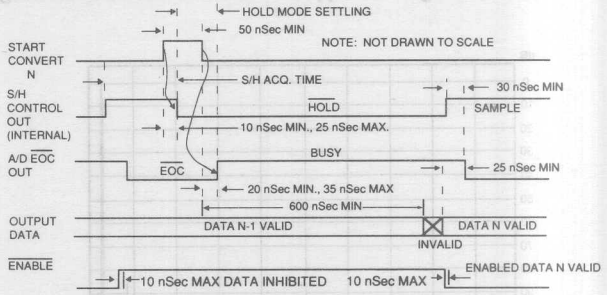
Two's complement coding requires use of the MSB (pin 31) with COMP BIN (pin 8) tied high, adjusting the potentiometer such that the code flickers between 00 0000 0000 0000 and 00 0000 0000 0001.

3. Full-Scale Adjustment
Set the output of the voltage reference used in step 2 to the value shown in Table 2.

Adjust the gain trimming potentiometer so that the output code flickers equally between 11 1111 1111 1110 and 11 1111 1111 1111 for COMP BIN (pin 8) tied low for unipolar operation or tied high for bipolar operation (straight binary/offset binary) or between 00 0000 0000 0000 and 00 0000 0000 0001 for COMP BIN tied high for unipolar operastion- or tied low for bipolar operation (complementary binary/complementary offset binary).

Two's complement coding requires use of the MSB (pin 31) with the COMP BIN (pin 8) tied high, adjusting the gain trimming potentiometer so that the output code flickers equally between 01 1111 1111 1110 and 01 1111 1111 1111.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 3.



NOTE: Retriggering the START CONVERT pulse before EOC goes low will not initiate a new conversion.

NOTE: The specifications listed apply over the full operating temperature range unless otherwise specified.

Figure 2. ADS-941 Timing Diagram

Table 3. Output Coding

	STRAIGHT BIN.	COMP. BINARY					
UNIPOLAR SCALE	INPUT RANGES, V dc 0 to +10V	OUTPUT CODING MSB LSB		MSB LSB		INPUT RANGE ±10V dc	BI POLAR SCALE
FS -1 LSB	-9.999390	11 1111 1111 1111		00 0000 0000 0000		01 1111 1111 1111	-4.99939	+FS -1 LSB
7/8 FS	-8.750000	11 1000 0000 0000		00 0111 1111 1111		01 1000 0000 0000	-3.75000	+3/4 FS
3/4 FS	-7.500000	11 0000 0000 0000		00 1111 1111 1111		01 0000 0000 0000	-2.50000	+1/2 FS
1/2 FS	-5.000000	10 0000 0000 0000		01 1111 1111 1111		00 0000 0000 0000	0.00000	0
1/4 FS	-2.500000	01 0000 0000 0000		10 1111 1111 1111		10 0000 0000 0000	+2.50000	-1/2 FS
1/8 FS	-1.250000	00 1000 0000 0000		11 0111 1111 1111		10 1000 0000 0000	+3.75000	-3/4 FS
1 LSB	-0.000610	00 0000 0000 0001		11 1111 1111 1110		10 0000 0000 0001	+4.99939	-FS +1 LSB
0	0.000000	00 0000 0000 0000		11 1111 1111 1111		10 00000000 0000	+5.00000	-FS
	OFF. BINARY	COMP.	OFF. BIN.	TWO'S	COMP.			

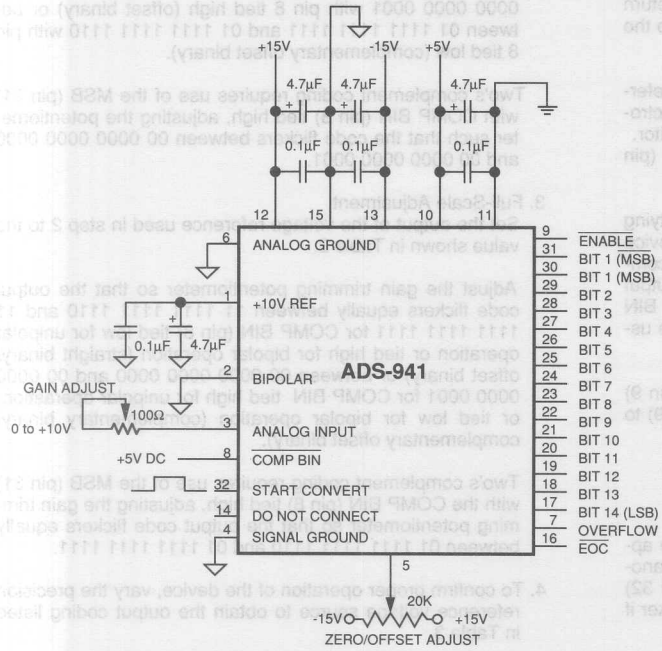
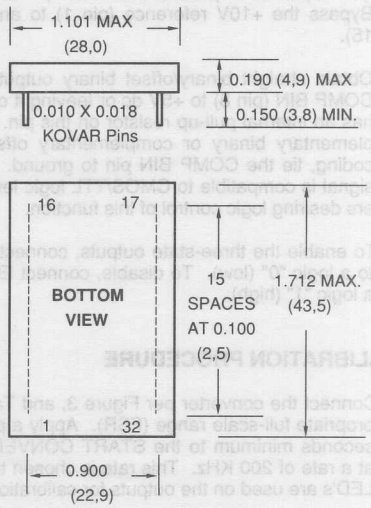


Figure 3. Typical ADS-941 Connection Diagram

MECHANICAL DIMENSIONS INCHES (MM)



NOTE: Pins have a 0.025 inch, ±0.01 stand-off from case.

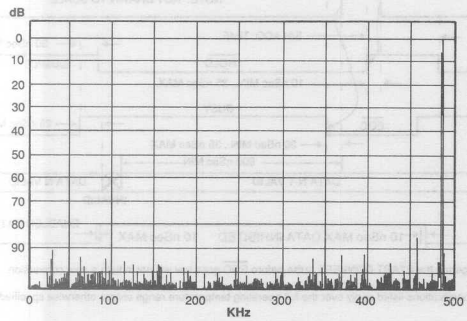


Figure 4. FFT Analysis of ADS-941

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	SEAL
ADS-941MC	0 °C to +70 °C	Hermetic
ADS-941MM	-55 °C to +125 °C	Hermetic
ACCESSORY	ADS-EVAL1	Evaluation Board (without ADS-941)

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 32 required.

For availibility of MIL-STD-883B versions, contact DATEL.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

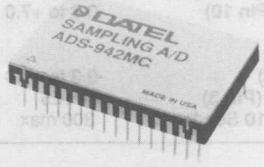
ADS-942

14-Bit, 2.0 MHz, High Resolution Sampling A/D Converter

PRELIMINARY PRODUCT DATA

FEATURES

- 14-Bit resolution
- Internal Sample/Hold
- 2.0 MHz minimum throughput
- Functionally complete
- Small 32-pin DIP
- Low-power 2.9 Watts
- Three-state output buffers
- Samples up to Nyquist



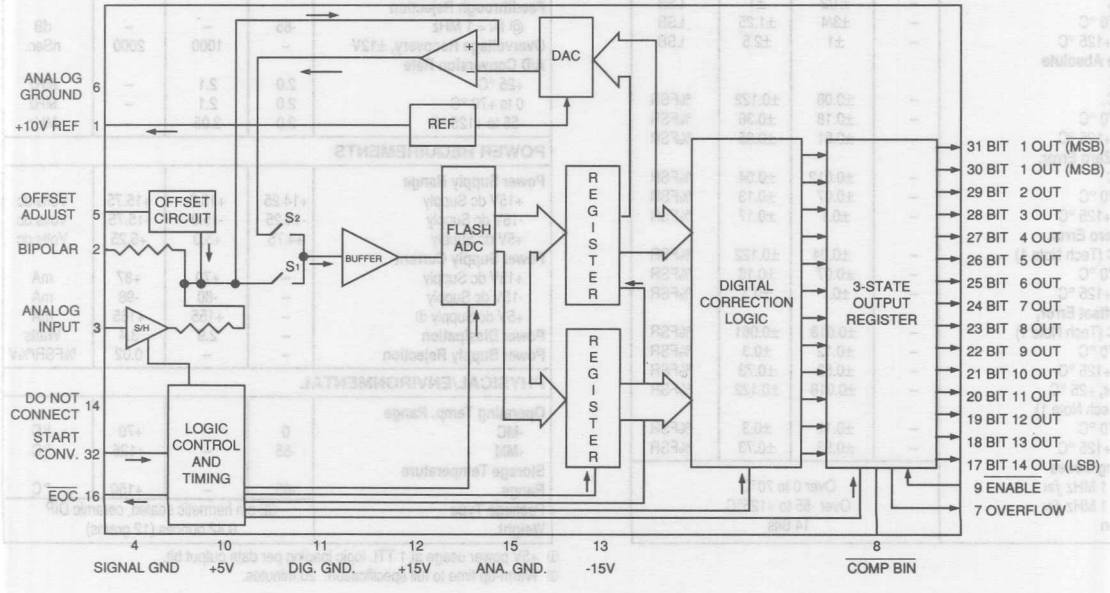
GENERAL DESCRIPTION

DATEL's ADS-942 is a 14-bit, 2.0 MHz sampling rate, functionally complete A/D converter. The ADS-942 samples up to Nyquist with no missing codes.

Packaged in a small 32-pin DIP, power requirements are ±15 volts and +5 volts with 2.9 Watts power dissipation.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+10V REF. OUT	17	BIT 14 OUT (LSB)
2	BIPOLAR	18	BIT 13 OUT
3	ANALOG INPUT	19	BIT 12 OUT
4	SIGNAL GROUND	20	BIT 11 OUT
5	OFFSET ADJUST	21	BIT 10 OUT
6	ANALOG GROUND	22	BIT 9 OUT
7	OVERFLOW	23	BIT 8 OUT
8	$\overline{\text{COMP. BIN}}$	24	BIT 7 OUT
9	$\overline{\text{ENABLE}}$	25	BIT 6 OUT
10	+5V	26	BIT 5 OUT
11	DIGITAL GROUND	27	BIT 4 OUT
12	+15V	28	BIT 3 OUT
13	-15V	29	BIT 2 OUT
14	DO NOT CONNECT	30	BIT 1 OUT (MSB)
15	ANALOG GROUND	31	$\overline{\text{BIT 1 OUT (MSB)}}$
16	$\overline{\text{EOC}}$	32	START CONVERT



ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 12)	-0.3 to +18	Volts dc
-15V Supply (Pin 13)	+0.3 to -18	Volts dc
+5V Supply (Pin 10)	-0.3 to +7.0	Volts dc
Digital Inputs (Pins 8, 9, 32)	-0.3 to +7.0	Volts dc
Analog Input (Pin 3)	±25	Volts
Lead Temp. (10 Sec.)	300 max	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and +5V dc unless otherwise specified.②

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range				
	–	0 to +10	–	Volts
	–	±5	–	Volts
Input Impedance	2.2	2.5	–	K Ohms
Input Capacitance	–	7	15	pf
DIGITAL INPUTS				
Logic Levels				
Logic "1"	2.0	–	–	Volts dc
Logic "0"	–	–	0.8	Volts dc
Logic Loading "1"	–	–	5.0	µA
Logic Loading "0"	–	–	-200	µA
PERFORMANCE				
Int. Non-Lin. @ f_{IN} = 1 MHz				
+25 °C	–	±1/2	±1	LSB
0 to +70 °C	–	±3/4	±1.5	LSB
-55 to +125 °C	–	±1	±2.5	LSB
Diff. Non-Lin. @ f_{IN} = 1 MHz				
+25 °C	–	±1/2	±1	LSB
0 to +70 °C	–	±3/4	±1.25	LSB
-55 to +125 °C	–	±1	±2.5	LSB
Full Scale Absolute Accuracy				
+25 °C.	–	±0.08	±0.122	%FSR
0 to +70 °C	–	±0.18	±0.36	%FSR
-55 to +125 °C	–	±0.61	±0.85	%FSR
Unipolar Zero Error,				
+25 °C	–	±0.012	±0.04	%FSR
0 to +70 °C	–	±0.07	±0.13	%FSR
-55 to +125 °C	–	±0.1	±0.17	%FSR
Bipolar Zero Error,				
+25 °C (Tech Note 1)	–	±0.04	±0.122	%FSR
0 to +70 °C	–	±0.07	±0.18	%FSR
-55 to +125 °C	–	±0.1	±0.3	%FSR
Bipolar Offset Error,				
+25 °C (Tech Note 1)	–	±0.018	±0.061	%FSR
0 to +70 °C	–	±0.12	±0.3	%FSR
-55 to +125 °C	–	±0.53	±0.73	%FSR
Gain Error, +25 °C (See Tech Note 1)	–	±0.018	±0.122	%FSR
0 to +70 °C	–	±0.12	±0.3	%FSR
-55 to +125 °C	–	±0.53	±0.73	%FSR
No Missing Codes				
14 Bits @ 1 MHz f_{IN}		Over 0 to 70°C		
13 Bits @ 1 MHz f_{IN}		Over -55 to +125°C		
Resolution		14 Bits		

OUTPUTS	MIN.	TYP.	MAX.	UNITS
Output Coding				
(Pin 8 Hi)		Straight binary/offset binary		
(Pin 8 Low)		Complementary binary		
Logic Levels				
Logic "1"	2.4	–	–	Volts dc
Logic "0"	–	–	0.4	Volts dc
Logic Loading "1"	–	–	-160	µA
Logic Loading "0"	–	–	6.4	mA
Internal Reference				
Voltage, +25 °C	+9.98	+10.0	+10.02	Volts dc
Drift	–	±13	±30	ppm/ °C
External Current	–	–	5	mA
DYNAMIC PERFORMANCE				
Total Harm. Distort. (-0.5 dB)				
DC to 100 KHz	-79	-85	–	FS - dB
100 KHz to 1 MHz	-73	-79	–	FS - dB
Signal-to-Noise Ratio (w/o distortion, -0.5 dB)				
DC to 100 KHz	-78	-85	–	FS - dB
100 KHz to 1 MHz	-73	-79	–	FS - dB
Signal-to-Noise Ratio & distortion, -0.5 dB				
DC to 100 KHz	-72	-77	–	FS - dB
100 KHz to 1 MHz	-68	-71	–	FS - dB
Effective Bits, -0.5 dB				
DC to 100 KHz	12.3	13.0	–	Bits
100 KHz to 1 MHz	11.7	12.3	–	Bits
Two-tone Intermodulation Distortion (f_{IN} = 100 KHz, 240 KHz, Fs=2.0 MHz, -0.5 dB)	-92	–	–	FS - dB
Input Bandwidth				
Small Signal (-20 dB input)	6	–	–	MHz
Full Power (0 dB input)	1.75	–	–	MHz
Slew Rate	210	250	–	V/µSec.
Aperture Delay Time	–	–	±10	nSec.
Aperture Uncertainty, Rms	–	–	±10	pSec.
S/H Acquisition Time (to 0.006%FS (10V step)	–	120	150	nSec.
Feedthrough Rejection @ f_{IN} = 1 MHz	-85	–	–	dB
Overvoltage Recovery, ±12V	–	1000	2000	nSec.
A/D Conversion Rate				
+25 °C	2.0	2.1	–	MHz
0 to +70 °C	2.0	2.1	–	MHz
-55 to +125 °C	2.0	2.05	–	MHz
POWER REQUIREMENTS				
Power Supply Range				
+15V dc Supply	+14.25	+15.0	+15.75	Volts dc
-15V dc Supply	-14.25	-15.0	-15.75	Volts dc
+5V dc Supply	+4.75	+5.0	+5.25	Volts dc
Power Supply Current				
+15V dc Supply	–	+70	+87	mA
-15V dc Supply	–	-80	-98	mA
+5V dc Supply ①	–	+155	+165	mA
Power Dissipation	–	2.9	3.4	Watts
Power Supply Rejection	–	–	0.02	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range				
-MC	0	–	+70	°C
-MM	-55	–	+125	°C
Storage Temperature Range	-65	–	+150	°C
Package Type		32-pin hermetic sealed, ceramic DIP		
Weight		0.42 ounces (12 grams)		

① +5V power usage at 1 TTL logic loading per data output bit.
② Warm-up time to full specification: 20 minutes.

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TECHNICAL NOTES

1. Use external potentiometers to remove system errors or the small initial errors to zero. Use a 200 Ω trimming potentiometer in series with the analog input for gain adjustment. Use a short in place of the gain adjustment trim pot for operation without adjustments. Use a 20K trimming potentiometer with the wiper tied to pin 5 for zero/offset adjustment (connect pin 5 to pin 15, analog ground for operation without adjustment).

2. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

3. Bypass the analog and digital supplies and the +10V reference (pin 1) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 1) to analog ground (pin 15).

4. Obtain straight binary/offset binary output coding by tying COMP BIN (pin 8) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie pin 18 to ground. The pin 18 signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

5. To enable the three-state outputs, connect ENABLE (pin 9) to a logic "0" (low). To disable, connect pin 9 to a logic "1" (high).

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3, and Table 1 for the appropriate full-scale range (FSR). Apply a pulse of 35 nanoseconds minimum to the START CONVERT input (pin 32) at a rate of 200 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

Table 1. Input Connections

INPUT RANGE	INPUT PIN	TIE TOGETHER
0 to +10V	Pin 3	Pins 2 and 4
±5V	Pin 3	Pins 1 and 2

Table 2. Zero and Gain Adjust

FSR	ZERO ADJUST +1/2 LSB	GAIN ADJUST FS - 1/2 LSB
0 to +10V	-305 µV	+9.999085V
±5V	-305 µV	-4.999085V

2. Zero Adjustments
   Apply a precision voltage reference source between the analog input (pin 3) and signal ground (pin 4). Adjust the output of the reference source per Table 2.

   For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 00 0000 0000 0000 and 00 0000 0000 0001 with the COMP BIN (pin 8) tied low (straight binary) or between 11 1111 1111 1111 and 11 1111 1111 1110 with the pin 8 tied high (complementary binary).

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 10 0000 0000 0000 and 10 0000 0000 0001 with pin 8 tied high (offset binary) or between 01 1111 1111 1111 and 01 1111 1111 1110 with pin 8 tied low (complementary offset binary).

   Two's complement coding requires use of the MSB (pin 31) with COMP BIN (pin 8) tied high, adjusting the potentiometer such that the code flickers between 00 0000 0000 0000 and 00 0000 0000 0001.

3. Full-Scale Adjustment
   Set the output of the voltage reference used in step 2 to the value shown in Table 2.

   Adjust the gain trimming potentiometer so that the output code flickers equally between 11 1111 1111 1110 and 11 1111 1111 1111 for COMP BIN (pin 8) tied low for unipolar operation or tied high for bipolar operation (straight binary/offset binary) or between 00 0000 0000 0000 and 00 0000 0000 0001 for COMP BIN tied high for unipolar operastion- or tied low for bipolar operation (complementary binary/complementary offset binary).

   Two's complement coding requires use of the MSB (pin 31) with the COMP BIN (pin 8) tied high, adjusting the gain trimming potentiometer so that the output code flickers equally between 01 1111 1111 1110 and 01 1111 1111 1111.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 3.

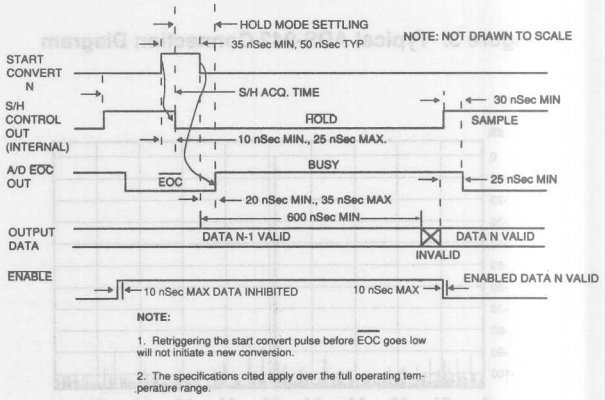


Figure 2. ADS-942 Timing Diagram

Table 3. Output Coding

		STRAIGHT BIN. COMP. BINARY					
UNIPOLAR SCALE	INPUT RANGES, V dc 0 to +10V	OUTPUT CODING MSB LSB	MSB LSB	MSB LSB	INPUT RANGE ±10V dc	BI POLAR SCALE
FS -1 LSB	+9.999390	11 1111 1111 1111	00 0000 0000 0000	01 1111 1111 1111	-4.99939	+FS -1 LSB
7/8 FS	+8.750000	11 1000 0000 0000	00 0111 1111 1111	01 1000 0000 0000	-3.75000	+3/4 FS
3/4 FS	+7.500000	11 0000 0000 0000	00 1111 1111 1111	01 0000 0000 0000	-2.50000	+1/2 FS
1/2 FS	+5.000000	10 0000 0000 0000	01 1111 1111 1111	00 0000 0000 0000	0.00000	0
1/4 FS	+2.500000	01 0000 0000 0000	10 1111 1111 1111	10 0000 0000 0000	+2.50000	-1/2 FS
1/8 FS	+1.250000	00 1000 0000 0000	11 0111 1111 1111	10 1000 0000 0000	+3.75000	-3/4 FS
1 LSB	+0.000610	00 0000 0000 0001	11 1111 1111 1110	10 0000 0000 0001	+4.99939	-FS +1 LSB
0	0.000000	00 0000 0000 0000	11 1111 1111 1111	10 00000000 0000	+5.00000	-FS
		OFF. BINARY	COMP. OFF. BIN.	TWO'S COMP.		

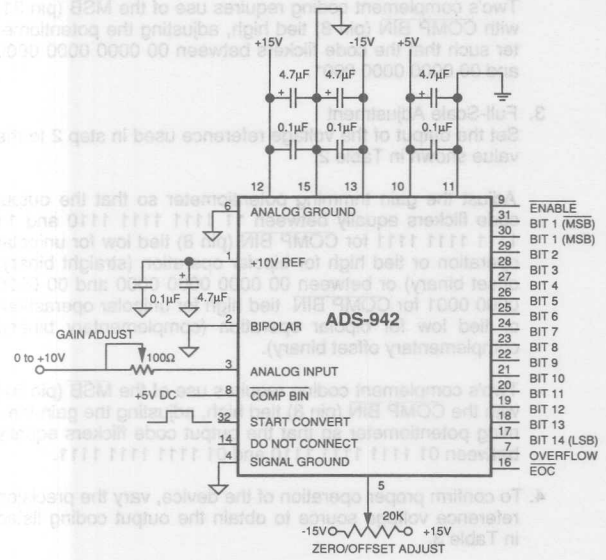
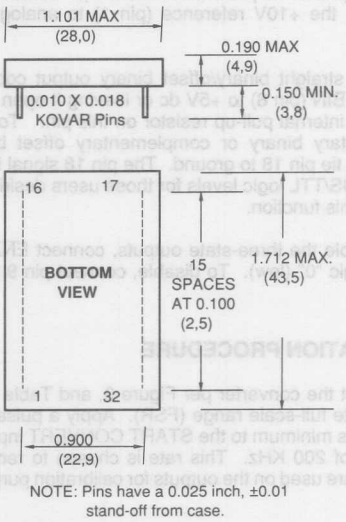


Figure 3. Typical ADS-942 Connection Diagram

MECHANICAL DIMENSIONS INCHES (MM)



NOTE: Pins have a 0.025 inch, ±0.01 stand-off from case.

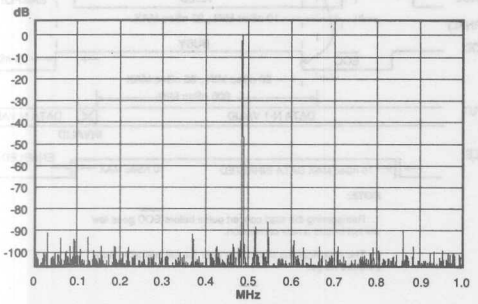


Figure 4. FFT Analysis of ADS-942

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	SEAL
ADS-942MC	0 °C to +70 °C	Hermetic
ADS-942MM	-55 °C to +125 °C	Hermetic
ACCESSORY	ADS-EVAL1	Evaluation Board (without ADS-942)

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 32 required.

For availibility of MIL-STD-883B versions, contact DATEL.

ADS-944

14-Bit, 5.0 MHz, High Resolution Sampling A/D Converter

ADVANCED PRODUCT DATA

FEATURES

- **14-Bit resolution**
- **Internal Sample/Hold**
- **5.0 MHz minimum throughput**
- **Functionally complete**
- **Small 32-pin DIP**
- **Low-power 3.4 Watts**
- **Three-state output buffers**
- **Samples up to Nyquist**

GENERAL DESCRIPTION

DATEL's ADS-944 is a 14-bit, 5.0 MHz sampling rate, functionally complete sampling A/D converter. The ADS-944 samples up to Nyquist with no missing codes.

Packaged in a small 32-pin DIP, power requirements are ±15 volts and +5 volts with 3.4 Watts power dissipation.

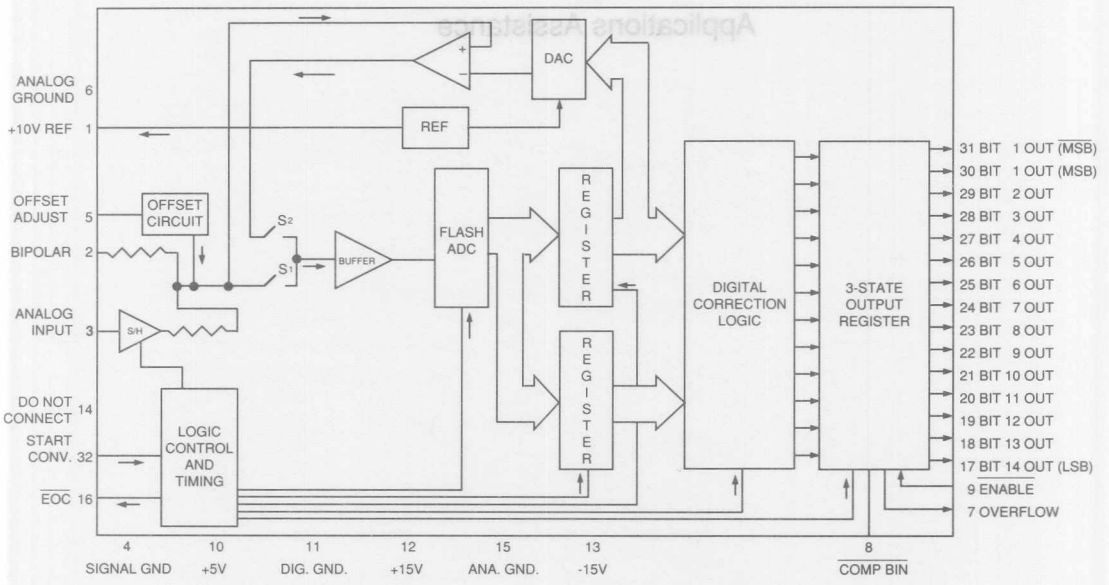
The ADS-944 is offered in the comercial 0 to +70 °C and military -55 to +125 °C operating temperature range.

APPLICATIONS

- **Spectrum analysis**
- **Imaging**
- **Radar**
- **Medical instrumentation**
- **High-speed data acquisition systems**

I/O CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+10V REF. OUT	17	BIT 14 OUT (LSB)
2	BIPOLAR	18	BIT 13 OUT
3	ANALOG INPUT	19	BIT 12 OUT
4	SIGNAL GROUND	20	BIT 11 OUT
5	OFFSET ADJUST	21	BIT 10 OUT
6	ANALOG GND	22	BIT 9 OUT
7	OVERFLOW	23	BIT 8 OUT
8	COMP. BIN.	24	BIT 7 OUT
9	ENABLE	25	BIT 6 OUT
10	+5V	26	BIT 5 OUT
11	DIGITAL GROUND	27	BIT 4 OUT
12	+15V	28	BIT 3 OUT
13	-15V	29	BIT 2 OUT
14	DO NOT CONNECT	30	BIT 1 OUT (MSB)
15	ANALOG GROUND	31	BIT 1 OUT (MSB)
16	EOC	32	START CONVERT



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Dial

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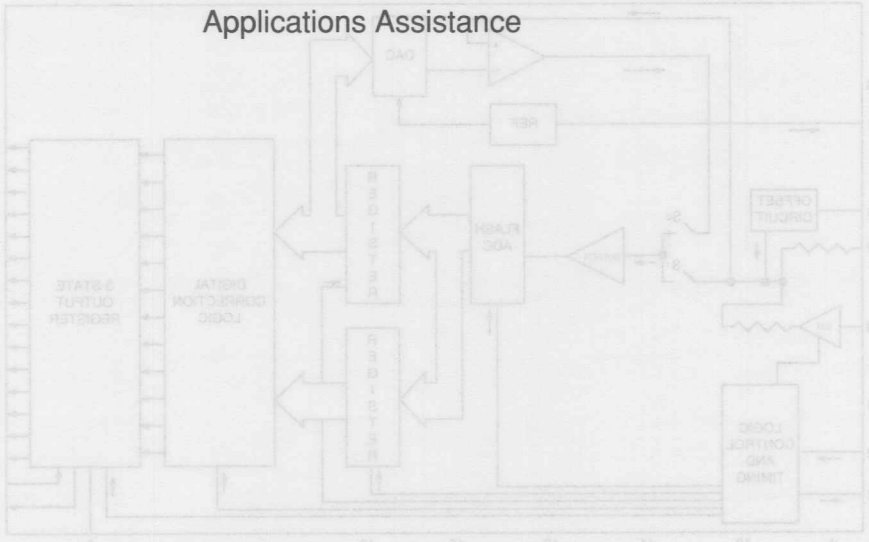


FEATURES

- **14-Bit resolution**
- **10 MHz sampling rate**
- **Functionally complete**
- **Internal S/H**
- **Small 40-pin DIP**
- **Low-power, 4.2 Watts**
- **Three-state output buffers**
- **Samples up to Nyquist**
- **16 word FIFO memory**

GENERAL DESCRIPTION

DATEL's ADS-945 is a 14-bit, 10 MHz sampling rate, functionally complete A/D converter with internal FIFO. The ADS-945 samples up to Nyquist with no missing codes.

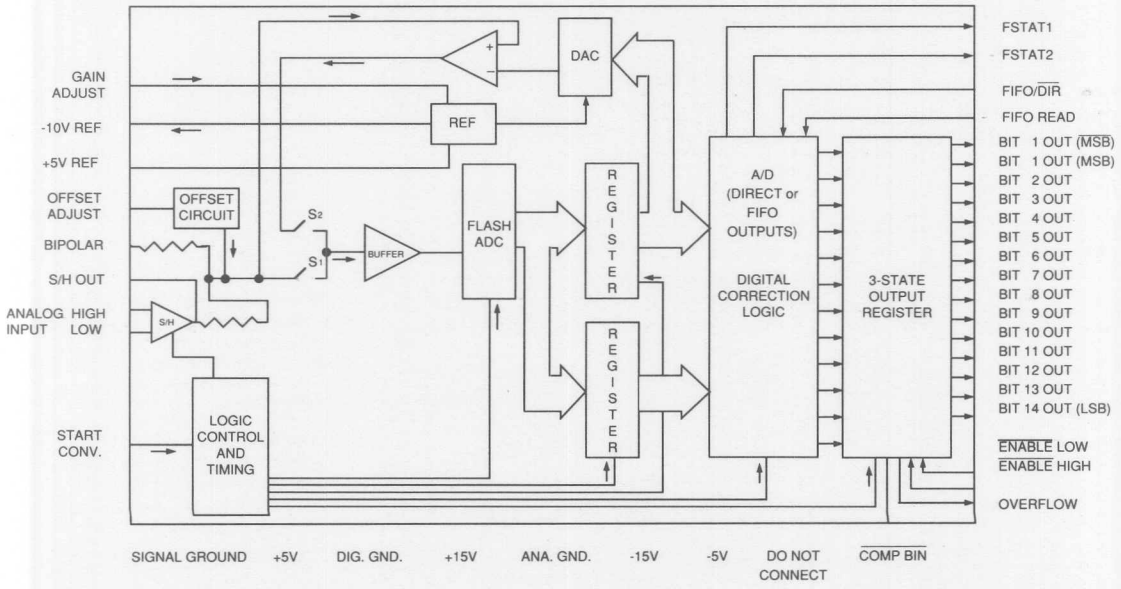
Packaged in a small 40-pin TDIP, power requirements are ±15 Volts and ±5 Volts with 4.2 Watts power dissipation.

APPLICATIONS

- **Spectroscopy**
- **Spectrum analysis**
- **Imaging**
- **Radar**
- **Medical instrumentation**
- **High-speed data acquisition systems**

I/O Connections

Function	Function
+5V REFERENCE	START CONVERT
OFFSET ADJUST	FIFO/$\overline{\text{DIR}}$
ANALOG INPUT HIGH	FIFO READ
ANALOG INPUT LOW	BIT 8 OUT
BIPOLAR	BIT 7 OUT
-10V REFERENCE	BIT 6 OUT
ENABLE LOW B9-14	BIT 5 OUT
GAIN ADJUST	BIT 4 OUT
OVERFLOW	BIT 3 OUT
DO NOT CONNECT	BIT 2 OUT
-5V	BIT 1 OUT (MSB)
BIT 14 OUT (LSB)	+5V
BIT 13 OUT	DIGITAL GROUND
BIT 12 OUT	ENABLE HIGH (B1-8)
BIT 11 OUT	S/H OUT
BIT 10 OUT	COMP BIN
BIT 9 OUT	-15V
FSTAT1	ANALOG GROUND
FSTAT2	ANALOG GROUND
BIT 1 OUT ($\overline{\text{MSB}}$)	+15V



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ADS-976
16-bit, 200 KHz, Low-Power Sampling A/D Converter

PRELIMINARY PRODUCT DATA

FEATURES

- **16-bit resolution**
- **200 KHz sampling rate**
- **Compatible to industry standard ADC76, AD376, AD1376**
- **Internal sample-hold**
- **Small 32-pin DIP**
- **Low-power, 1.8 Watts**
- **Samples to Nyquist**
- **16 word FIFO memory**

GENERAL DESCRIPTION

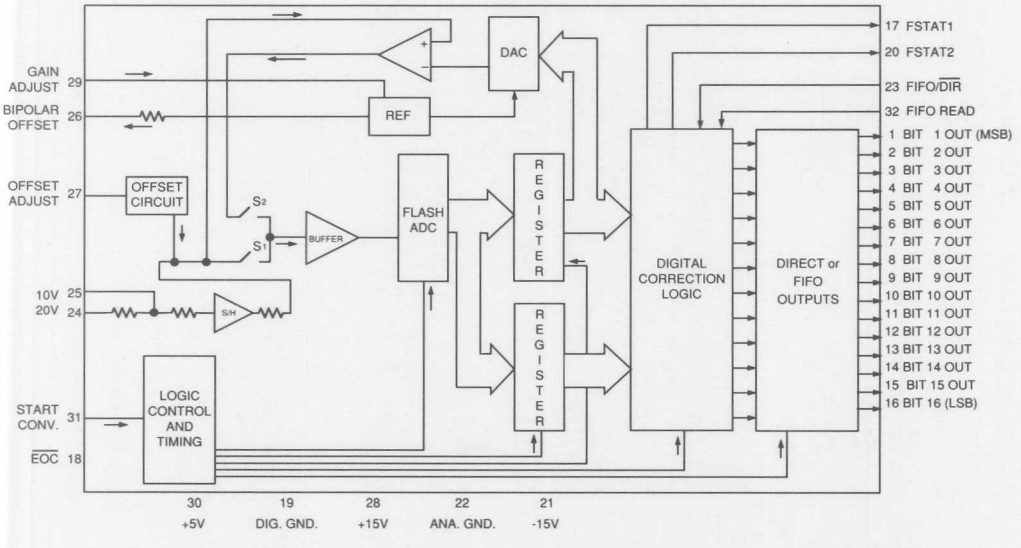
DATEL's ADS-976 is a 16-bit, 200 KHz sampling rate, functionally complete A/D converter with an internal sample-hold. The ADS-976 samples up to Nyquist with no missing codes.

The internal FIFO can be either bypassed or utilized with full (16 words) or half-full (8 words). The FIFO capability still allows the ADS-976 to be compatible to the industry pin-out versions for 16-bit parallel output applications.

Packaged in a small 32-pin DIP, power requirements are ±15 volts and +5 volts with a 1.8 Watts power dissipation.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 OUT (MSB)	32	FIFO READ
2	BIT 2 OUT	31	START CONVERT
3	BIT 3 OUT	30	+5V
4	BIT 4 OUT	29	GAIN ADJUST
5	BIT 5 OUT	28	+15V
6	BIT 6 OUT	27	OFFSET ADJUST
7	BIT 7 OUT	26	BIPOLAR OFFSET
8	BIT 8 OUT	25	10V
9	BIT 9 OUT	24	20V
10	BIT 10 OUT	23	FIFO/$\overline{DIR}$
11	BIT 11 OUT	22	ANALOG GROUND
12	BIT 12 OUT	21	-15V
13	BIT 13 OUT	20	FSTAT2
14	BIT 14 OUT	19	DIGITAL GROUND
15	BIT 15 OUT	18	$\overline{EOC}$
16	BIT 16 OUT (LSB)	17	FSTAT1



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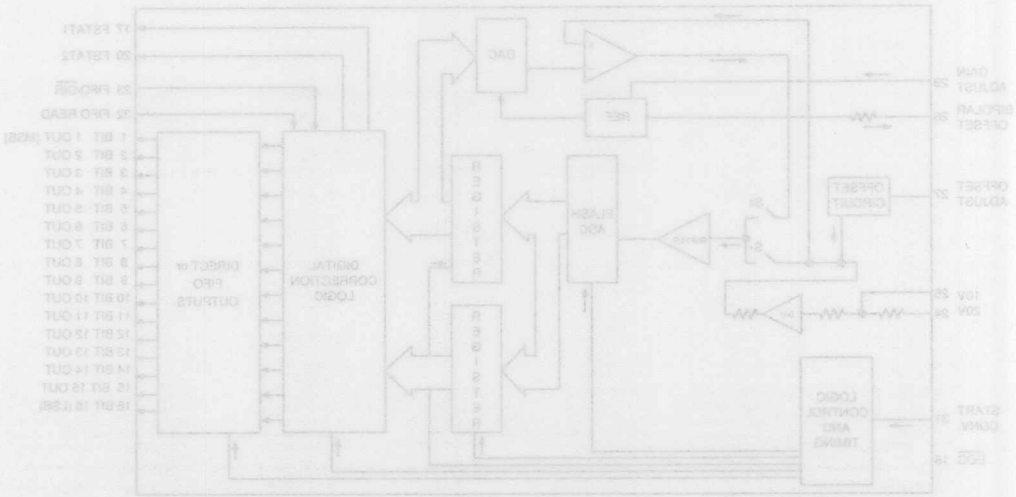

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A/D CONVERTERS

	Model	Resolution (Bits)	Conversion Time (µsec)	Linearity Error	Power (Watts)	Case	Page
	ADC-207	7	0.050	±1/2 LSB	0.25	18-Pin DIP	2-1
	ADC-228	8	0.040	±1/2 LSB	1.25	24-Pin DIP	2-9
	ADC-208	8	0.050	±3/4 LSB	0.60	24-Pin DIP	2-5
	ADC-304	8	0.050	±1/2 LSB	0.39	28-Pin DIP	2-13
New	**ADC-530**	12	0.350	±3/4 LSB	2.10	32-Pin DIP	2-33
	ADC-500	12	0.500	±1 LSB	1.70	32-Pin DIP	2-17
	ADC-505	12	0.550	±1 LSB	1.70	32-Pin DIP	2-17
	ADC-508	12	0.700	±1 LSB	1.70	32-Pin DIP	2-21
	ADC-520	12	0.800	±1/2 LSB	1.60	32-Pin DIP	2-29
	ADC-521	12	0.800	±1/2 LSB	1.60	32-Pin DIP	2-29
	ADC-511	12	1.0	±3/4 LSB	1.25	24-Pin DIP	2-25
	ADC-HZ12B	12	8	±1/2 LSB	1.5	32-Pin DIP	2-55
	ADC-HX12B	12	20	±1/2 LSB	1.5	32-Pin DIP	2-55
	ADC-HC12B	12	300	±1/2 LSB	0.17	32-Pin DIP	2-47
	ADC-908	14	1.0	±1/2 LSB	2.70	32-Pin DIP	2-37
	ADC-914	14	2.4	±1 LSB	1.20	24-Pin DIP	2-41

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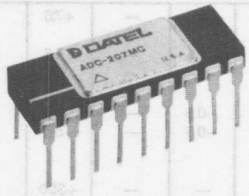
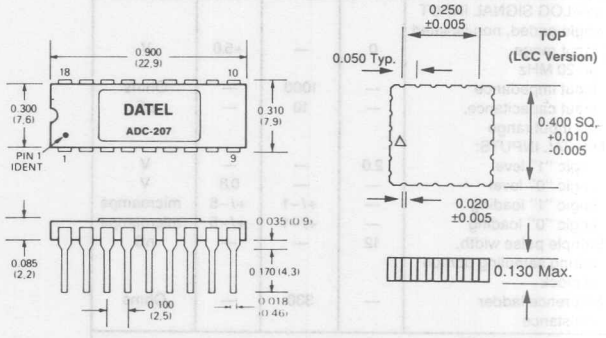
ADC-207
7-Bit, 20 MSPS CMOS Flash A/D

FEATURES

- 7-Bit flash A/D converter
- 20 MHz Sampling rate
- Low-power (250 mW)
- +5V dc Operation
- 1.2 Micron CMOS
- 7-bit latched 3-state output with overflow bit
- Surface mount versions
- MIL-STD-883 versions
- No missing codes

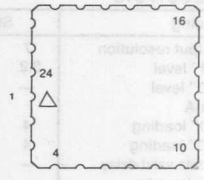


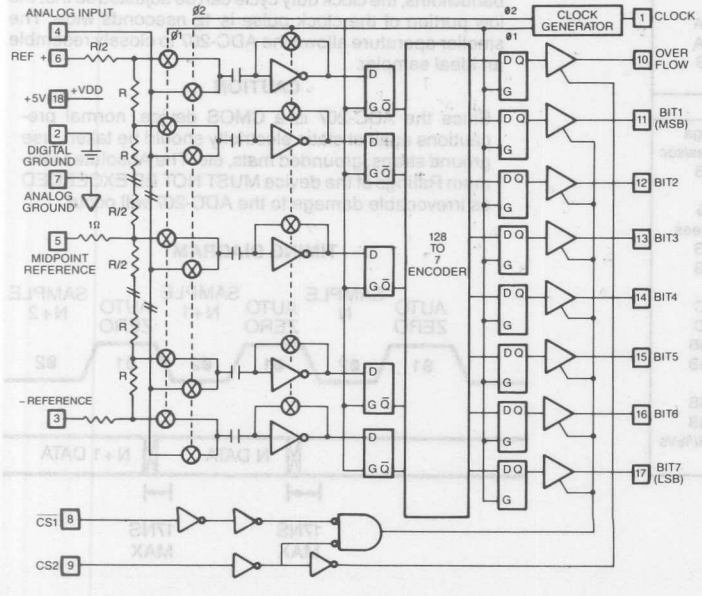
MECHANICAL DIMENSIONS



GENERAL DESCRIPTION

The ADC-207 is the industry's first 7-bit flash converter using a high-speed 1.2 micron CMOS process. This process offers some very distinctive advantages over other processes, making the ADC-207 a very unique device. The smaller geometrics of the process achieves high-speed, better linearity and better temperature performance. Since the ADC-207 is a CMOS device, it also has very low power consumption (250 mW). The device draws power from a single +5V supply, and is conservatively rated for 20 MHz operation. The ADC-207 allows using sampling apertures as small as 12nS, making it more closely approach an ideal sampler. The small sampling apertures also let the device operate at greater than 20 MHz.





INPUT/OUTPUT CONNECTIONS

DIP PINS	FUNCTION	LCC PINS
1	CLOCK IN	1
2	DIGITAL GROUND	4
3	-REFERENCE	5
4	ANA/DIG INPUT	6
5	MIDPOINT	7
6	+ REFERENCE	8
7	ANALOG GROUND	9
8	CS1	11
9	CS2	12
10	OVERFLOW	13
11	BIT 1 (MSB)	14
12	BIT 2	16
13	BIT 3	17
14	BIT 4	19
15	BIT 5	20
16	BIT 6	21
17	BIT 7	23
18	+VDD	24

FUNCTIONAL SPECIFICATIONS

(Typical at +5Vdc power, +25 deg. C, 20 MHz clock, +Reference = 5V, −Reference = Ground, unless noted)

DESCRIPTION	MIN.	TYPICAL	MAX.	UNITS
ABSOLUTE MAXIMUM RATINGS				
Power supply voltage (+Vdd, pin 18)	−0.5	—	+7.0	V dc
Digital inputs	−0.5	—	+5.5	V dc
Analog input	−0.5	—	+Vdd +0.5	V dc
Reference inputs	−0.5	—	+Vdd	V dc
Digital outputs (short circuit protected to ground)	−0.5	—	+5.5	V dc
Lead temperature, 10 sec. ma	—	—	+300	°C
Ambient temperature	−65	—	+150	°C
INPUTS				
ANALOG SIGNAL INPUT single-ended, non-isolated				
Input range dc-20 MHz	0	—	+5.0	V
Input impedance	—	1000	—	Ohms
Input capacitance, full input range	—	10	—	pF
DIGITAL INPUTS:				
Logic "1" level	2.0	—	—	V
Logic "0" level	—	—	0.8	V
Logic "1" loading	—	+/−1	+/−5	microamps
Logic "0" loading	—	+/−1	+/−5	microamps
Sample pulse width, during sampling portion of clock	12	—	—	nS
Reference ladder resistance	—	330	—	Ohms
DIGITAL OUTPUTS				
Data coding	Straight binary			
Data output resolution	7	—	—	
Logic "1" level	3.2	4.5	—	V
Logic "0" level at 1.6 mA	—	—	0.4	V
Logic "1" loading	4	—	—	mA
Logic "0" loading	4	—	—	mA
Output data valid delay from rising edge	—	15	17	nS
PERFORMANCE				
Conversion rate[1]	20	35	—	mega samples/sec
Harmonic distortion[2] (8 MHz 2nd order harmonic)	—	−40	—	dB
Differential gain[3]	—	3	—	%
Differential phase[3]	—	1.5	—	degrees
Aperture delay	—	8	—	nS
Aperture jitter	—	50	—	pS
No missing codes				
MC grade	0	—	+70	°C
MM grade	−55	—	+125	°C
Integral linearity at 25°C	—	+/−0.8	+/−1	LSB
Adjustable over temp. range	—	+/−1.0	—	LSB
Differential nonlinearity at 25°C	—	+/−0.3	+/−0.5	LSB
Over temp. range	—	+/−0.4	+/−0.6	LSB
Power supply rejection	—	0.02	—	%FSR/%Vs

DESCRIPTION	MIN.	TYPICAL	MAX.	UNITS
POWER REQUIREMENTS				
Power supply range (+Vdd)	+3.0	+5.0	+5.5	V dc
Power supply current	—	+50	+70	mA
Power dissipation	—	250	385	mW
ENVIRONMENTAL — MECHANICAL				
Operating temp. range:				
LC/MC Versions	0	—	+70	°C
MM/LM/883 Versions	−55	—	+125	°C
Storage temp. range	−65	—	+150	°C
Package type				
DIP	18-pin hermetic sealed, ceramic DIP			
LCC	24-pin hermetic sealed, ceramic LCC			
Pin material	.010 x .018 inch Kovar			

NOTES: 1. At full power input and chip selects enabled

2. At 4 MHz input and 20 MHz clock

3. For 10-step, 40 IRE NTSC ramp test

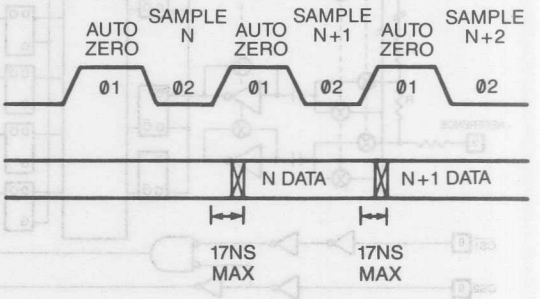
TECHNICAL NOTES

1. Input Buffer Amplifier—Since the ADC-207 has a switched capacitor type input, the input impedance of the 207 is dependent on the clock frequency. At relatively slow conversion rates a general purpose type input buffer can be used; at high coversion rates DATEL recommends either the HA-5033, the LH-0033 or Elantec 2003. See Figure 2 for typical connections.
2. Reference Ladder—Adjusting the voltage at +Ref adjusts the gain of the ADC-207. Adjusting the voltage at −Ref adjusts the offset or zero of the ADC-207. The midpoint pin is usually bypassed to ground through a .1uf capacitor, although it can be tied to a precision voltage halfway between +Ref and -Ref. This would improve integral linearity beyond 7 bits.
3. Clock Pulse Width—To improve performance at Nyguist bandwidths, the clock duty cycle can be adjusted so that the low portion of the clock pulse is 12 nseconds wide. The smaller aperature allows the ADC-207 to closely resemble an ideal sampler.

CAUTION

Since the ADC-207 is a CMOS device, normal precautions against static electricity should be taken. use ground straps, grounded mats, etc. The Absolute Maximum Ratings of the device MUST NOT BE EXCEEDED as irrevocable damage to the ADC-207 will occur.

TIMING DIAGRAM



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OUTPUT CODING

(+Ref=+5.12V, −Ref=Gnd, MID POINT=no connection)

NOTE: The reference should be held to 0.1% accuracy or better. Do not use the +5V power supply as a reference input without precision regulation and high frequency decoupling.

Values shown here are for a 5.12Vdc reference. Scale other references proportionally. Calibration equipment should test for code changes at the midpoints between these center values shown in Table 1. For example, at the half-scale major carry, set the input to 2.54V and adjust the reference until the code flickers equally between 63 and 64. Note also that the weighting for the comparator resistor network leaves the first and last thresholds to within ½ LSB of the end points to adjust the code transition to the proper midpoint values.

Table 1. ADC-207 Output Coding

Analog In (Center Value)	Code	Overflow	1 MSB	2	3	4	5	6	7 LSB	Decimal	Hexadecimal (incl. 0V)
0.00V	Zero	0	0	0	0	0	0	0	0	0	00
+0.04V	+1 LSB	0	0	0	0	0	0	0	1	1	01
+1.28V	+1/4 FS	0	0	1	0	0	0	0	0	32	20
+2.52V	+1/2FS−1 LSB	0	0	1	1	1	1	1	1	63	3F
+2.56V	+1/2FS	0	1	0	0	0	0	0	0	64	40
+2.60V	+1/2FS +1 LSB	0	1	0	0	0	0	0	1	65	41
+3.84V	+3/4FS	0	1	1	0	0	0	0	0	96	60
+5.08V	+FS	0	1	1	1	1	1	1	1	127	7F
+5.12V	Overflow	1	1	1	1	1	1	1	1	255*	FF

* — Note that the overflow code does not clear the data bits.

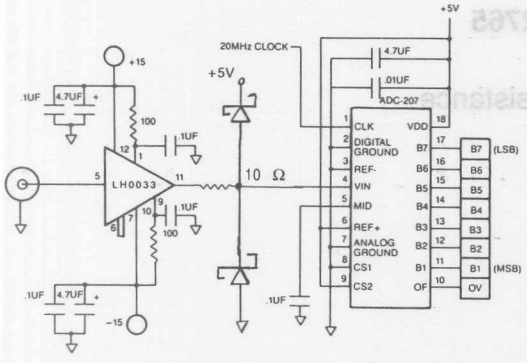


Figure 2. Typical Connections for Using the ADC-207

CHIP SELECT

The 3-state buffer has two enable lines, $\overline{CS1}$ and CS2. Table 2 shows the truth table for chip select signals. $\overline{CS1}$ has the function of enabling/disabling bits 1 through 7. CS2 has the function of enabling/disabling bits 1 through 7 and the overflow bit. Also a full-scale input produces all ones, including the overflow bit at the output.

Table 2. Chip Select Truth Table

$\overline{CS1}$	CS2	Bits 1-7	Overflow Bit
0	0	3 State Mode	3 State Mode
1	0	3 State Mode	3 State Mode
0	1	DATA Outputed	DATA Outputed
1	1	3 State Mode	DATA Outputed

ORDERING INFORMATION

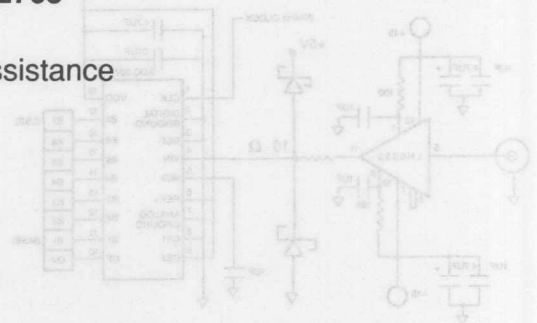
MODEL	TEMP. RANGE	PACKAGE
ADC-207MC	0 to +70 °C	18-pin DIP
ADC-207MM	-55 to +125 °C	18-pin DIP
ADC-207/883B	-55 to +125 °C	18-pin DIP
ADC-207LC	0 to +125 °C	24-pin LCC
ADC-207LM	-55 to +125 °C	24-pin LCC
ADC-207L/883B	-55 to +125 °C	24-pin LCC

ACCESSORIES

ADC-B207/208 Evaluation Board (without ADC-207)

Contact DATEL for your
Data Acquisition component
needs.

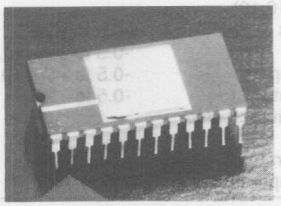
Dial
1-800-233-2765
for
Applications Assistance



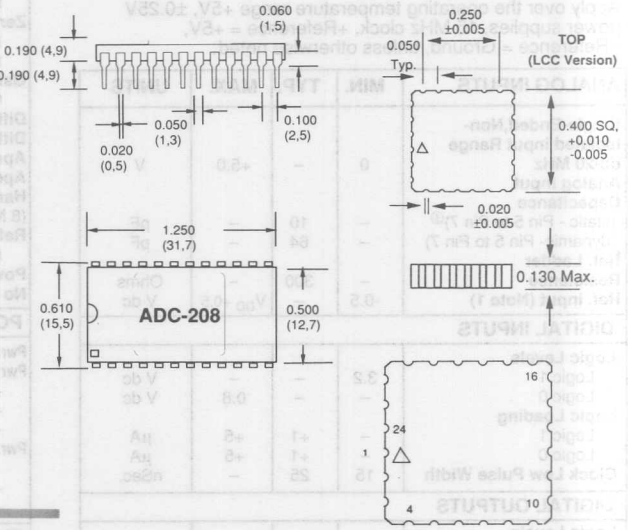
ADC-208
8-bit, 20 Msps Cmos Flash A/D

FEATURES

- 8-Bit flash A/D converter
- 20 MHz sampling rate
- 10 MHz full-power bandwidth
- Sample-hold not required
- Low power CMOS
- +5V dc operation
- 1.2 Micron CMOS
- 8-Bit latched three-state outputs with overflow bit
- Surface mount versions
- MIL-STD-883B versions
- No missing codes



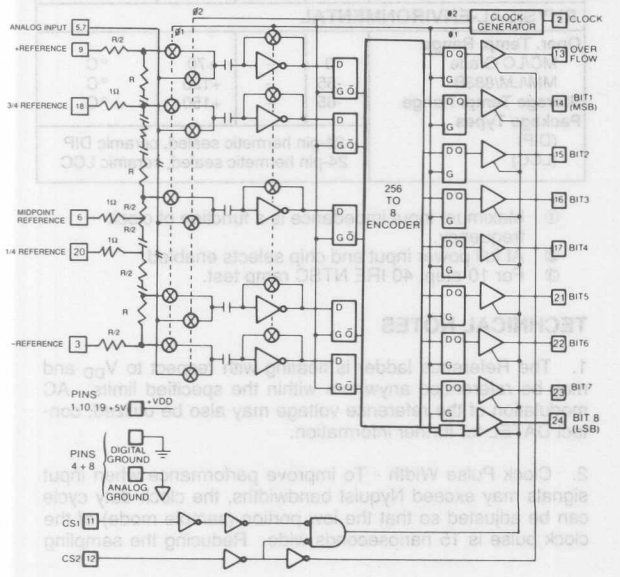
ADC-208 DIP ADC-208 LCC



GENERAL DESCRIPTION

The ADC-208 utilizes an advanced VLSI 1.2 micron CMOS in providing 20 MHz sampling rates at 8-bits. The flexibility of the design architecture and process delivers effective bit rates to 30 MHz in the burst mode, one shot mode conversion times of 35 nanoseconds, low power modes to 150 mW, latch-up free operation without external components and operation over the full military temperature range.

The ADC-208 has 256 auto-zeroing comparators which are auto-balanced on every conversion to cancel out any offsets due to temperature and/or dynamic effects. These comparators sample the difference between the analog input and the reference voltages generated by the precision reference ladder network. Parallel output data and the overflow pin have Three-State outputs. The overflow pin allows cascading two devices for 9-bit operation.



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	VDD
2	CLOCK
3	-REFERENCE
4	ANA/DIG GND (VSS)
5	ANALOG INPUT
6	REFERENCE MID-POINT
7	ANALOG INPUT
8	ANA/DIG GND (VSS)
9	+REFERENCE
10	VDD
11	CS1 (OUTPUT ENABLE)
12	CS2 (OVERFLOW ENABLE)
13	OVERFLOW BIT
14	BIT 1 (MSB)
15	BIT 2
16	BIT 3
17	BIT 4
18	REF 3/4 FS
19	VDD
20	REF 1/4 FS
21	BIT 5
22	BIT 6
23	BIT 7
24	BIT 8 (LSB)

ABSOLUTE MAXIMUM RATINGS

DESCRIPTION	LIMITS	UNITS
Power Supply Voltage (V_{DD} Pin 1,10,19)	-0.5 to +7.0	V dc
Digital Inputs	-0.5 to +5.5	V dc
Analog Input	-0.5 to +V_{DD} +0.5	V dc
Reference Inputs	-0.5 to +V_{DD} +0.5	V dc
Digital Outputs (short circuit protected to ground)	-0.5 to +5.5	V dc
Lead Temperature(10 sec)	+300 max.	°C
Storage Temperature	-65 to +150	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range +5V, ±0.25V power supplies, 15 MHz clock, +Reference = +5V, –Reference = Ground, unless otherwise noted.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Single-Ended,Non-Isolated Input Range				
dc-20 MHz	0	–	+5.0	V
Analog Input Capacitance				
(static - Pin 5 to Pin 7)①	–	10	–	pF
(dynamic- Pin 5 to Pin 7)	–	64	–	pF
Ref. Ladder Resistance	–	300	–	Ohms
Ref. input (Note 1)	-0.5	–	V_{DD} +0.5	V dc
DIGITAL INPUTS				
Logic Levels				
Logic 1	3.2	–	–	V dc
Logic 0	–	–	0.8	V dc
Logic Loading				
Logic 1	–	+1	+5	µA
Logic 0	–	+1	+5	µA
Clock Low Pulse Width	15	25	–	nSec.
DIGITAL OUTPUTS				
Logic Levels				
Logic 1	–	4.5	5.0	V dc
Logic 0	–	–	0.4	V dc
Logic Loading				
Logic 1	4	–	–	mA
Logic 0	4	–	–	mA
Output Data Valid Delay from Rising Clock Edge				
99% probability	5	10	15	nSec.
100% probability				
+25 °C	5	10	25	nSec.
-55 °C to +125 °C	–	–	40	nSec
Coding	Straight Binary			
Resolution	8 Bits			
PERFORMANCE				
Sampling Rate.②	15	20	–	MSPS
Full Power Bandwidth	10	–	–	MHz
Diff. Linearity at +25 °C (See Tech, Note 4)				
Code Transitions	–	±0.5	±1.0	LSB
Center of Codes	–	±0.25	–	LSB
Diff. Lin. Over Temp.				
Code Transitions	–	±0.5	±1.0	LSB
Center of Codes	–	±0.25	–	LSB

PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Int. Lin. at +25 °C (See Tech. Note 4) (Ref. adjusted)				
End-point	–	–	±1/2	LSB
Best-fit Line	–	–	±1/2	LSB
Int. Lin. Over Temp. (Ref. adjusted)				
Best-fit Line	–	±1/2	±1	LSB
Int. Lin. at +25 °C (Ref. unadjusted)				
End-point	–	±2	±2.5	LSB
Best-fit Line	–	±1.6	±1.9	LSB
Int. Lin. Over Temp. (Ref. unadjusted)				
End-point	–	±2.3	±2.6	LSB
Best-fit Line	–	±1.8	±2.0	LSB
Zero-Scale Offset (Code "0" to "1" transition)	–	±2.5	±4	LSB
Gain Error, +25 °C	–	±1	±1.75	LSB
Over temp.	–	±1.5	±2.5	LSB
Differential Gain③	–	2	–	%
Differential Phase③	–	1.1	–	degree
Aperture Delay	–	8	–	nSec.
Aperture Jitter	–	50	–	pSec.
Harmonic Distortion (8 MHz 2nd Order Harm.)	-40	-46	–	dB
Ref. Bandwidth (See Tech. Note 1)	–	10	–	MHz
Power Supply Rej.	–	0.02	0.05	%FSR/%/Vs
No Missing Codes	Over the operating temperature range			
POWER REQUIREMENTS				
Pwr. Supply Range (+V_{DD})	+3.5	+5.0	+5.5	V dc
Pwr. Supply Current				
+25 °C	–	+120	+145	mA
+125 °C	–	+100	+125	mA
-55 °C	–	+135	+160	mA
Pwr. Dissipation				
+25 °C	–	660	725	mW
+125 °C	–	550	690	mW
-55 °C	–	745	880	mW
PHYSICAL-ENVIRONMENTAL				
Oper. Temp. Range				
MC/LC Grade	0	–	+70	°C
MM/LM/883B	-55	–	+125	°C
Storage Temp. Range	-65	–	+150	°C
Package Types				
(DIP)	24-pin hermetic sealed, ceramic DIP			
(LCC)	24-pin hermetic sealed, ceramic LCC			

① Maximum input impedance is a function of clock frequency.
② At full power input and chip selects enabled.
③ For 10-step, 40 IRE NTSC ramp test.

TECHNICAL NOTES

1. The Reference ladder is floating with respect to V_{DD} and may be referenced anywhere within the specified limits. AC modulation of the reference voltage may also be utilized; contact DATEL for further information.

2. Clock Pulse Width - To improve performance when input signals may exceed Nyquist bandwidths, the clock duty cycle can be adjusted so that the low portion (sample mode) of the clock pulse is 15 nanoseconds wide. Reducing the sampling

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Table 1. ADC-208 Output Coding

ANALOG INPUT	CODE	OVER FLOW	DATA 1234	BITS 5678	DECIMAL	HEX
0.00 V	Zero	0	0000	0000	0	00
+0.02 V	+1 LSB	0	0000	0001	1	01
+1.28 V	+1/4 FS	0	0100	0000	64	40
+2.54 V	+1/2 FS-1 LSB	0	0111	1111	127	7F
+2.56 V	+1/2 FS	0	1000	0000	128	80
+2.58 V	+1/2 FS+1 LSB	0	1000	0001	129	81
+3.84 V	+3/4 FS	0	1100	0000	192	C0
+5.10 V	+FS	0	1111	1111	255	FF
+5.12 V	Overflow	1	1111	1111	511*	1FF

* Note the overflow code does not clear the data bits.
Values shown here are for a +5.12Vdc reference. Scale other references proportionally.
(+REF = +5.12V, -REF = GND, 1/4,1/2, and 3/4 Reference FS = No Connection)

time period minimizes the amount the input voltage slews and prevents the comparators from saturating.

3. The parallel output data and Overflow pin become available at the three-state buffer output when enabled. A full-scale input produces all "1"s on the data outputs. The OVERFLOW pin goes "high" when the analog input level exceeds + REF minus 1/2 LSB. Table 2 shows the truth table for the chip select enable signals.

4. DATEL uses the conservative definitions when specifying Integral Linearity (end-point) and Differential Linearity (code transition). The specifications using the less conservative definition have also been provided as a comparative specification for products specified this way.

5. The process that is used to fabricate the ADC-208 eliminates the latchup phenomena that has plagued CMOS devices in the past. The ADC-208 does not require external protection diodes.

CALIBRATION PROCEDURE

1. Connect the converter appropriately; a typical connection circuit is shown in Figure 2. Then apply an appropriate clock input. The ADC-208's reference input should be held to ±0.1% accuracy or better. Do not use the +5V power supply as a reference without precision regulation and high frequency decoupling capacitors.

2. Zero Adjustment
Apply a precision voltage reference source between the analog input (pins 5 & 7) and ground. Adjust the output of the reference source per Table 1 for the Unipolar Zero adjustment (+ 1/2 LSB). Adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 and 0000 0001. Ground -REFERENCE (pin 3) for operation without adjustment.

3. Full Scale Adjustment
Set the output of the voltage reference used in step 2 to the value shown in Table 1 for the Unipolar Gain Adjustment (+FS -1 1/2 LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1110 and 1111 1111. The + REFERENCE (pin 9) should be tied directly to a +5V reference for operation without adjustment.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 1.

5. Integral Nonlinearity Adjustments
Provision is made for optional adjustment of Integral Nonlinearity through access of the reference's 1/4, 1/2 & 3/4 Full Scale points. For example, at the half-scale major carry, set the input to 2.55V and adjust the reference until the code flickers equally between 127 and 128 for a 5.12V Full Scale input.

Table 2. Chip Select Truth Table

CS1	CS2	Bits 1-8	Overflow Bit
0	0	Tri-State Mode	Tri-State Mode
1	0	Tri-State Mode	Tri-State Mode
0	1	DATA Outputted	DATA Outputted
1	1	Tri-State Mode	DATA Outputted

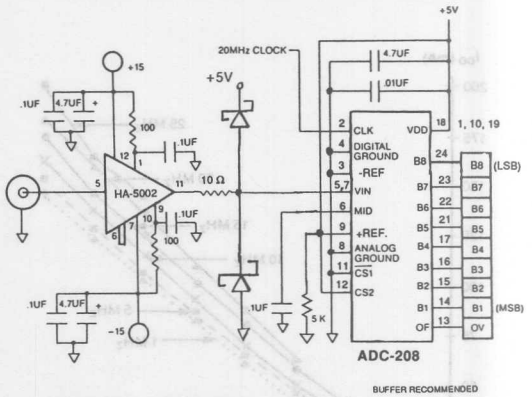
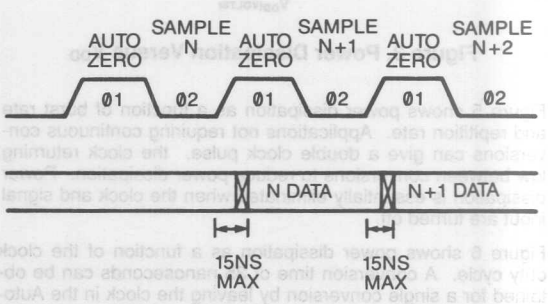


Figure 2. ADC-208 Typical Connections

NOTES:
Tie all V_{DD} pins (1,10, & 19) together. Tie both Analog Input pins (5 & 7) together. Connect both ANA/DIG GNDs (VSS pins 4 & 8) to one point, the ground plane beneath the converter.



Timing Diagram

LOW POWER MODES

Power Supply Aspect of Power Dissipation

Reduction of the V_{DD} power supply of the ADC-208 results in lower power dissipation. Refer to the curve of Figure 3 for power dissipation as a function of V_{DD}. The limiting factor is V_{DD} must be greater than the TTL or CMOS output levels. Interfacing to standard logic families presents little problem as the output drivers go to V_{DD} for a high state and to VSS for a low state.

BURST MODE

Applications can utilize an inherent system clock up to 30 MHz in the burst mode. The system clock can generate a one shot for a single conversion without requiring generation of a separate clock at a lower frequency.

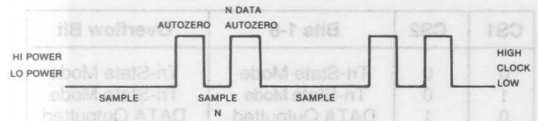


Figure 4. Burst Mode for Low Power

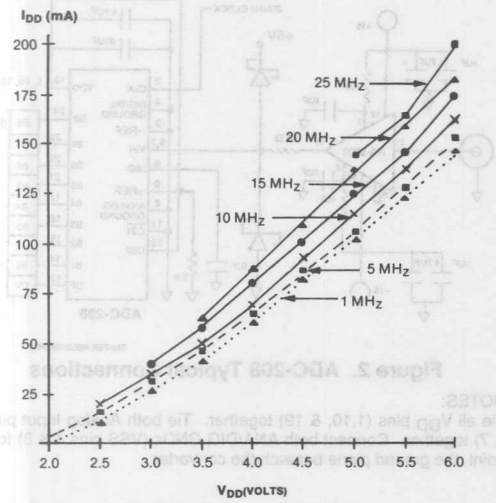


Figure 3. Power Dissipation Versus V_{DD}

Figure 5 shows power dissipation as a function of burst rate and repitition rate. Applications not requiring continuous conversions can give a double clock pulse, the clock returning low between conversions to reduce power dissipation. Power dissipation is essentially eliminated when the clock and signal input are turned off.

Figure 6 shows power dissipation as a function of the clock duty cycle. A conversion time of 35 nanoseconds can be obtained for a single conversion by leaving the clock in the Auto-zero mode. To initiate a conversion, the clock is put in the sample mode for 25 nanoseconds and then brought back high to the Auto-zero mode. Data is valid 15 nanoseconds after the clock goes high, eliminating the pipeline delay.

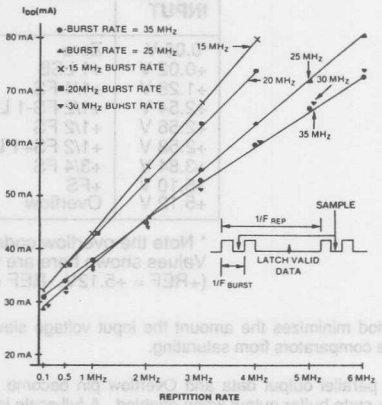


Figure 5. Power Dissipation vs. Burst Rate vs. Repetition Rate

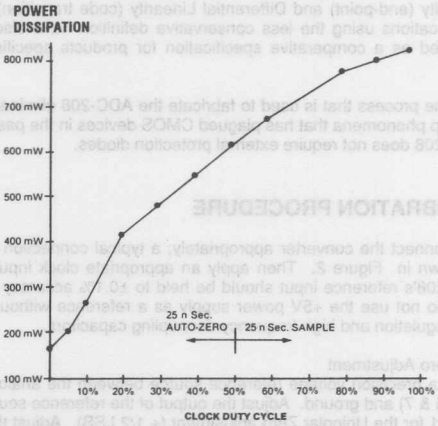


Figure 6. Power Dissipation vs. Duty Cycle for One-Shot Mode

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	PACKAGE
ADC-208MC	0 °C to +70 °C	24-pin DIP
ADC-208MM	-55 °C to +125 °C	24-pin DIP
ADC-208/883B	-55 °C to +125 °C	24-pin DIP
ADC-208LC	0 °C to +70 °C	24-pin LCC
ADC-208LM	-55 °C to +125 °C	24-pin LCC
ADC-208L/883B	-55 °C to +125 °C	24-pin LCC
ACCESSORIES		
ADC-B207/208	Evaluation Board (without ADC-208)	

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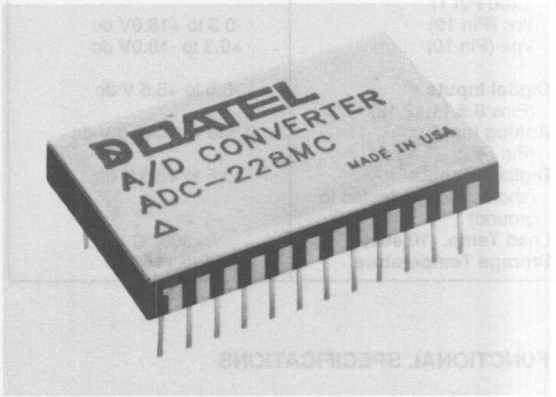
ADC-228
8-Bit, 20 MSPS Complete A/D Converter

FEATURES

- 8-Bit Flash A/D converter
- 20 MHz Sampling rate
- Complete support circuitry
- Low power, 1.5W
- 10 MHz Full power bandwidth
- Sample-hold not required
- Three-state outputs
- MIL-STD-883B versions



GENERAL DESCRIPTION

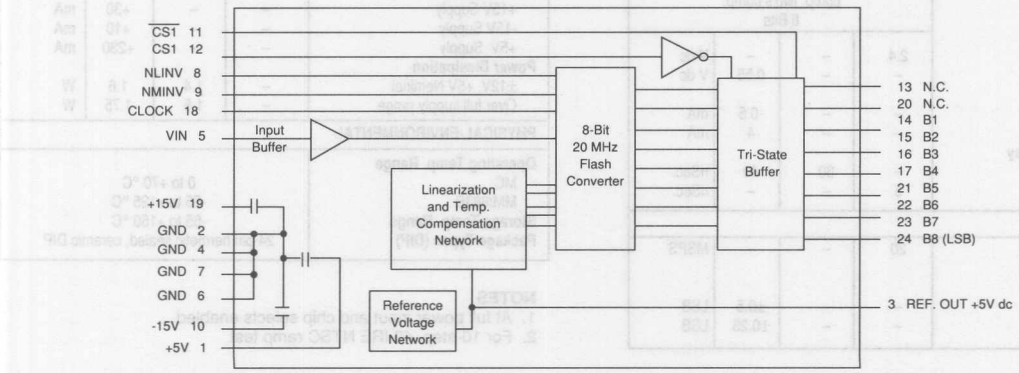
The ADC-228 combines analog front-end circuitry and a flash A/D converter to digitize high speed analog signals at a 20 mega samples per second rate. The ADC-228 contains an 8-bit, 20 MHz, flash A/D, a wideband analog input buffer, a precision voltage reference, temperature compensation circuitry, reference trims, and a three-state output buffer in a 24-pin package.

The ADC-228 offers significant savings by combining all of the circuitry in a single package. Valuable board real estate is saved, and design time and manufacturing costs are reduced to achieve these savings.

The ADC-228 is housed in a 24-pin hermetically sealed package and is available in the commercial, 0 to +70 °C, and military, -55 to +125 °C, temperature ranges. Operation is from ±15V and +5V dc power supplies.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+5V POWER IN	24	BIT 8
2	GROUND	23	BIT 7
3	±5V REF	22	BIT 6
4	GROUND	21	BIT 5
5	ANALOG INPUT	20	N/C
6	GROUND	19	+15V POWER IN
7	GROUND	18	CLOCK INPUT
8	NLINV	17	BIT 4
9	NLINV	16	BIT 3
10	-15V POWER IN	15	BIT 2
11	$\overline{CS1}$	14	BIT 41 (MSB)
12	CS1	13	N/C



ABSOLUTE MAXIMUM RATINGS

DESCRIPTION	PARAMETERS
Power Supply Voltage (VDD Pin 1)	-0.5 to+7.0 V dc
Vcc (Pin 19)	-0.3 to +18.0V dc
Vee (Pin 10)	+0.3 to -18.0V dc
Digital Inputs (Pins 8,9,11,12,18)	-0.5 to +5.5 V dc
Analog Input (Pin 5)	-0.5 to +Vdd+0.5 V dc
Digital Outputs (short circuit protected to ground)	-0.5 to +5.5 V dc
Lead Temp. (10 sec)	+300 °C
Storage Temperature	-65 to +150 °C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and ±15V dc and +5V dc power supply voltages unless otherwise specified (20 MHz clock).

DESCRIPTION	MIN	TYP	MAX	UNITS
ANALOG INPUTS				
Single-Ended, Non-Isolated Input Range dc-20 MHz	0	–	+5.0	Volts
Analog Input Resistance	2.45	2.5	2.55	Kohm
Analog Input Capacitance	–	5	–	pF
DIGITAL INPUTS				
Logic Levels				
Logic 1	2.0	–	–	V dc
Logic 0	–	–	0.8	V dc
Logic Loading				
Logic 1	–	–	160	µA
Logic 0	–	–	-0.5	mA
Clock Low Pulse Widths				
"high"	15	–	–	nSec.
"low"	15	–	–	nSec.
DIGITAL OUTPUTS				
Coding	straight bin., comp. bin. two's comp., comp. two's comp.			
Resolution	8 Bits			
Logic Levels				
Logic 1	2.4	–	–	V dc
Logic 0	–	–	0.55	V dc
Logic Loading				
Logic 1	–	–	-0.5	mA
Logic 0	–	–	4	mA
Output Data Valid Delay				
From Rising Edge	–	30	40	nSec.
Output Hold Time	5	–	–	nSec.
PERFORMANCE				
Sampling Rate (1)	20	–	–	MSPS
Differential Linearity (See Tech Note 4)				
(code transitions)	–	–	±0.5	LSB
(center of codes)	–	–	±0.25	LSB

PERFORMANCE CON'T.	MIN	TYP	MAX	UNITS
Integral Linearity +25 °C				
End-point	–	–	±0.5	LSB
Best-fit Line	–	–	±0.5	LSB
Over temperature				
End-point	–	–	±1.0	LSB
Best-fit Line	–	–	±0.75	LSB
Zero-Scale Offset (Code "0" to "1" Transition)				
(+25 °C)	–	–	±0.5	LSB
(-55 to +125 °C)	–	±0.5	±1.0	LSB
Gain error	–	±0.5	±1.0	LSB
Full Scale Absolute Accuracy	–	±0.5	±1.0	LSB
Differential Gain (2)	–	2	–	%
Differential Phase (2)	–	1	–	deg.
Aperture Delay	-5	–	+10	nSec.
Aperture Jitter	–	50	–	pSec.
No Missing Codes	Over the operating temperature range			
Power Supply Rejection	0.02 %FSR/%/Vs Maximum			
DYNAMIC PERFORMANCE				
Total Harm. Distort.,-0.5dB				
DC to 2.5 MHz	-53	-55	–	FS, -dB
2.5 MHz to 5 MHz	-48	-50	–	FS, -dB
5 MHz to 10 MHz	-36	-39	–	FS, -dB
Signal-to-Noise Ratio and Distortion,-0.5dB				
DC to 2.5 MHz	-45	-48	–	FS, -dB
2.5 MHz to 5 MHz	-44	-46	–	FS, -dB
5 MHz to 10 MHz	-35	-39	–	FS, -dB
Signal-to-Noise Ratio w/o Distortion,-0.5 dB				
DC to 2.5 MHz	-52	-55	–	FS, -dB
2.5 MHz to 5 MHz	-52	-55	–	FS, -dB
5 MHz to 10 MHz	-52	-55	–	FS, -dB
Effective Bits,-0.5dB				
DC to 2.5 MHz	7.5	7.75	–	Bits
2.5 MHz to 5 MHz	7.25	7.5	–	Bits
5 MHz to 10 MHz	6.75	7	–	Bits
Input Bandwidth				
Full Power Bandwidth (0Db)	10	–	–	MHz
Small Signal (-20dB)	20	–	–	MHz
POWER SUPPLY				
Power Supply Range				
+15V dc Supply	+11	+15	+15.75	Volts
-15V dc Supply	-11	-15	-15.75	Volts
+5V dc Supply	+4.75	+5	+5.25	Volts
Power Supply Current				
+15V Supply	–	–	+30	mA
-15V Supply	–	–	+10	mA
+5V Supply	–	–	+230	mA
Power Dissipation				
±12V, +5V Nominal	–	1.4	1.6	W
Over full supply range	–	1.5	1.75	W
PHYSICAL-ENVIRONMENTAL				
Operating Temp. Range				
MC	0 to +70 °C			
MM/883B	-55 to +125 °C			
Storage Temp. Range	-65 to +150 °C			
Package Types (DIP)	24-pin hermetic sealed, ceramic DIP			

NOTES
1. At full power input and chip selects enabled.
2. For 10-step, 40 IRE NTSC ramp test

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TECHNICAL NOTES

1. Rated performance requires using good high frequency techniques. The analog and digital grounds are connected internally. Avoid ground related problems by connecting the grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.
2. Bypass all the analog and digital supplies and the + reference (pin 3) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor.
3. DATEL uses the conservative definitions when specifying Integral Linearity (end-point) and Differential Linearity (code transition). The specifications using the less conservative definition have also been provided as a comparative specification for products specified this way.
4. Single conversions (one-shot mode) would require another clock edge to read out data. Users desiring to provide just a single clock pulse could use the circuit shown in Figure 2 to obtain the data.

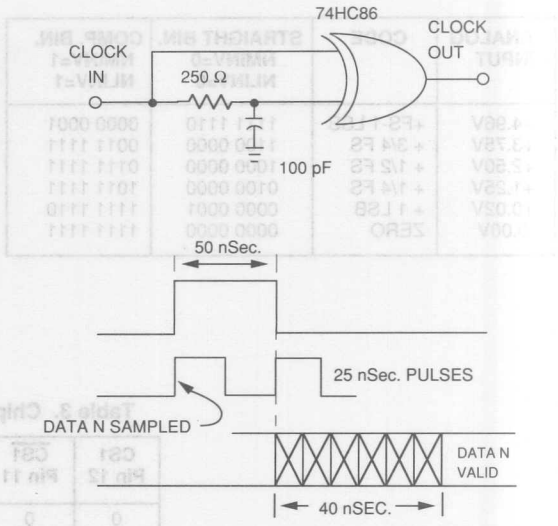


Figure 2. Single Clock Pulse Circuit and Operation

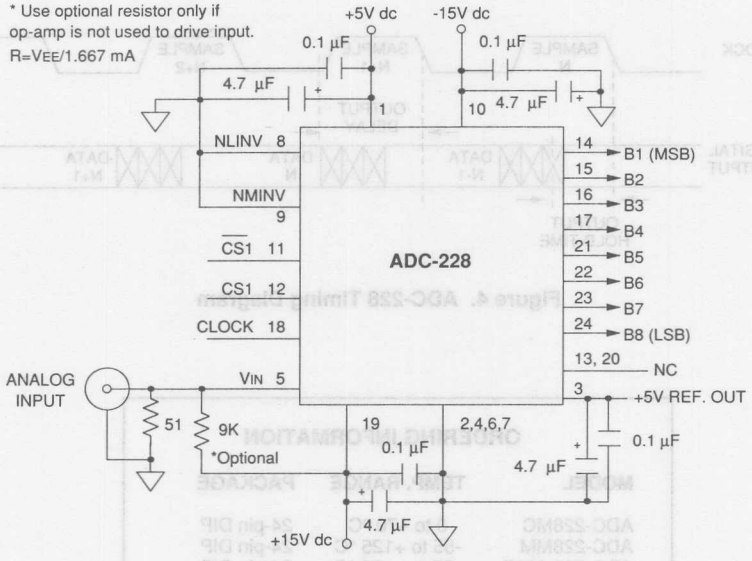


Figure 3. ADC-228 Typical Connections

Table 1. ADC-228 Unipolar Output Coding

ANALOG INPUT	CODE	STRAIGHT BIN. NMINV=0 NLINV=0	COMP. BIN. NMINV=1 NLINV=1
+4.96V	+FS-1 LSB	1111 1110	0000 0001
+3.75V	+ 3/4 FS	1100 0000	0011 1111
+2.50V	+ 1/2 FS	1000 0000	0111 1111
+1.25V	+ 1/4 FS	0100 0000	1011 1111
+0.02V	+ 1 LSB	0000 0001	1111 1110
0.00V	ZERO	0000 0000	1111 1111

Table 2. ADC-228 Bipolar Output Coding (Assumes analog input is externally offset)

ANALOG INPUT	CODE	TWO'S COMP. NMINV=1 NLINV=0	COMP. TWO'S COMP. NMINV=0 NLINV=1
+2.480V	+FS-1 LSB	0111 1111	1000 0000
+1.250V	+1/2 FS	0100 0000	1011 1111
+0.020V	+1 LSB	0000 0001	1111 1110
+0.000V	ZERO	0000 0000	1111 1111
-1.250V	-1/2 FS	1100 0000	0011 1111
-2.480V	-FS+1 LSB	1000 0001	0111 1110
-2.500V	-FS	1000 0000	0111 1111

Table 3. Chip Select Truth Table

CS1 Pin 12	$\overline{CS1}$ Pin 11	Bits 1-8
0	0	Three State Mode
0	1	Three State Mode
1	0	Data Outputted
1	1	Three State Mode

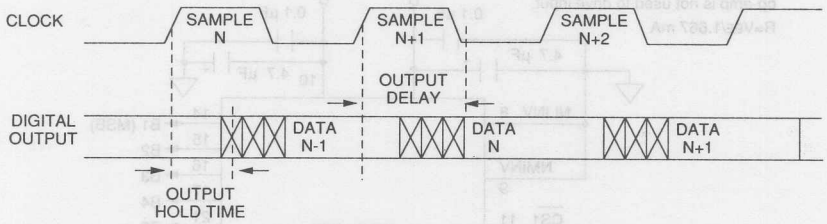


Figure 4. ADC-228 Timing Diagram

ORDERING INFORMATION

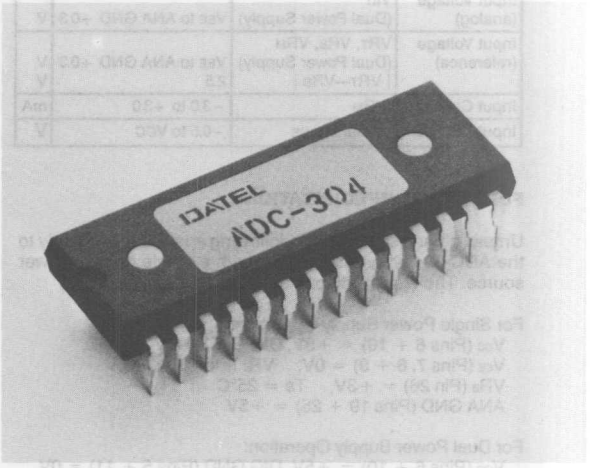
MODEL	TEMP. RANGE	PACKAGE
ADC-228MC	0 to +70 °C	24-pin DIP
ADC-228MM	-55 to +125 °C	24-pin DIP
ADC-228/883B	-55 to +125 °C	24-pin DIP

Receptacle for PC board mounting can be ordered through AMP Inc., part # 3-331272-8 (component lead socket), 24 required.

ADC-304
8-Bit, 20 MHz Low-Power, Flash A/D

FEATURES

- **8-Bit resolution**
- **± ½ LSB non-linearity**
- **20 MHz conversion rate**
- **8 MHz input bandwidth (-3 dB)**
- **Low-power consumption (390 mW)**
- **TTL-compatible**
- **Single or dual supply operation**



GENERAL DESCRIPTION

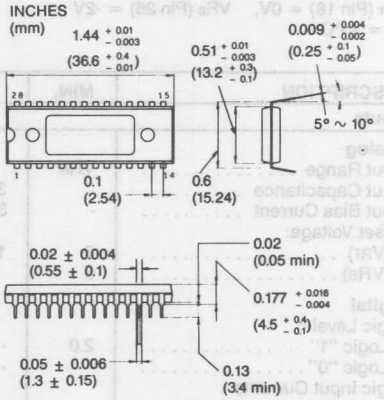
DATEL's ADC-304 is an 8-bit, 20 MHz analog-to-digital flash converter. The ADC-304 offers many performance features not obtainable from other flash A/D's.

Key features include a low-power dissipation of 390 mW and TTL compatible outputs. A wide analog input bandwidth of 8 MHz (-3 dB) allows operation without the need of a sample-hold. Also, single +5V supply operation is obtainable with an input range of +3 to +5V, eliminating the need for an additional power supply. A 0 to -2 V input range is available with ±5V supply operation.

Another novel feature of the ADC-304 is its user-selectable output coding. The MINV and LINV pins allow selection of binary, complementary binary, and if external offset circuitry is used for bipolar inputs, offset binary, two's complement, and complementary two's complement coding.

The ADC-304 is supplied in a 28-pin dual in-line package and operates over a -20°C to +75°C temperature range. Storage temperature range is from -65°C to +150°C.

MECHANICAL DIMENSIONS



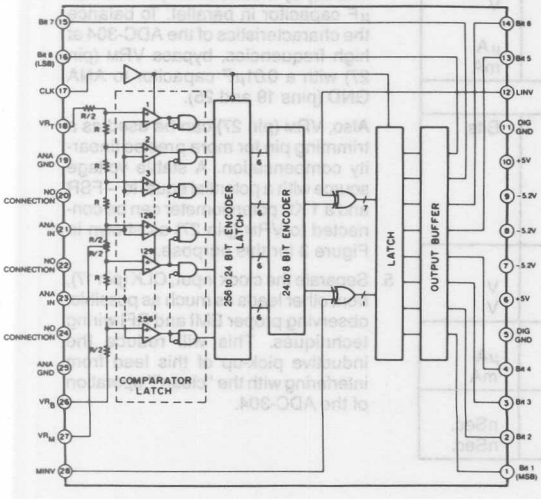


Table 1. ADC-304 Input/Output Connections

Pin	Function	Pin	Function
1	BIT 1 OUT (MSB)	15	BIT 7 OUT
2	BIT 2 OUT	16	BIT 8 OUT (LSB)
3	BIT 3 OUT	17	CLOCK INPUT
4	BIT 4 OUT	18	VRT
5	DIG GND	19	ANA GND
6	+5V POWER (VCC)	20	NO CONNECTION
7	−5.2V POWER (VEE)	21	ANA IN
8	−5.2V POWER (VEE)	22	NO CONNECTION
9	−5.2V POWER (VEE)	23	ANA IN
10	+5V POWER (VCC)	24	NO CONNECTION
11	DIG GND	25	ANA GND
12	LINV	26	VRB
13	BIT 5 OUT	27	VRM
14	BIT 6 OUT	28	MINV

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)			
Supply Voltage	V_{CC}-GND V_{EE}-GND	0 to +6 0 to −6	V V
Input Voltage (analog)	Vin (Dual Power Supply)	V_{EE} to ANA GND +0.3	V
Input Voltage (reference)	V_{RT}, V_{RB}, V_{RM} (Dual Power Supply) | V_{RT}—V_{RB} |	V_{EE} to ANA GND +0.3 2.5	V V
Input Current	I_{VRM}	−3.0 to +3.0	mA
Input Voltage	Digital Inputs	−0.5 to V_{CC}	V

FUNCTIONAL SPECIFICATIONS

Unless otherwise noted, the following specifications apply to the ADC-304 when used either with a single or dual power source. The test conditions are:

For Single Power Supply Operation:
V_{CC} (Pins 6 + 10) = +5V, DIG GND = 0V
V_{EE} (Pins 7, 8 + 9) = 0V, V_{RT} (Pin 18) = +5V
V_{RB} (Pin 26) = +3V, Ta = 25°C
ANA GND (Pins 19 + 25) = +5V

For Dual Power Supply Operation:
V_{CC} (Pins 6 + 10) = +5V, DIG GND (Pins 5 + 11) = 0V
ANA GND = 0V, V_{EE} = -5V
V_{RT} (Pin 18) = 0V, V_{RB} (Pin 26) = -2V
Ta = 25°C

DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Inputs				
Analog				
Input Range	V_{RB}		V_{RT}	V
Input Capacitance	-	30	35	pF
Input Bias Current	-	50	100	μA
Offset Voltage:				
(V_{RT})	8	13	19	mV
(V_{RB})	0	5	11	mV
Digital				
Logic Levels:				
Logic "1"	2.0	-	-	V
Logic "0"	-	-	0.8	V
Logic Input Currents :				
Logic "1"	-	−100	0	μA
Logic "0"	-	−0.32	−0.5	mA
Outputs				
Resolution Output Coding	8 Straight Binary Complementary Binary 2's Complement Complementary 2's Complement			Bits
Logic levels:				
Logic "1"	2.7	3.4	-	V
Logic "0"	-	-	0.5	V
Logic Level Loading:				
Logic "1"	-	−500	-	μA
Logic "0"	-	-	3	mA
Output Data Delay				
(TDLH)	-	25	30	nSec.
(TDHL)	-	26	35	nSec.

TECHNICAL NOTES

1. DIG GND pins (5 and 11) and V_{CC} pins (6 and 10) connect to separate internal circuits within the ADC-304. Connect these pins to their respective PCB patterns.
2. Layout of the analog and digital sections should be separated to reduce interference from noise. To further guard against unwanted noise, it is recommended to bypass, as close as possible, the voltage supply pins (6,10) to their respective ground pins (5,11) with a 1 μF and a 0.01 μF ceramic disk capacitor in parallel.
3. The input capacitance of the analog input is much smaller than that of a typical Flash A/D Converter. It is necessary to use an amplifier with sufficient bandwidth and driving power. The analog input pins (21,23) are separated internally, so they should be connected together externally. If the ADC-304 is driven with a low- output impedance amplifier, parasitic oscillations may occur.

   These parasitic oscillations can be prevented by introducing a small resistance of 2 to 10Ω between the amplifier output and the ADC-304's A/D input. This resistance must be of very low value of inductance at high frequencies.

   Note that each of the analog input pins are divided in this manner with these resistances. Connect the driving amplifier as close as possible to the A/D input of the ADC-304.
4. The voltage between V_{RT} (pin 18) and V_{RB} (pin 26) is equivalent to the dynamic range of the analog input. Bypass V_{RB} to ANA GND (pins 19 and 25) by means of a 1 μF and 0.01 μF capacitor in parallel. To balance the characteristics of the ADC-304 at high frequencies, bypass V_{RM} (pin 27) with a 0.01μF capacitor to ANA GND (pins 19 and 25).

   Also, V_{RM} (pin 27) can be used as a trimming pin for more precise linearity compensation. A stable voltage source with a potential equal to −FSR and a 1 KΩ potentiometer can be connected to V_{RM} (pin 27) as shown in Figure 3 for this purpose.
5. Separate the clock input, CLK (pin 17), from other leads as much as possible, observing proper EMI and RFI wiring techniques. This will reduce the inductive pick-up of this lead from interfering with the "clean'" operation of the ADC-304.

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Performance	MIN.	TYP.	MAX.	UNITS
Conversion Rate[1]	20	-	-	MHz
Non-Linearity	-	-	±1/2	LSB
Differential Non-Linearity	-	-	±1/2	LSB
Differential Gain Error[2]	-	-	1.5	%
Differential Phase Error[2]	-	-	0.5	Degrees
Aperture Delay	5	7	9	nSec.
Aperture Jitter	-	30	-	pSec.
Clock pulse width: Tpw1	35	-	-	nSec.
Tpw0	10	-	-	nSec.
Reference Pin Current	-	15	18	mA
Reference Resistance (VRT to VRB)	-	130	-	ohms
Reference Input (Dual Supply)				
(VRT)	−0.1	0	+0.1	V
(VRB)	−1.8	−2.0	−2.2	V
Power Supply Requirements				
Single Power Supply				
Supply voltage				
(VCC)	4.75	-	5.25	V
(VEE)	-	0	-	V
Supply Current:				
(ICC + IEE)	-	71	88	mA
Power Dissipation	-	360	442	mW
Dual Power Supply				
Supply Voltage:				
(VCC)	4.75	5.0	5.25	V
(VEE)	−4.75	−5.2	−5.5	V
Supply Current				
(ICC)	-	10	14	mA
(IEE)	-	62	75	mA
Power Dissipation	-	390	440	mW
Physical/Environmental				
Operating Temperature	−20	-	+75	°C
Storage Temperature	−55	-	+150	°C

1. fin = 1 KHz, ramp
2. NTSC 40 IRE-modulated ramp, Fc = 14.3 MSPS

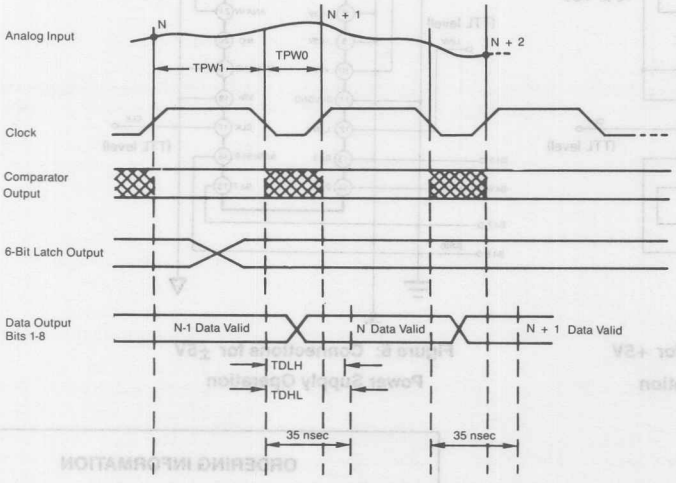

Figure 2: ADC-304 Timing Diagram

TECHNICAL NOTES (CONT.)

6. The analog input signal is sampled on the positive-going edge of CLK. Corresponding digital data appears at the output on the negative-going edge of the CLK pulse after a small delay of 35 nSec. maximum (TDLH, TDHL). Refer to the Timing diagram, Figure 4, for more information.
7. Connect all free pins to ANA GND (pins 19 and 25) to reduce unwanted noise.

The analog input range is equal to a 2V spread. The voltage on VRT-VRB will equal 2V. The connection of VRT and ANA GND is 2V higher than VRB. Whether using a single or dual power supply, the analog input will range from the value of VRT to VRB. If VRT equals +5V, then VRB will equal +3V and the analog input range will be from +5 to +3V.

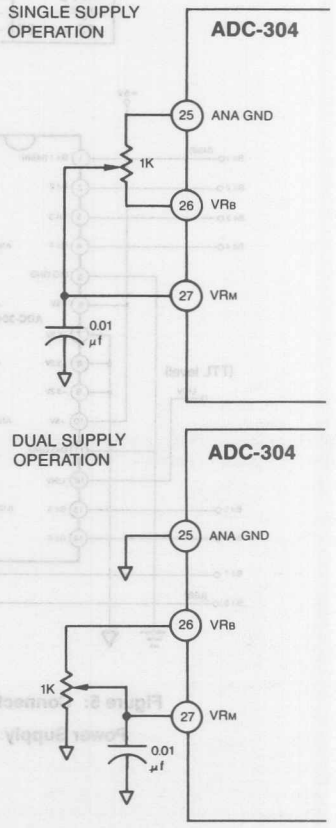

Figure 3: Improving Linearity Compensation

Table 2. Output Coding for +5V Power Supply Operation (+5 to +3V Signal Input)

		Straight Binary	Complement 2's Complement	2's Complement	Complement Binary
Unipolar Scale	MINV	0	0	1	1
	LINV	0	1	0	1
+FS – 1 LSB	+4.9922V	11111111	10000000	01111111	00000000
+⅞ FS	+4.7500V	11011111	10100000	01011111	00100000
+¾ FS	+4.5000V	10111111	11000000	00111111	01000000
+½ FS	+4.0000V	01111111	00000000	11111111	10000000
+¼ FS	+3.5000V	00111111	01000000	10111111	11000000
+⅛ FS	+3.2500V	00011111	00100000	11011111	11100000
+1 LSB	+3.0078V	00000001	01111110	10000001	11111110
Zero	+3.0000V	00000000	01111111	10000000	11111111

Table 3. Output Coding for ±5V Power Supply Operation (0 to –2V Signal Input)

		Straight Binary	Complement 2's Complement	2's Complement	Complement Binary
Unipolar Scale	MINV	0	0	1	1
	LINV	0	1	0	1
0	0V	11111111	10000000	01111111	00000000
–1 LSB	–7.813 mV	11111110	10000001	01111110	00000001
–⅛ FS	–250.00 mV	11011111	10100000	01011111	00100000
–¼ FS	–500.00 mV	10111111	11000000	00111111	01000000
–½ FS	–1.0V	01111111	00000000	11111111	10000000
–¾ FS	–1.5V	00111111	01000000	10111111	11000000
–⅞ FS	–1.75V	00011111	00100000	11011111	11100000
–FS + 1 LSB	–1.9922V	00000000	01111111	10000000	11111111

APPLICATION CIRCUITS

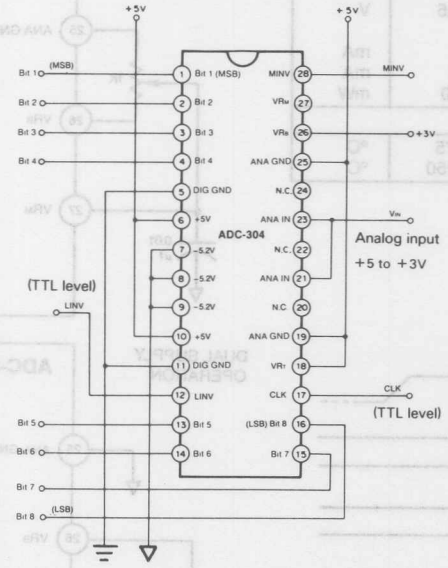

Figure 5: Connections for +5V Power Supply Operation

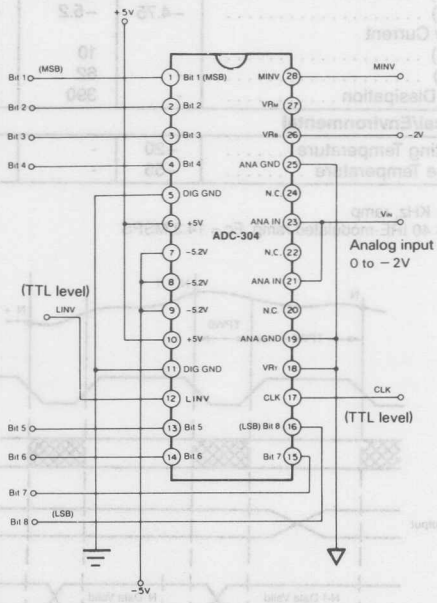

Figure 6: Connections for ±5V Power Supply Operation

ORDERING INFORMATION

MODEL	DESCRIPTION
ADC-304	8-bit, 20 MHZ, Low-power, flash A/D

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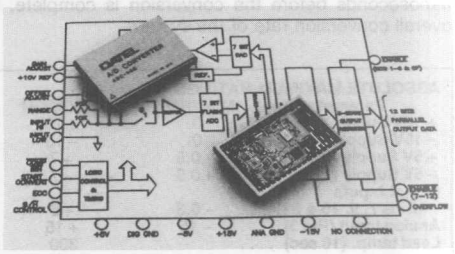
ADC-500, ADC-505

12-Bit, Ultra-Fast, Low-Power A/D Converters

FEATURES

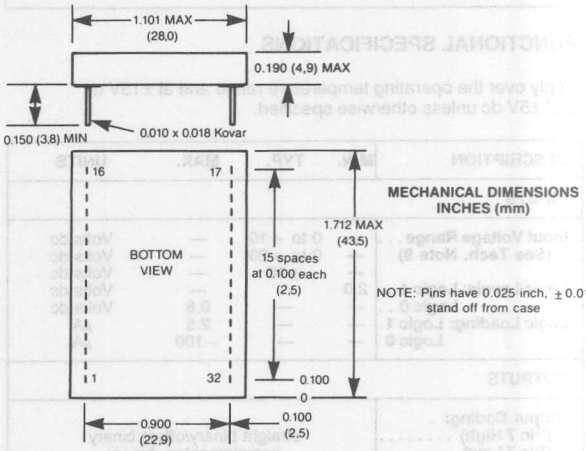
- **12-Bit resolution**
- **500 Nanosecond maximum conversion time**
- **Low-power, 1.6W**
- **Small initial errors**
- **Three-state output buffers**
- **-55°C to +125°C operation**
- **Small 32-pin DIP**
- **No missing codes**



GENERAL DESCRIPTION

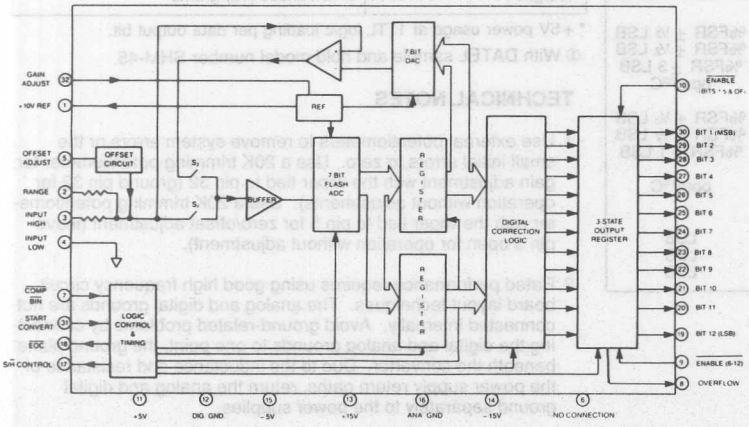
DATEL's ADC-500 and ADC-505 are 12-bit analog-to-digital converters which have small initial errors and can also provide adjustment capability for system errors. Both models have identical specifications except for conversion times. The ADC-505 has a maximum conversion time of 550 nanoseconds while the ultra-fast ADC-500 accomplishes a 12-bit conversion in less than 500 nanoseconds. Figure 1 is a simplified block diagram applicable to both devices.

Manufactured using thick-film and thin-film hybrid technology, these converters' remarkable performances are based upon a digitally-corrected subranging architecture. DATEL further enhances this technology by using a proprietary custom chip and unique laser trimming schemes. The ADC-500 and ADC-505 are packaged in a 32-pin ceramic DIP and consume 1.6 watts.



MECHANICAL DIMENSIONS INCHES (mm)

NOTE: Pins have 0.025 inch, ±0.01 stand off from case



INPUT/OUTPUT CONNECTIONS

PIN	SIGNAL NAME
1	+10V REF
2	RANGE
3	INPUT HIGH
4	INPUT LOW
5	OFFSET ADJUST
6	NO CONNECTION
7	COMP BIN
8	OVERFLOW
9	ENABLE (6-12)
10	ENABLE (1-5, O.F.)
11	+5V
12	DIGITAL GROUND
13	+15V
14	-15V
15	-5V
16	ANALOG GROUND
17	S/H CONTROL
18	EOC
19	BIT 12 (LSB)
20	BIT 11
21	BIT 10
22	BIT 9
23	BIT 8
24	BIT 7
25	BIT 6
26	BIT 5
27	BIT 4
28	BIT 3
29	BIT 2
30	BIT 1 (MSB)
31	START CONVERT
32	GAIN ADJUST

Another novel feature of the ADC-500 is the provision of a Sample/Hold control pin for applications where a sample-hold is used in conjunction with the ADC-500. This feature allows the sample-and-hold device to go back into the sample mode a minimum of 30 nanoseconds before the conversion is complete, improving the overall conversion rate of the system.

ABSOLUTE MAXIMUM RATINGS Parameters	MINIMUM	MAXIMUM	UNITS
+15V Supply (Pin 13)	0	+18	Volts dc
−15V Supply (Pin 14)	0	−18	Volts dc
+5V Supply (Pin 11)	−0.5	+7	Volts dc
−5V Supply (Pin 15)	+0.5	−7	Volts dc
Digital Inputs (Pins 7, 9, 10 & 31)	−0.3	+6	Volts dc
Analog Input (Pin 3)	−15	+15	Volts dc
Lead temp. (10 sec)		300	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and ±5V dc unless otherwise specified.

DESCRIPTION	MIN.	TYP.	MAX.	UNITS
INPUTS				
Input Voltage Range	—	0 to +10	—	Volts dc
(See Tech. Note 9)	—	0 to +20	—	Volts dc
	—	±10	—	Volts dc
Logic Levels: Logic 1	2.0	—	—	Volts dc
Logic 0	—	—	0.8	Volts dc
Logic Loading: Logic 1	—	—	2.5	μA
Logic 0	—	—	−100	μA
OUTPUTS				
Output Coding:				
(Pin 7 High)	straight binary/offset binary			
(Pin 7 Low)	complementary binary complementary offset binary			
Logic Levels: Logic 1	2.4	—	—	Volts dc
Logic 0	—	—	0.4	Volts dc
Logic Loading: Logic 1	—	—	−160	μA
Logic 0	—	—	6.4	mA
Internal Reference:				
Voltage, +25°C	9.98	10.0	10.02	Volts dc
Drift	—	±5	±30	ppm/°C
External Current	—	—	1.5	mA
PERFORMANCE				
Integral Nonlinearity:				
+25°C	—	—	±0.0125	%FSR ±½ LSB
0°C to +70°C	—	—	±0.0125	%FSR ±½ LSB
−55°C to +125°C	—	—	±0.0125	%FSR ±3 LSB
Integral Nonlin. Tempco.	—	±3	±8	ppm/°C
Differential Nonlinearity				
+25°C	—	—	±0.0125	%FSR ±½ LSB
0°C to +70°C	—	—	±0.0125	%FSR ±½ LSB
−55°C to +125°C	—	—	±0.0125	%FSR ±1 LSB
Differential Nonlin. Tempco	—	—	±2.5	ppm/°C
Full-Scale Absol. Accuracy:				
+25°C	—	±3	±8	LSB
0°C to +70°C	—	±4	±14	LSB
−55°C to +125°C	—	±8	±29	LSB

PERFORMANCE (cont.) DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Unipolar Zero Error, +25°C	—	±1	±3	LSB
Unipolar Zero Tempco	—	±13	±25	ppm/°C
Bipolar Zero Error, +25°C	—	±1	±3	LSB
Bipolar Zero Tempco	—	±13	±25	ppm/°C
Bipolar Offset Error, +25°C	—	±2	±5	LSB
Bipolar Offset Error Tempco	—	±17.5	±35	ppm/°C
Gain Error, +25°C	—	±2	±5	LSB
Gain Tempco	—	±17.5	±35	ppm/°C
Conversion Times:				
ADC-500				
+25°C	—	—	500	nsec.
0°C to +70°C	—	—	540	nsec.
−55°C to +125°C			560	nsec.
ADC-505				
+25°C	—	—	550	nsec.
0°C to +70°C	—	—	590	nsec.
−55°C to +125°C	—	—	620	nsec.
Harm. Distort. (-FS) ①				
+25 °C	-72 dB min.			
0 to +70 °C	-72 dB min.			
-55 to +125 °C	-65 dB min.			
No Missing Codes (12 Bits)	Over the Operating Temp. Range			
POWER SUPPLY REQUIREMENTS				
Power Supply Range:				
+15V dc Supply	+14.25	+15	+15.75	Volts dc
−15V dc Supply	−14.25	−15	−15.75	Volts dc
+5V dc Supply	+4.75	+5	+5.25	Volts dc
−5V dc Supply	−4.75	−5	−5.25	Volts dc
Power Supply Current:				
+15V Supply	—	+23	+30	mA
−15V Supply	—	−11	−15	mA
+5V Supply*	—	+55	+90	mA
−5V Supply	—	−175	−210	mA
Power Dissipation	—	1.6	1.8	Watts
Power Supply Rejection	—	—	0.01	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range:				
−BMC	0	—	+70	°C
−BMM	−55	—	+125	°C
Storage Temperature Range	−65	—	+150	°C
Package Type	32-pin hermetic sealed, ceramic DIP			
Pins	0.010 x 0.018 inch Kovar			
Weight	0.42 ounces (12) grams			

* +5V power usage at 1TTL logic loading per data output bit.

① With DATEL sample and hold model number SHM-45.

TECHNICAL NOTES

1. Use external potentiometers to remove system errors or the small initial errors to zero. Use a 20K trimming potentiometer for gain adjustment with the wiper tied to pin 32 (ground pin 32 for operation without adjustments). Use a 20K trimming potentiometer with the wiper tied to pin 5 for zero/offset adjustment (leave pin 5 open for operation without adjustment).

2. Rated performance requires using good high frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

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3. Bypass all the analog and digital supplies and the +10V reference (pin 1) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 1) to analog ground (pin 16). The -5V dc supply is treated as an analog supply and analog ground (pin 16) should be treated as its return path for decoupling purposes.

4. Obtain straight binary/offset binary output coding by tying COMP BIN (pin 7) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie the COMP BIN pin to ground. The COMP BIN signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

5. An overflow signal, pin 8, indicates when analog input signals are below or above the desired full-scale range. To overflow pin also has a three-state output and is enabled by pin 10 (Enable bits 1-5 & O.F.).

6. The Sample/Hold control signal, pin 17, goes low following the rising edge of START CONVERT pulse and high 30 nanoseconds minimum before EOC goes low. This indicates that the converter can accept a new analog input.

7. The drive requirements of the ADC-500/505 may be satisfied with a wide-bandwidth, low output impeance input source. Applications of these converters that require the use of a sample-hold may be satisfied by using DATEL's model SHM-45. Using this device with multiplexers or for test purposes will require an input buffer.

8. Over temperature, input capacitance is 50 pF maximum and input impedance is 1.75K minimum (2.5K typical) for unipolar and 3.75K minimum (5K typical) for bipolar. These values are guaranteed by design.

9. Requirements for ±2.5V inputs can be satisfied using DATEL's AM-1435 amplifier in front of the SHM-45/ADC-500 configuration, shown in Figure 3, at the appropriate gain. The SHM-45's gain of 2 mode allows 0 to +5V or ±5V input ranges.

TIMING

Figure 2 shows the relationship between the various input signals. The timing cited applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

TABLE 2. INPUT CONNECTIONS

INPUT VOLTAGE RANGE	INPUT PIN	CONNECT PIN 2 (RANGE) TO PIN:
0 to +10V dc	3	3
0 to +20V dc	3	16
±10V dc	3	1

TABLE 3. ZERO AND GAIN ADJUST

FSR	ZERO ADJUST +1/2 LSB	GAIN ADJUST +FS -1 1/2 LSB
0 to +10V dc	+1.22 mV	+9.9963V dc
0 to +20V dc	+2.44 mV	+19.9927V dc
±10V dc	+2.44 mV	+9.9927V dc

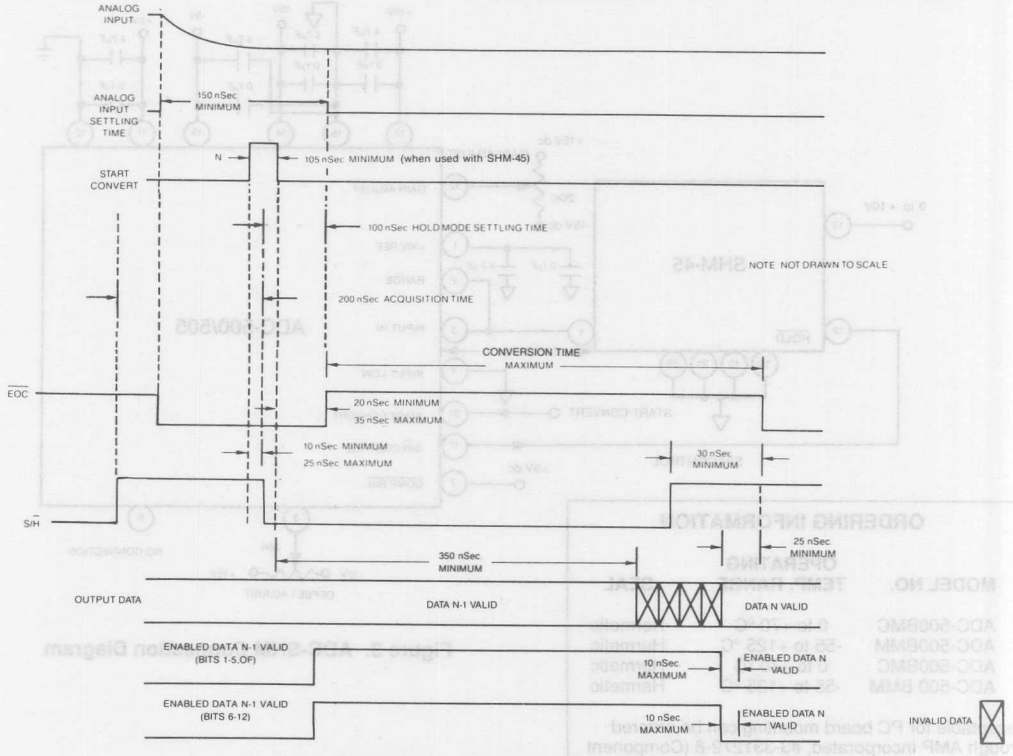

Figure 2. ADC-500/505 and SHM-45 Timing Diagram

CALIBRATION PROCEDURE

Removal of system errors or the small initial errors is accomplished as follows:

1. Connect the converter per Figure 3 and Table 2 for the appropriate full-scale range (FSR). Apply a pulse of 50 nanoseconds minimum to the START CONVERT input (pin 31) at a rate of 500 KHz. This rate chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments - Apply a precision voltage reference source between the analog input (pin 3) and ground (pin 16). Adjust the output of the reference source per Table 3. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with the COMP BIN (pin 7) tied high or between 1111 1111 1111 and 1111 1111 1110 with the COMP BIN tied low.

3. Full-Scale Adjustment - Set the output of the voltage reference used in step 2 to the value shown in Table 3. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for COMP BIN (pin 7) tied high or between 0000 0000 0001 and 0000 0000 0000 for COMP BIN tied low.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 4.

TABLE 4. OUTPUT CODING

			STRAIGHT BIN.		COMP. BINARY			
UNIPOLAR	INPUT RANGES, V dc		OUTPUT CODING				INPUT RANGE	BIPOLAR
SCALE	0 to +10V	0 to +20V	MSB	LSB	MSB	LSB	±10V dc	SCALE
+FS -1 LSB	+9.9976V	+19.9951V	1111 1111 1111		0000 0000 0000		+9.9951V	+FS -1 LSB
7/8 FS	+8.7500V	+17.500V	1110 0000 0000		0001 1111 1111		+7.5000V	+3/4 FS
3/4 FS	+7.5000V	+15.000V	1100 0000 0000		0011 1111 1111		+5.0000V	+1/2 FS
1/2 FS	+5.0000V	+10.000V	1000 0000 0000		0111 1111 1111		0.0000V	0
1/4 FS	2.5000V	+5.0000V	0100 0000 0000		1011 1111 1111		-5.0000V	-1/2 FS
1/8 FS	1.2500V	+2.5000V	0010 0000 0000		1101 1111 1111		-7.5000V	-3/4 FS
1 LSB	0.0024V	+0.0049V	0000 0000 0001		1111 1111 1110		-9.9951V	-FS +1 LSB
0	0.0000V	0.0000V	0000 0000 0000		1111 1111 1111		-10.000V	-FS
			OFF. BINARY		COMP. OFF. BIN.			

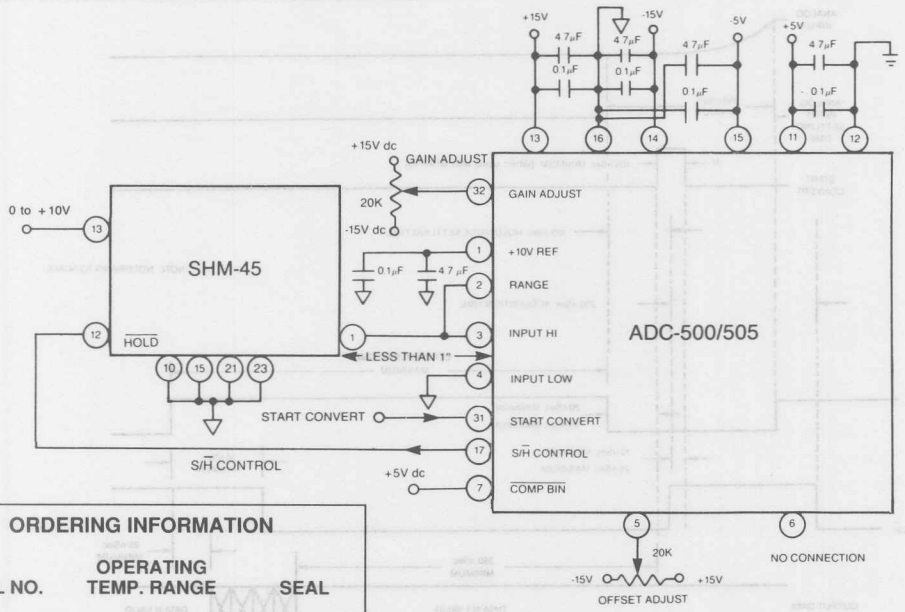

Figure 3. ADC-SHM Connection Diagram

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE	SEAL
ADC-500BMC	0 to +70 °C	Hermetic
ADC-500BMM	-55 to +125 °C	Hermetic
ADC-500BMC	0 to +70 °C	Hermetic
ADC-500 BMM	-55 to +125 °C	Hermetic

Receptable for PC board mounting can be ordered through AMP Incorporated, #3-331272-8 (Component Lead Socket), 32 required.

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ADC-508

12-Bit, Ultra-Fast, Low-Power A/D Converter

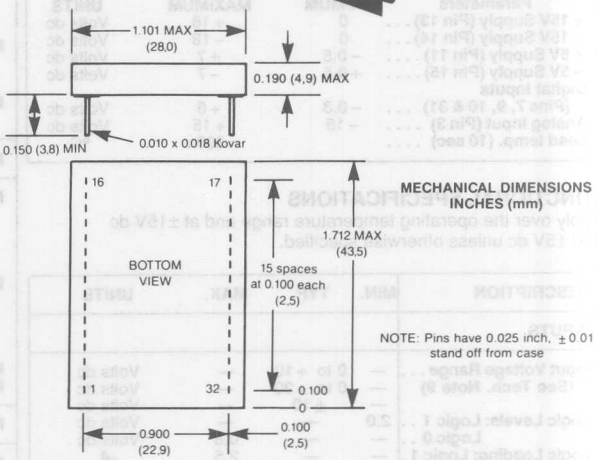
FEATURES

- **12-Bit resolution**
- **700 Nanosecond maximum conversion time**
- **Low-power, 1.6W**
- **Small initial errors**
- **Three-state output buffers**
- **-55°C to +125°C operation**
- **Small 32-pin DIP**
- **No missing codes**

GENERAL DESCRIPTION

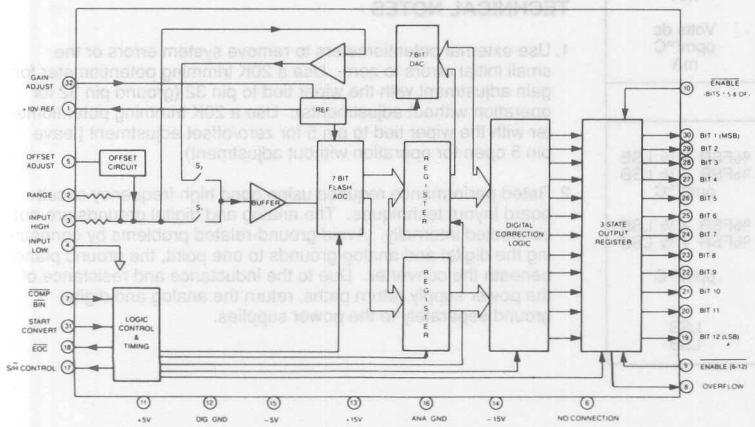
DATEL's ADC-508 is a 12-bit, analog-to-digital converter which has small initial errors and can also provide adjustment capability for system errors. The ADC-508 has a maximum conversion time of 700 nanoseconds. Figure 1 is a simplified block diagram.

Manufactured using thick-film and thin-film hybrid technology, this converter's remarkable performance is based upon a digitally-corrected subranging architecture. DATEL further enhances this technology by using a proprietary custom chip and unique laser trimming schemes. The ADC-508 is packaged in a 32-pin ceramic DIP and consumes 1.6 watts.



MECHANICAL DIMENSIONS INCHES (mm)

NOTE: Pins have 0.025 inch, ±0.01 stand off from case



INPUT/OUTPUT CONNECTIONS

PIN	SIGNAL NAME
1	+10V REF
2	RANGE
3	INPUT HIGH
4	INPUT LOW
5	OFFSET ADJUST
6	NO CONNECTION
7	COMP BIN
8	OVERFLOW
9	ENABLE (6-12)
10	ENABLE (1-5, O.F.)
11	+5V
12	DIGITAL GROUND
13	+15V
14	-15V
15	-5V
16	ANALOG GROUND
17	S/H CONTROL
18	EOC
19	BIT 12 (LSB)
20	BIT 11
21	BIT 10
22	BIT 9
23	BIT 8
24	BIT 7
25	BIT 6
26	BIT 5
27	BIT 4
28	BIT 3
29	BIT 2
30	BIT 1 (MSB)
31	START CONVERT
32	GAIN ADJUST

conjunction with the ADC-508. This feature allows the sample-and-hold device to go back into the sample mode a minimum of 30 nanoseconds before the conversion is complete, improving the overall conversion rate of the system.

Power required is ±15V dc and ±5V dc. Models are available in the commercial 0°C to +70°C, and military −55°C to +125°C operating temperature range. Typical applications include spectrum, transient, vibration, and waveform analysis. These devices are also ideally suited for radar, sonar and video digitization, medical instrumentation, and high-speed data acquisition systems. For information

ABSOLUTE MAXIMUM RATINGS Parameters	MINIMUM	MAXIMUM	UNITS
+15V Supply (Pin 13)	0	+18	Volts dc
−15V Supply (Pin 14)	0	−18	Volts dc
+5V Supply (Pin 11)	−0.5	+7	Volts dc
−5V Supply (Pin 15)	+0.5	−7	Volts dc
Digital Inputs (Pins 7, 9, 10 & 31)	−0.3	+6	Volts dc
Analog Input (Pin 3)	−15	+15	Volts dc
Lead temp. (10 sec)		300	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and ±5V dc unless otherwise specified.

DESCRIPTION	MIN.	TYP.	MAX.	UNITS
INPUTS				
Input Voltage Range	—	0 to +10	—	Volts dc
(See Tech. Note 9)	—	0 to +20	—	Volts dc
	—	±10	—	Volts dc
Logic Levels: Logic 1	2.0	—	—	Volts dc
Logic 0	—	—	0.8	Volts dc
Logic Loading: Logic 1	—	—	2.5	μA
Logic 0	—	—	−100	μA
OUTPUTS				
Output Coding:				
(Pin 7 High)		straight binary/offset binary		
(Pin 7 Low)		complementary binary complementary offset binary		
Logic Levels: Logic 1	2.4	—	—	Volts dc
Logic 0	—	—	0.4	Volts dc
Logic Loading: Logic 1	—	—	−160	μA
Logic 0	—	—	6.4	mA
Internal Reference:				
Voltage, +25°C	9.98	10.0	10.02	Volts dc
Drift	—	±5	±30	ppm/°C
External Current	—	—	1.5	mA
PERFORMANCE				
Integral Nonlinearity:				
+25°C	—	—	±0.0125	%FSR ±½ LSB
0°C to +70°C	—	—	±0.0125	%FSR ±½ LSB
Integral Nonlin. Tempco.	—	±3	±8	ppm/°C
Differential Nonlinearity				
+25°C	—	—	±0.0125	%FSR ±½ LSB
0°C to +70°C	—	—	±0.0125	%FSR ±½ LSB
Differential Nonlin. Tempco	—	—	±2.5	ppm/°C
Full-Scale Absol. Accuracy:				
+25°C	—	±3	±8	LSB
0°C to +70°C	—	±4	±14	LSB
Unipolar Zero Error, +25°C	—	±1	±3	LSB
Unipolar Zero Tempco	—	±13	±25	ppm/°C
Bipolar Zero Error, +25°C	—	±1	±3	LSB
Bipolar Zero Tempco	—	±13	±25	ppm/°C
Bipolar Offset Error, +25°C	—	±2	±5	LSB
Bipolar Offset Error Tempco	—	±17.5	±35	ppm/°C
Gain Error, +25°C	—	±2	±5	LSB
Gain Tempco	—	±17.5	±35	ppm/°C
Conversion Times: ADC-508				
+25°C	—	—	700	nsec.
0°C to +70°C	—	—	740	nsec.
Harm. Distort. (-FS) ①				
+25 °C		-72 dB min.		
0 to +70 °C		-72 dB min.		
No Missing Codes (12 Bits):		Over the Operating Temp. Range		
POWER SUPPLY REQUIREMENTS				
Power Supply Range:				
+15V dc Supply	+14.25	+15	+15.75	Volts dc
−15V dc Supply	−14.25	−15	−15.75	Volts dc
+5V dc Supply	+4.75	+5	+5.25	Volts dc
−5V dc Supply	−4.75	−5	−5.25	Volts dc
Power Supply Current:				
+15V Supply	—	+23	+30	mA
−15V Supply	—	−11	−15	mA
+5V Supply*	—	+55	+90	mA
−5V Supply	—	−175	−210	mA
Power Dissipation	—	1.6	1.8	Watts
Power Supply Rejection	—	—	0.01	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range: −BMC	0	—	+70	°C
Storage Temperature Range	−65	—	+150	°C
Package Type	32-pin hermetic sealed, ceramic DIP			
Pins	0.010 x 0.018 inch Kovar			
Weight	0.42 ounces (12) grams			

* +5V power usage at 1TTL logic loading per data output bit.

① With DATEL sample and hold model number SHM-45.

TECHNICAL NOTES

1. Use external potentiometers to remove system errors or the small initial errors to zero. Use a 20K trimming potentiometer for gain adjustment with the wiper tied to pin 32 (ground pin 32 for operation without adjustments). Use a 20K trimming potentiometer with the wiper tied to pin 5 for zero/offset adjustment (leave pin 5 open for operation without adjustment).

2. Rated performance requires using good high frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

3. Bypass all the analog and digital supplies and the +10V reference (pin 1) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 1) to analog ground (pin 16). The -5V dc supply is treated as an analog supply and analog ground (pin 16) should be treated as its return path for decoupling purposes.

4. Obtain straight binary/offset binary output coding by tying $\overline{\text{COMP BIN}}$ (pin 7) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie the $\overline{\text{COMP BIN}}$ pin to ground. The $\overline{\text{COMP BIN}}$ signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

5. An overflow signal, pin 8, indicates when analog input signals are below or above the desired full-scale range. To overflow pin also has a three-state output and is enabled by pin 10 ($\overline{\text{Enable bits 1-5 \& O.F.}}$).

6. The Sample/$\overline{\text{Hold}}$ control signal, pin 17, goes low following the rising edge of START CONVERT pulse and high 30 nanoseconds minimum before EOC goes low. This indicates that the converter can accept a new analog input.

7. The drive requirements of the ADC-508 may be satisfied with a wide-bandwidth, low output impeance input source. Applications of these converters that require the use of a sample-hold may be satisfied by using DATEL's model SHM-45. Using this device with multiplexers or for test purposes will require an input buffer.

8. Over temperature, input capacitance is 50 pF maximum and input impdeance is 1.75K minimum (2.5K typical) for unipolar and 3.75K minimum (5K typical) for bipolar. These values are guaranteed by design.

9. Requirements for ±2.5V inputs can be satisfied using DATEL's AM-1435 amplifier in front of the SHM-45/ADC-508 configuration, shown in Figure 3, at the appropriate gain. The SHM-45's gain of 2 mode allows 0 to +5V or ±5V input ranges.

TIMING

Figure 2 shows the relationship between the various input signals. The timing cited applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

TABLE 2. INPUT CONNECTIONS

INPUT VOLTAGE RANGE	INPUT PIN	CONNECT PIN 2 (RANGE) TO PIN:
0 to +10V dc	3	3
0 to +20V dc	3	16
±10V dc	3	1

TABLE 3. ZERO AND GAIN ADJUST

FSR	ZERO ADJUST +1/2 LSB	GAIN ADJUST +FS -1 1/2 LSB
0 to +10V dc	+1.22 mV	+9.9963V dc
0 to +20V dc	+2.44 mV	+19.9927V dc
±10V dc	+2.44 mV	+9.9927V dc

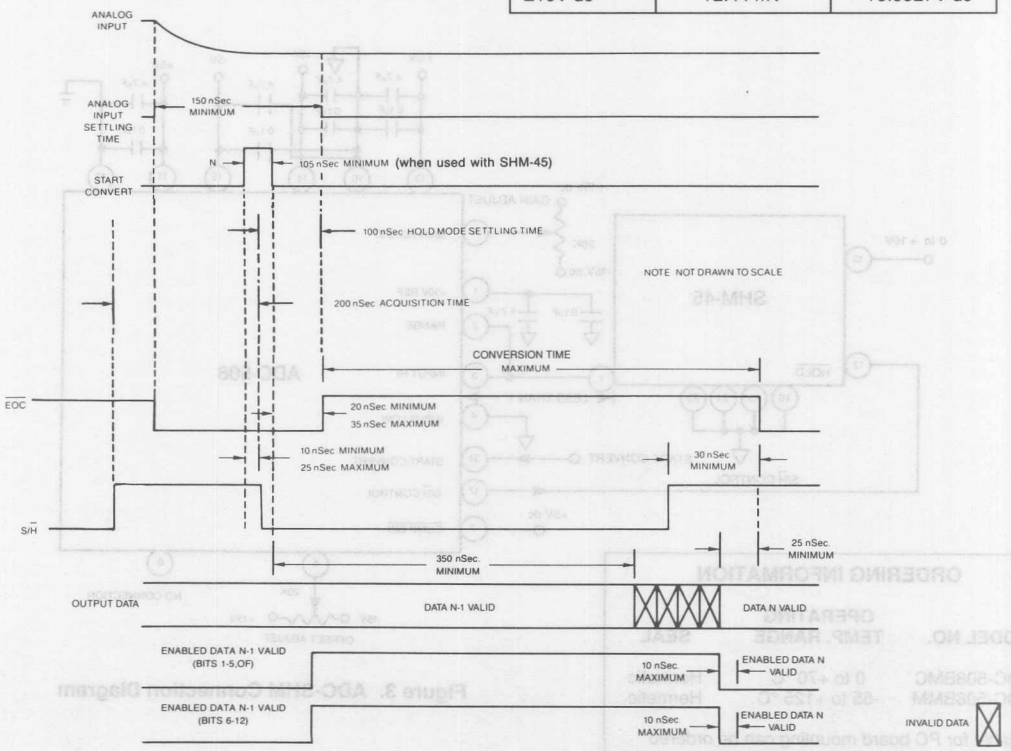


Figure 2. ADC-508 and SHM-45 Timing Diagram

CALIBRATION PROCEDURE

Removal of system errors or the small initial errors is accomplished as follows:

1. Connect the converter per Figure 3 and Table 2 for the appropriate full-scale range (FSR). Apply a pulse of 50 nanoseconds minimum to the START CONVERT input (pin 31) at a rate of 500 KHz. This rate chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments - Apply a precision voltage reference source between the analog input (pin 3) and ground (pin 16). Adjust the output of the reference source per Table 3. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with the COMP BIN (pin 7) tied high or between 1111 1111 1111 and 1111 1111 1110 with the COMP BIN tied low.

3. Full-Scale Adjustment - Set the output of the voltage reference used in step 2 to the value shown in Table 3. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for COMP BIN (pin 7) tied high or between 0000 0000 0001 and 0000 0000 0000 for COMP BIN tied low.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 4.

TABLE 4. OUTPUT CODING

			STRAIGHT BIN. COMP. BINARY				
UNIPOLAR	INPUT RANGES, V dc		OUTPUT CODING			INPUT RANGE	BIPOLAR
SCALE	0 to +10V	0 to +20V	MSB	LSB	MSB LSB	±10V dc	SCALE
+FS -1 LSB	+9.9976V	+19.9951V	1111 1111	1111	0000 0000 0000	+9.9951V	+FS -1 LSB
7/8 FS	+8.7500V	+17.500V	1110 0000	0000	0001 1111 1111	+7.5000V	+3/4 FS
3/4 FS	+7.5000V	+15.000V	1100 0000	0000	0011 1111 1111	+5.0000V	+1/2 FS
1/2 FS	+5.0000V	+10.000V	1000 0000	0000	0111 1111 1111	0.0000V	0
1/4 FS	2.5000V	+5.0000V	0100 0000	0000	1011 1111 1111	-5.0000V	-1/2 FS
1/8 FS	1.2500V	+2.5000V	0010 0000	0000	1101 1111 1111	-7.5000V	-3/4 FS
1 LSB	0.0024V	+0.0049V	0000 0000	0001	1111 1111 1110	-9.9951V	-FS +1 LSB
0	0.0000V	0.0000V	0000 0000	0000	1111 1111 1111	-10.000V	-FS
			OFF. BINARY		COMP. OFF. BIN.		

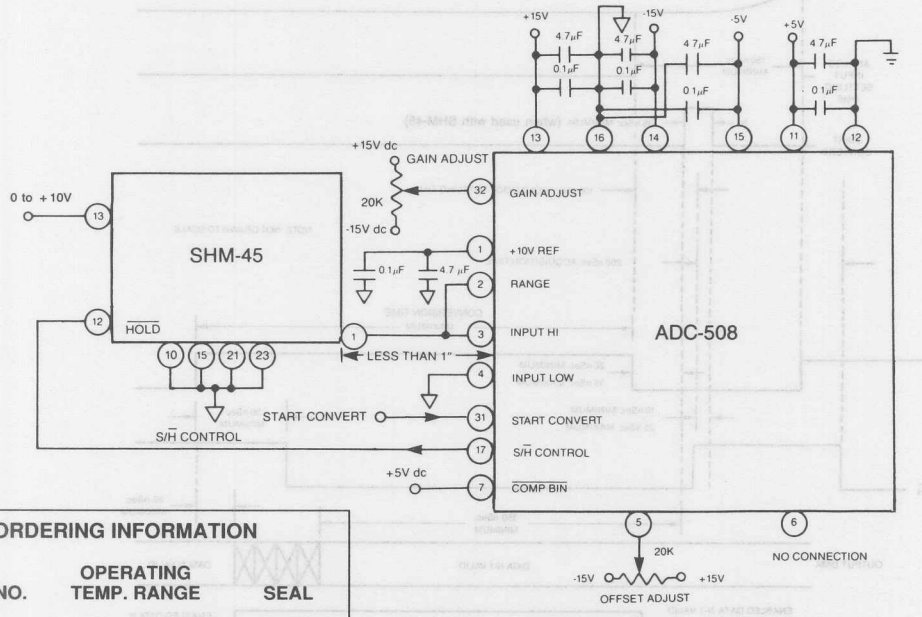


Figure 3. ADC-SHM Connection Diagram

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE	SEAL
ADC-508BMC	0 to +70 °C	Hermetic
ADC-508BMM	-55 to +125 °C	Hermetic

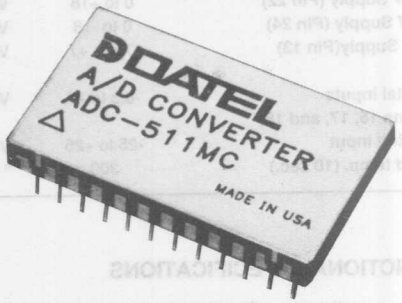
Receptable for PC board mounting can be ordered through AMP Incorporated, #3-331272-8 (Component Lead Socket), 32 required.

ADC-511

12-Bit, High-Speed, Low-Power A/D Converter

FEATURES

- 12-Bit resolution
- 1.0 Microsecond maximum conversion time
- Low-power, 925 milliwatts
- Three-state, output buffers
- Functionally complete
- Small 24-pin DIP
- No missing codes



GENERAL DESCRIPTION

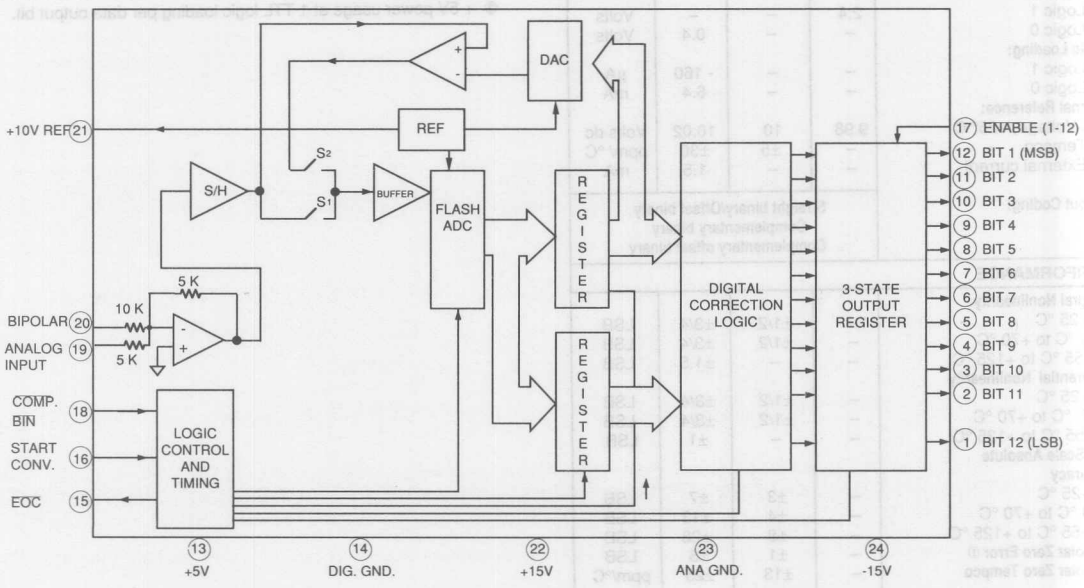
DATEL's ADC-511 uses an advanced design to provide a high-speed, functionally complete 12-bit A/D converter in a small 24-pin DIP. The ADC-511 delivers a conversion speed of 1 microsecond while consuming only 925 milliwatts of power.

Manufactured using thin- and thick-film hybrid technology, the ADC-511's exclusive performance is based upon a digitally-corrected subranging architecture. DATEL further enhances this technology by using a proprietary custom chip and unique laser trimming schemes.

Functionally complete, the ADC-511 contains an internal clock, three-state outputs and an internal reference.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 OUT (LSB)	13	+5V
2	BIT 11 OUT	14	DIGITAL GROUND
3	BIT 10 OUT	15	EOC
4	BIT 9 OUT	16	START CONVERT
5	BIT 8 OUT	17	ENABLE (1 - 12)
6	BIT 7 OUT	18	COMP BIN
7	BIT 6 OUT	19	ANALOG INPUT
8	BIT 5 OUT	20	BIPOLAR
9	BIT 4 OUT	21	+10V REF
10	BIT 3 OUT	22	+15V
11	BIT 2 OUT	23	ANALOG GROUND
12	BIT 1 OUT (MSB)	24	-15V



ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 22)	0 to +18	Volts dc
-15V Supply (Pin 24)	0 to -18	Volts dc
+5V Supply(Pin 13)	-0.5 to +7	Volts dc
Digital inputs (Pins 16, 17, and 18)	-0.3 to +7	Volts dc
Analog input	-25 to +25	Volts dc
Lead temp. (10 sec.)	300	° C max.

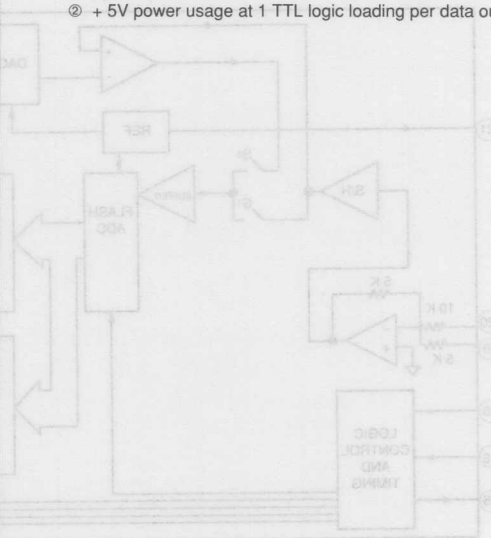
FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and ±5V dc unless otherwise specified.

INPUTS	MIN.	TYP.	MAX.	UNITS
Analog Signal Range	–	0 to +10	–	Volts
(See Table 5 also)	–	±5	–	Volts
Input Impedance				
Resistance	2	2.5	–	K Ohms
Capacitance	–	–	50	pF
Logic Levels:				
Logic 1	2.0	–	–	Volts
Logic 0	–	–	0.8	Volts
Logic Loading:				
Logic 1	–	–	2.5	µA
Logic 0	–	–	-100	µA
OUTPUTS				
Resolution	12	–	–	Bits
Logic Levels:				
Logic 1	2.4	–	–	Volts
Logic 0	–	–	0.4	Volts
Logic Loading:				
Logic 1	–	–	- 160	µA
Logic 0	–	–	6.4	mA
Internal Reference:				
+Voltage, +25° C	9.98	10	10.02	Volts dc
Tempco	–	±5	±30	ppm/ °C
External current	–	–	1.5	mA
Output Coding:	Straight binary/Offset binary Complementary binary Complementary offset binary			
PERFORMANCE				
Integral Nonlinearity				
+25 °C	–	±1/2	±3/4	LSB
0 °C to +70 °C	–	±1/2	±3/4	LSB
-55 °C to +125 °C	–	–	±1.5	LSB
Differential Nonlinearity				
+25 °C	–	±1/2	±3/4	LSB
0 °C to +70 °C	–	±1/2	±3/4	LSB
-55 °C to +125 °C	–	–	±1	LSB
Full-Scale Absolute Accuracy				
+25 °C	–	±3	±7	LSB
0 °C to +70 °C	–	±4	±13	LSB
-55 °C to +125 °C	–	±8	±28	LSB
Unipolar Zero Error ①	–	±1	±3	LSB
Unipolar Zero Tempco	–	±13	±25	ppm/°C

PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Bipolar Zero Error ①	–	±1	±3	LSB
Bipolar Zero Tempco	–	±2	±5	ppm/°C
Bipolar Offset Error ①	–	±2	±4	LSB
Bipolar Offset Tempco	–	±17.5	±35	ppm/°C
Gain Error ①	–	±2	±4	LSB
Gain Error Tempco	–	±17.5	±35	ppm/°C
Conversion Time				
+25 °C	–	–	1.0	µSec.
0 °C to +70 °C	–	–	1.0	µSec.
-55 °C to +125 °C	–	–	1.15	µSec.
No missing codes (For 12 binary bits)	Guaranteed over operating temp. range			
POWER REQUIREMENTS				
Power Supply Range				
+15V dc Supply	+14.25	+15	+15.75	Volts dc
-15V dc Supply	-14.25	-15	-15.75	Volts dc
+5V dc Supply	+4.75	+5	+5.25	Volts dc
Supply Current				
+15V Supply	–	+20	+29	mA
-15V Supply	–	-20	-28	mA
+5V Supply ②	–	+65	+79	mA
Power Dissipation	–	925	1250	mW
Supply Rejection	–	–	±0.01	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temperature Range				
—MC Models	0	–	+70	° C
—MM Models	-55	–	+125	° C
Storage Temperature Range	-65	–	+150	° C
Package Type	24-pin hermetically sealed ceramic DIP			
Weight	0.42(12)oz.(gram)			

① Specifications cited are at +25 °C. See Techical Note 1 for further information.
② + 5V power usage at 1 TTL logic loading per data output bit.



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1. Applications unaffected by endpoint errors or those that remove them through software will use the typical connections shown in Figure 2. The optional external circuitry of Figure 4 removes system errors or helps adjust the small initial errors of the ADC-511 to zero. The external adjustment circuit has no affect on the throughput rate. Table 1 shows how to select the input range.

2. Rated performance requires using good high frequency circuit board layout techniques. The analog and digital grounds are connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter. This prevents contamination of the analog ground by noisy digital ground currents.

3. Bypass the analog and digital supplies and the +10V reference (pin 21) to ground with a 4.7μF, 25V tantalum electrolytic capacitor in parallel with a 0.1 μF ceramic capacitor. Bypass the +10V reference (pin 21) to analog ground (pin 23).

4. Obtain straight binary/offset binary output coding by tying COMP BIN (pin 18) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie pin 18 to ground. The complementary signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

5. To obtain Three-State outputs, connect $\overline{\text{ENABLE}}$ (pin 17) to a logic "0" (low). Otherwise, connect pin 17 to a logic "1" (high).

TIMING

Figure 3 shows the relationship between the various input signals. The timing shown applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

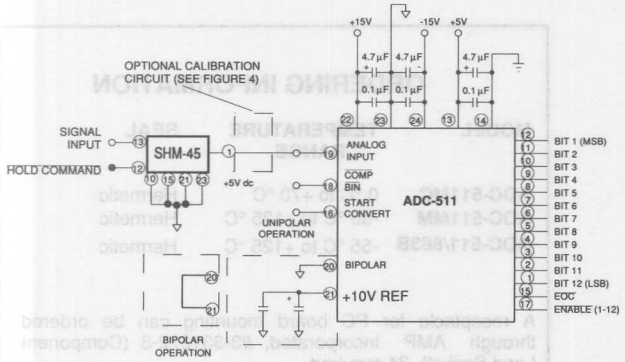


Figure 2. Typical Input Connections for the ADC-511

1. The data outputs should be connected to LED's to observe the resulting data values. Connect the converter per Figure 2, Figure 4, and Table 1 for the appropriate Full Scale Range (FSR). Apply a pulse of 200 nanoseconds minimum to the START CONVERT input (pin 16) at a rate of 250 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments
   Apply a precision voltage reference source between the amplifier's signal input and analog ground. Use a very low-noise signal source for accurate calibration.

   Adjust the output of the reference source per Table 4. For unipolar operation, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with the $\overline{\text{COMP BIN}}$ (pin 18) tied high or between 1111 1111 1111 and 1111 1111 1110 with pin 18 tied low.

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with pin 18 tied high or between 0111 1111 1111 and 0111 1111 1110 with pin 18 tied low.

3. Full-Scale Adjustment
   Set the output of the voltage reference used in step 2 to the value shown in Table 4. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for pin 18 tied high or between 0000 0000 0001 and 0000 0000 0000 for pin 18 tied low.

   To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 6.

Table 1. Input Connections

INPUT RANGE	INPUT PIN	JUMPER THESE PINS:
0 to -10V dc	Pin 19	Pin 20 to GROUND
±5V dc	Pin 19	Pin 20 to Pin 21

Table 4. Zero and Gain Adjust

FSR	ZERO ADJUST +1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to +10V dc	+1.22mV dc	+9.9963V dc
±5V dc	+1.22mV dc	+4.9963V dc

Table 5. Input Ranges (using external calibration)

INPUT RANGE	R1	R2	UNIT
0 to +10V, +5V	2	2	K Ohms
0 to +5V, ±2.5V	2	6	K Ohms
0 to +2.5V, +1.25V	2	14	K Ohms

Table 6. Output Coding

		STRAIGHT BIN.. COMP. BINARY			
UNIPOLAR	INPUT RANGES, V dc	OUTPUT CODING		INPUT RANGE	BIPOLAR
SCALE	0 to +10V	MSB LSB	MSB LSB	±10V dc	SCALE
+FS -1 LSB	+9.9976V	1111 1111 1111	0000 0000 0000	+4.9976V	+FS -1 LSB
7/8 FS	+8.7500V	1110 0000 0000	0001 1111 1111	+3.7500V	+3/4 FS
3/4 FS	+7.5000V	1100 0000 0000	0011 1111 1111	+2.5000V	+1/2 FS
1/2 FS	+5.0000V	1000 0000 0000	0111 1111 1111	0.0000V	0
1/4 FS	+2.5000V	0100 0000 0000	1011 1111 1111	-2.5000V	-1/2 FS
1/8 FS	+1.2500V	0010 0000 0000	1101 1111 1111	-3.7500V	-3/4 FS
1 LSB	+0.0024V	0000 0000 0001	1111 1111 1110	-4.9976V	-FS +1 LSB
0	0.0000V	0000 0000 0000	1111 1111 1111	-5.0000V	-FS
		OFF. BINARY	COMP. OFF. BIN.		

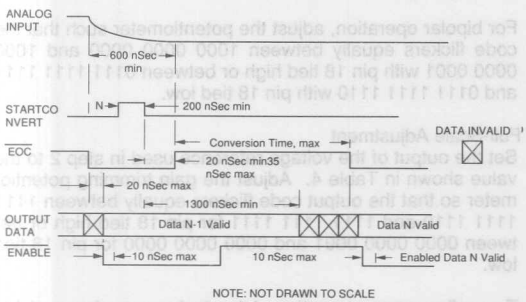
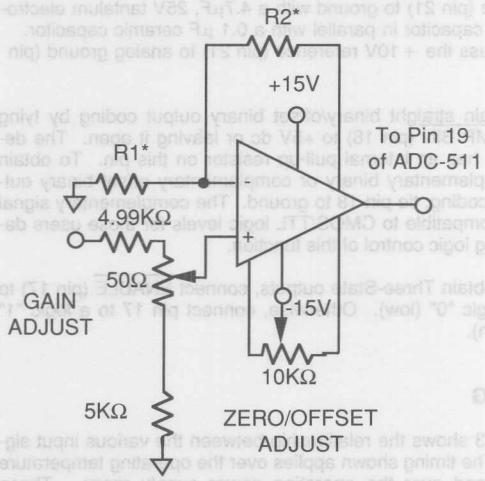


Figure 3. ADC-511 Timing Diagram

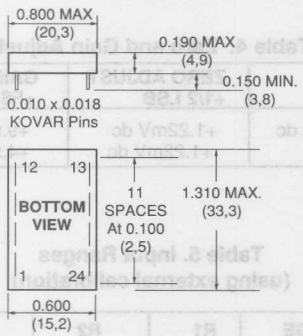
Optional Calibration Circuit



* See Table 5 for R1 and R2 values.

Figure 4. Optional Calibration Circuit

MECHANICAL DIMENSIONS INCHES (MM)



NOTE: Pins have 0.025 Inch ±0.01 standoff from case.

NOTE: Pins have a 0.025 Inch, ±0.01 standoff from case.

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	SEAL
ADC-511MC	0 °C to +70 °C	Hermetic
ADC-511MM	-55 °C to +125 °C	Hermetic
ADC-511/883B	-55 °C to +125 °C	Hermetic

A receptacle for PC board mounting can be ordered through AMP Incorporated, #3-331272-8 (Component Lead Socket), 24 required.

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ADC-520, ADC-521

12-Bit, Ultra-Fast, Low-Power A/D Converters

FEATURES

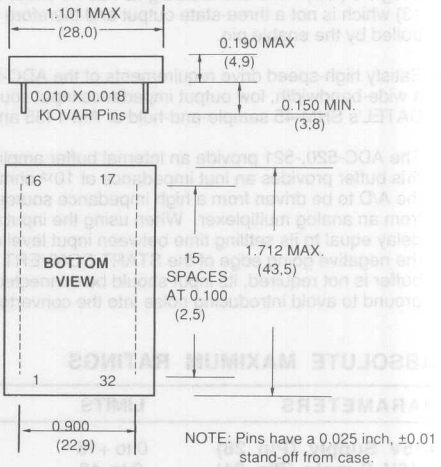
- **12-Bit resolution**
- **800 Nanosecond maximum conversion time**
- **Pin-programmable input ranges**
- **Internal high impedance buffer**
- **Low 1.6 watts power consumption**
- **Three-state output buffers**
- **Small 32-pin DIP**
- **No missing codes**

GENERAL DESCRIPTION

DATEL's ADC-520 and ADC-521 are 12-bit analog-to-digital converters with conversion speeds of up to 800 nanoseconds. Both models are identical except for the analog input voltage ranges.

The performance of these converters is based upon a digitally-correcting subranging architecture. DATEL further enhances this technology by using unique laser trimming schemes. The ADC-520 and ADC-521 are packaged in a 32-pin ceramic DIP and consume 1.6 watts.

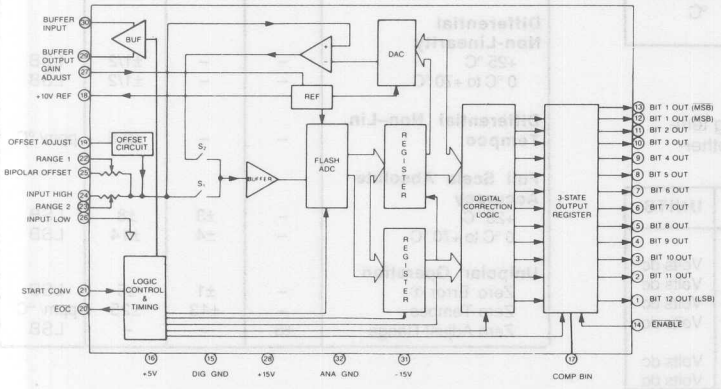
MECHANICAL DIMENSIONS INCHES (mm)



NOTE: Pins have a 0.025 inch, ±0.01 stand-off from case.

TECHNICAL NOTES

1. Use external potentiometers to remove system errors or the small initial errors to zero. Use a 20K ohm trimming potentiometer for gain adjjustment with the wirper tied to pin 27 (ground pin 27 for operation without adjustments). Use a 20K ohm trimming potentiometer with the wiper tied to pin 19 for zero/offset adjustment (leave pin 19 open for operation without adjustment).



I/O CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 OUT (LSB)	17	COMP BIN
2	BIT 11 OUT	18	REF. OUT (+10V dc)
3	BIT 10 OUT	19	OFFSET ADJUST
4	BIT 9 OUT	20	EOC
5	BIT 8 OUT	21	START CONVERT
6	BIT 7 OUT	22	RANGE 1
7	BIT 6 OUT	23	RANGE 2
8	BIT 5 OUT	24	INPUT HIGH
9	BIT 4 OUT	25	BIPOLAR OFFSET
10	BIT 3 OUT	26	INPUT LOW
11	BIT 2 OUT	27	GAIN ADJUST
12	BIT 1 OUT (MSB)	28	+15V
13	BIT 1 OUT (MSB)	29	BUFFER OUTPUT
14	ENABLE	30	BUFFER INPUT
15	DIGITAL GROUND	31	-15V
16	+5V	32	ANALOG GROUND

2. Rated performance requires using good high frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

3. Bypass all the analog and digital supplies and the +10V reference (pin 18) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 18) to analog ground (pin 32) the same way.

4. Obtain straight binary/offset binary output coding by tying $\overline{\text{COMP BIN}}$ (pin 7) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie the COMP BIN pin to ground. In the bipolar mode, two's complement output coding is available by using the MSB output (pin 13). The COMP BIN signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

5. Enable the three-state outputs by connecting $\overline{\text{ENABLE}}$ (pin 14) to a logic 0 (low). The ENABLE signal has no effect on MSB (pin 13) which is not a three-state output and therefore is not controlled by the enable pin.

6. Satisfy high-speed drive requirements of the ADC-520, -521 with a wide-bandwidth, low output impedance input source such as DATEL's SHM-45 sample-and-hold or AM-1435 amplifier.

7. The ADC-520,-521 provide an internal buffer amplifier. Using this buffer provides an inut impedance of 10^{12} ohms, allowing the A/D to be driven from a high impedance source or directly from an analog multiplexer. When using the input buffer, allow a delay equal to its settling time between input level change and the negative going edge of the START CONVERT pulse. If the buffer is not required, its input should be connected to analog ground to avoid introducing noise into the converter.

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 28)	0 to +18	Volts dc
-15V Supply (Pin 31)	0 to -18	Volts dc
+5V Supply (Pin 16)	-0.5 to +7.0	Volts dc
Digital Inputs (Pins 14, 17, 21)	-0.3 to +6.0	Volts dc
Analog Input (Pin 24)	-15 to +15	Volts dc
Lead Temp.(10 Sec.)	300	°C

FUNCTIONAL SPECIFICATIONS

The following specifications apply over the operating temperature range and at ±15V dc and +5V dc unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Range				
(ADC–520)	–	±10	–	Volts dc
	–	0 to +10	–	Volts dc
	–	0 to +20	–	Volts dc
	–	0 to -20	–	Volts dc
(ADC–521)	–	±2.5	–	Volts dc
	–	0 to +5	–	Volts dc
Input Impedance				
(ADC–520)				
Unipolar:	1.75	2.5	–	K Ohms
Bipolar:	3.75	5.0	–	K Ohms
(ADC–521)				
Unipolar:	2.0	2.5	–	K Ohms
Bipolar:	1.6	2.0	–	K Ohms
Input Capacitance	–	–	50	pf
Buffer Amplifier				
Input Voltage	+10	–	–	Volts dc
Input Impedance	–	10^{12}	–	Ohms
Settling Time	–	700	1000	nSec.
DIGITAL INPUTS				
Logic "1"	2.0	–	–	Volts dc
Logic "0"	–	–	0.8	Volts dc
Logic Loading "1"	–	–	5	µA
Logic Loading "0"	–	–	-200	µA
OUTPUTS				
Resolution	12	–	–	Bits
Logic "1"	2.4	–	–	Volts dc
Logic "0"	–	–	0.4	Volts dc
Logic Loading "1"	–	–	-160	µA
Logic Loading "0"	–	–	6.4	mA
Internal Reference Voltage, +25 °C	9.98	10.0	10.02	Volts dc
Drift	–	±5	±30	ppm/ °C
External Current	–	–	1.5	mA
Output Coding				
(Pin 17 HI)	Straight binary/offset binary			
(Pin 17 Low)	Complementary binary			
	Complementary offset binary			
(Note 4)	Two's complement			
(Note 4)	Complementary two's complement			
PERFORMANCE				
Integral Non-Linearity				
+25 °C	–	–	±1/2	LSB
0 °C to +70 °C	–	–	±1/2	LSB
Integral Non–Lin. Tempco	–	±3	±8	ppm/ °C
Differential Non-Linearity				
+25 °C	–	–	±1/2	LSB
0 °C to +70 °C	–	–	±1/2	LSB
Differential Non–Lin. Tempco	–	–	±2.5	ppm/ °C
Full Scale Absolute Accuracy				
+25 °C	–	±3	±8	LSB
0 °C to +70 °C	–	±4	±14	LSB
Unipolar Operation				
Zero Error ①	–	±1	±5	LSB
Zero Tempco	–	±13	±25	ppm/ °C
Zero Adjust Range	±5	–	–	LSB

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Bipolar Operation	MIN.	TYP.	MAX.	UNITS
Zero Error ①	–	±1	±5	LSB
Zero Tempco	–	±2	±5	ppm/ °C
Zero Adjust Range	±5	–	–	LSB
Offset Error ①	–	±2	±5	LSB
Offset Tempco	–	±17.5	±35	ppm/ °C
Offset Adjust Range	±5	–	–	LSB
Gain Error ①	–	±2	±5	LSB
Gain Tempco	–	±17.5	±35	ppm/ °C
Gain Error Adjust Range	±5	–	–	LSB
Conversion Times				
+25 °C	–	–	800	nSec.
0 °C to +70 °C	–	–	850	nSec.
Harm. Distort. (-FS) ②				
+25 °C		-72 dB min.		
0 to +70 °C		-72 dB min.		
-55 to +125 °C		-65 dB min.		
No Missing Codes (12 Bits)		Over the Operating Temperature Range		
POWER REQUIREMENTS				
Power Supply Range				
+15V dc Supply	+14.25	+15.0	+15.75	Volts dc
-15V dc Supply	-14.25	-15.0	-15.75	Volts dc
+5V dc Supply	+4.75	+5.0	+5.25	Volts dc
Power Supply Current				
+15V dc Supply	–	+52	+65	mA
-15V dc Supply	–	-36	-45	mA
+5V dc Supply*	–	+66	+70	mA
Power Dissipation	–	1.6	1.9	Watts
Power Supply Rejection	–	–	0.01	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range	0	–	+70	°C
Storage Temperature Range	-65	–	+150	°C
Package Type	32-Pin hermetic sealed, ceramic DIP			
Pins	0.010 x 0.018 inch Kovar			
Weight	0.42 ounces (12 grams)			

* +5V power usage at 1 TTL logic loading per data output bit.

① Specifications cited are at +25 °C. See Technical Note 1 for further information.

② With DATEL SHM-45, see Figure 3.

INPUT CONNECTIONS

Table 2a. ADC-520 Input Connections

INPUT RANGE	INPUT PIN W/O BUFFER	INPUT PIN WITH BUFFER	CONNECT
±10V dc	Pin 24	Pin 30, tie 29 to 24	Pin 18 to 25
0 to +10V dc	Pin 24	Pin 30, tie 29 to 24	Pin 24 to 25
0 to +20V dc	Pin 24	DO NOT USE	Pin 26 to 25
0 to -20V dc	Pin 25	DO NOT USE	Pin 18 to 24, 22 to 23 to 24

Table 2b. ADC-521 Input Connections

INPUT RANGE	INPUT PIN W/O BUFFER	INPUT PIN WITH BUFFER	CONNECT
±2.5V dc	Pin 24,22,23	Pin 30, tie 29 to 24	Pin 25 to 18
0 to +5V dc	Pin 24,22,23	Pin 30, tie 29 to 24	Pin 25 to 26

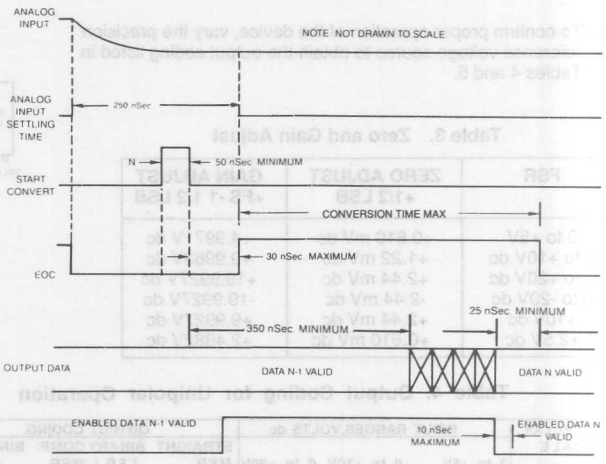

Figure 2. ADC-520, ADC-521 Timing Diagram

TIMING

Figure 2 shows the relationship between the various input signals. The timing cited applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3 and Tables 2a and 2b for the appropriate full-scale range (FSR). Apply a pulse of 50 nanoseconds minimum to the START CONVERT input (pin 21) at a rate of 500 KHz. This rate reduces flicker if LED's are used on the outputs for calibration purposes.
2. Zero Adjustments - Apply a precision voltage reference source between the analog input and ground. Refer to Tables 2a and 2b for the correct input pin. Adjust the output of the reference source per Table 3. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with the COMP BIN (pin 17) tied high (straight binary) or between 1111 1111 1111 and 1111 1111 1110 with the COMP BIN tied low (complementary binary).

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with COMP BIN (pin 17) tied high (offset binary) or between 0111 1111 1111 and 0111 1111 1110 with COMP BIN (pin 17) tied low (complementary offset binary).

Two's complement and complementary two's complement requires the use of MSB (pin 13) versus MSB (pin 12) as given for offset binary or complementary offset binary respectively.

3. Full-Scale Adjustment - Set the output of the voltage reference used in step 2 to the value shown in Table 3. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for COMP BIN (pin 17) tied high or between 0000 0000 0001 and 0000 0000 0000 for COMP BIN tied low. Two's complement and complementary two's complement respectively requires using MSB, pin 13.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Tables 4 and 5.

Table 3. Zero and Gain Adjust

FSR	ZERO ADJUST +1/2 LSB	GAIN ADJUST +FS -1 1/2 LSB
0 to +5V	+0.610 mV dc	+4.9971V dc
0 to +10V dc	+1.22 mV dc	+9.9963V dc
0 to +20V dc	+2.44 mV dc	+19.9927V dc
0 to -20V dc	-2.44 mV dc	-19.9927V dc
+10V dc	+2.44 mV dc	+9.9927V dc
+2.5V dc	+0.610 mV dc	+2.4982V dc

Table 4. Output Coding for Unipolar Operation

UNIPOLAR SCALE	INPUT RANGES,VOLTS dc			OUTPUT CODING	
				STRAIGHT BINARY	COMP. BINARY
	0 to +5V	0 to +10V	0 to +20V	MSB LSB	MSB LSB
+FS-1LSB	+4.9988V	+9.9976V	+19.9951V	1111 1111 1111	0000 0000 0000
7/8 FS	+4.3750V	+8.7500V	+17.500V	1110 0000 0000	0001 1111 1111
3/4 FS	+3.7500V	+7.5000V	+15.000V	1100 0000 0000	0011 1111 1111
1/2 FS	+2.5000V	+5.0000V	+10.000V	1000 0000 0000	0111 1111 1111
1/4 FS	+1.2500V	+2.5000V	+5.0000V	0100 0000 0000	1011 1111 1111
1/8 FS	+0.0024V	+1.2500V	+2.5000V	0010 0000 0000	1101 1111 1111
1 LSB	+0.0012V	+0.0024V	+0.0048V	0000 0000 0001	1111 1111 1110
0	0.0000V	0.0000V	0.0000V	0000 0000 0000	1111 1111 1111

Table 5. Output Coding for Bipolar Operation

BIPOLAR SCALE	INPUT RANGES,VOLTS dc		OUTPUT CODING		
			OFFSET BINARY	COMP TWO'S COMP	TWO'S COMP.
	±2.5V	±10V	MSB LSB	MSB LSB	MSB LSB
+FS -1 LSB	+2.4988V	+9.9951V	1111 1111 1111	1000 0000 0000	0111 1111 1111
+3/4 FS	+1.8750V	+7.5000V	1110 0000 0000	1001 1111 1111	0110 0000 0000
+1/2 FS	+1.2500V	+5.0000V	1100 0000 0000	1011 1111 1111	0100 0000 0000
0	0.0000V	0.0000V	1000 0000 0000	1111 1111 1111	0000 0000 0000
-1/2 FS	-1.2500V	-5.0000V	0100 0000 0000	0011 1111 1111	1100 0000 0000
-3/4 FS	-1.8750V	-7.5000V	0010 0000 0000	0101 1111 1111	1010 0000 0000
-FS +1 LSB	-2.4988V	-9.9951V	0000 0000 0001	0111 1111 1110	1000 0000 0001
-FS	-2.5000V	-10.000V	0000 0000 0000	0111 1111 1111	1000 0000 0000

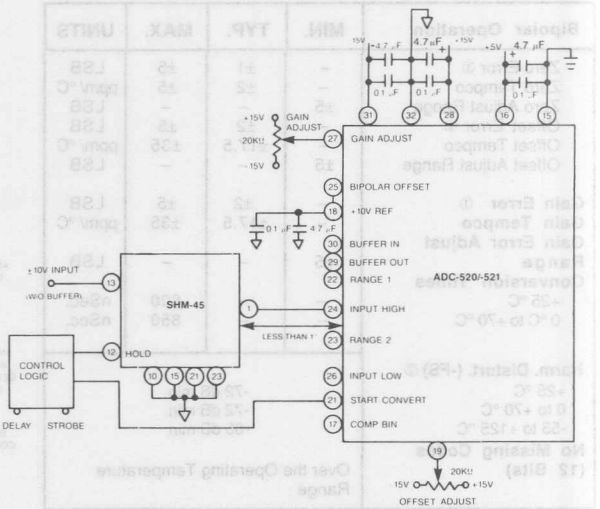

Figure 3. ADC/SHM Connection Diagram

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
ADC-520MC	0 to +70 °C
ADC-521MC	0 to +70 °C

Order PC board mounting receptacle through AMP Inc. part #3-331272-8 (Component Lead Socket), 32 required.

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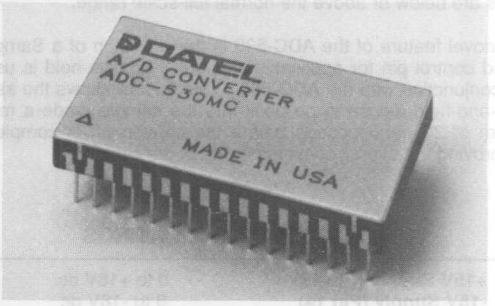
ADC-530

12-Bit, Ultra-fast, Low-Power A/D Converter

FEATURES

- 12-Bit resolution
- 350 Nanoseconds maximum conversion time
- Low-power, 2.1W
- Small initial errors
- Three-state output buffers
- -55 to +125 °C operation
- Small 32-pin DIP
- No missing codes



GENERAL DESCRIPTION

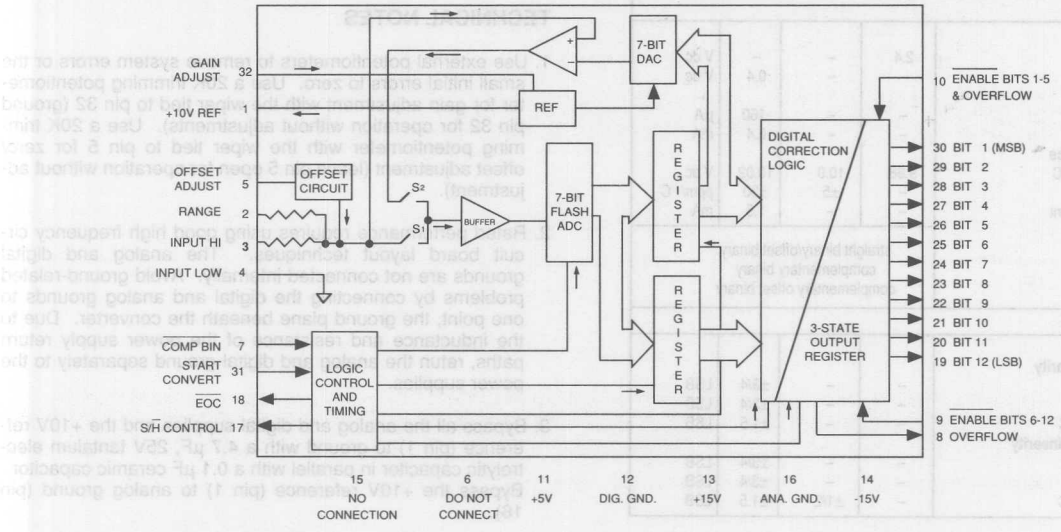
DATEL's ADC-530 reflects the ultimate in state-of-the-art analog signal conversion technology. The ADC-530 boasts a conversion speed of 350 nanoseconds, along with a low-power consumption of 2.1 watts.

DATEL's ADC-530 is a 12-bit analog-to-digital converter which has small initial errors and can also provide adjustment capability for system errors. The ADC-530 has a maximum conversion time of 350 nanoseconds.

Manufactured using thick-film and thin-film hybrid technology, this converter's remarkable performance is based upon a digitally-corrected subranging architecture. DATEL further enhances this technology by using a proprietary custom chip and unique laser trimming schemes. The ADC-530 is packaged in a 32-pin ceramic DIP.

INPUT/OUTPUT CONNECTIONS

PIN	SIGNAL NAME	PIN	SIGNA NAME
1	+10V REF. OUT	17	S/H CONTROL
2	RANGE	18	EOC
3	INPUT HIGH	19	BIT 12 OUT (LSB)
4	INPUT LOW	20	BIT 11 OUT
5	OFFSET ADJUST	21	BIT 10 OUT
6	DO NOT CONNECT	22	BIT 9 OUT
7	COMP BIN	23	BIT 8 OUT
8	OVERFLOW	24	BIT 7 OUT
9	ENABLE (BITS 7-12)	25	BIT 6 OUT
10	ENABLE (BITS 1-6) & OVERFLOW	26	BIT 5 OUT
11	+5V	27	BIT 4 OUT
12	DIGITAL GROUND	28	BIT 3 OUT
13	+15V	29	BIT 2 OUT
14	-15V	30	BIT 1 OUT (MSB)
15	NO CONNECTION	31	START CONVERT
16	ANALOG GROUND	32	GAIN ADJUST



All digital inputs and three-state outputs are TTL- and CMOS-compatible. Output coding can be in straight binary/offset binary or complementary binary/complementary offset binary by using the COMP BIN pin. An overflow pin indicates when inputs are below or above the normal full-scale range.

A novel feature of the ADC-530 is the provision of a Sample/Hold control pin for applications where a sample-hold is used in conjunction with the ADC-530. This feature allows the sample-and-hold device to go back into the sample mode a minimum of 30 nanoseconds before the conversion is complete, improving the overall conversion rate of the system.

ABSOLUTE MAXIMUM RATINGS

+15V Supply (Pin 13)	0 to +18V dc
-15V Supply (Pin 14)	0 to -18V dc
+5V Supply (Pin 11)	-0.5 to +7V dc
Digital Inputs (Pins 7, 9, 10, & 31)	-0.3 to +6V dc
Analog Input (Pin 3)	-15 to +15V dc
Lead temperature (10 Sec.)	300 °C max.

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and +5V power supply voltages unless otherwise specified.

INPUTS	MIN.	TYP.	MAX.	UNIT
Input Voltage Range	–	0 to +10	–	V dc
(See Tech Note 9)	–	0 to +20	–	V dc
	–	±10	–	V dc
Logic Levels				
Logic 1	2.0	–	–	V dc
Logic 0	–	–	0.8	V dc
Logic Loading				
Logic 1	–	–	2.5	µA
Logic 0	–	–	-100	µA
OUTPUTS				
Logic Levels				
Logic 1	2.4	–	–	V dc
Logic 0	–	–	0.4	V dc
Logic Loading				
Logic 1	–	–	-160	µA
Logic 0	–	–	6.4	mA
Internal Reference				
Voltage, +25 °C	9.98	10.0	10.02	V dc
Drift	–	±5	±30	ppm/ °C
External Current	–	–	1.5	mA
Output Coding				
(Pin 7 High)	straight binary/offset binary			
(Pin 7 Low)	complementary binary complementary offset binary			
PERFORMANCE				
Integral Nonlinearity				
+25 °C	–	–	±3/4	LSB
0 to +70 °C	–	–	±3/4	LSB
-55 to +125 °C	–	–	±1.5	LSB
Differential Nonlinearity				
+25 °C	–	–	±3/4	LSB
0 to +70 °C	–	–	±3/4	LSB
-55 to +125 °C	–	±1/2	±1.5	LSB

PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Full-Scale Abs. Accuracy				
+25 °C	–	±0.1	±0.25	%FSR
0 to +70 °C	–	±0.13	±0.32	%FSR
-55 to +125 °C	–	±0.2	±0.5	%FSR
Unipolar Zero Error				
+25 °C	–	±0.05	±0.13	%FSR
Unipolar Zero Tempco	–	±13	±25	ppm/ °C
Bipolar Zero Error				
+25 °C	–	±0.05	±0.13	%FSR
Bipolar Zero Tempco	–	±13	±25	ppm/ °C
Bipolar Offset Error				
+25 °C	–	±0.1	±0.2	%FSR
Bipolar Offset Error				
Tempco	–	±17.5	±35	ppm/ °C
Gain Error, +25 °C	–	±0.08	±0.17	%FSR
Gain Tempco	–	±17.5	±35	ppm/ °C
Conversion Times				
+25 °C	–	–	350	nSec.
0 to +70 °C	–	–	400	nSec.
-55 to +125 °C	–	–	400	nSec.
No Missing Codes (12 Bits)	Over the operating temp. range			
POWER SUPPLY REQUIREMENTS				
Power Supply Range				
+15V dc Supply	+14.25	+15	+15.75	V dc
-15V dc Supply	-14.25	-15	-15.75	V dc
+5V dc Supply	+4.75	+5	+5.25	V dc
Power Supply Current				
+15V Supply	–	+60	+70	mA
-15V Supply	–	-30	-40	mA
+5V Supply *	–	+150	+180	mA
Power Dissipation	–	2.1	2.5	Watts
Power Supply Rejection	–	–	0.01	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temperature Range, Case				
-MC	0 to +70 °C			
-MM	-55 to +125 °C			
Storage Temp. Range	-65 to +150 °C			
Package Type	32-pin hermetic, ceramic DIP			
Weight	0.42 ounces (12 grams)			

*+5V power usage at 1 TTL logic loading per data output bit.

TECHNICAL NOTES

1. Use external potentiometers to remove system errors or the small initial errors to zero. Use a 20K trimming potentiometer for gain adjustment with the wiper tied to pin 32 (ground pin 32 for operation without adjustments). Use a 20K trimming potentiometer with the wiper tied to pin 5 for zero/offset adjustment (leave pin 5 open for operation without adjustment).

2. Rated performance requires using good high frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, retun the analog and digital ground separately to the power supplies.

3. Bypass all the analog and digital supplies and the +10V reference (pin 1) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 1) to analog ground (pin 16).

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4. Obtain straight binary/offset binary output coding by tieing COMP BIN (pin 7) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding tie the COMP BIN pin to ground. The COMP BIN signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

5. An overflow signal, pin 8, indicates when analog input signals are below or above the desired full-scale range. The overflow pin also has a three-state output and is enabled by pin 10 (ENABLE bits 1-5 & O.F.).

6. The sample-and-hold (S/H) control signal, pin 17, goes low following the rising edge of a start convert pulse and high 30 nanoseconds minimum before EOC goes low. This indicates that the converter can accept a new analog input.

7. The drive requirements of the ADC-530 may be satisfied with a wide-bandwidth, low output impedance input source. Applications of these converters that require the use of a sample-and-hold may be satisfied by using DATEL's model SHM-45. Using this device with multiplexers or for test purposes will require an input buffer.

8. Over temperature, input capacitance is 50 pF maximum and input impedance is 1.75K minimum (2.5K typical) for 0 to +10V and 3.75K minimum (5K typical) for 0 to +20V, ±10V. These values are guaranteed by design.

9. Requirements for ±2.5V inputs can be satisfied using DATEL's AM-1435 amplifier in front of the SHM-45/ADC-530 configuration, shown in Figure 3, at the appropriate gain. The SHM-45's gain of 2 mode allows 0 to +5V or ±5V input ranges.

TIMING

Figure 2 shows the relationship between the various input signals. The timing cited applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

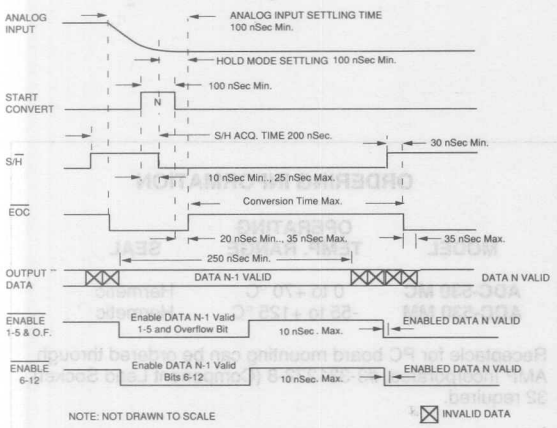


Figure 2. ADC-530 and SHM-45 Timing Diagram

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3 and Table 2 for the appropriate full-scale range (FSR). Apply a pulse of 100 nanoseconds minimum to the START CONVERT input (pin 31) at a rate of 500 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments
   Apply a precision voltage reference source between the analog input (pin 3) and ground (pin 16). Adjust the output of the reference source per Table 3. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with the COMP BIN (pin 7) tied high or between 1111 1111 1111 and 1111 1111 1110 with pin 7 tied low.

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with pin 7 tied high or between 0111 1111 1111 and 0111 1111 1110 with pin 7 tied low.

3. Full-Scale Adjustment
   Set the output of the voltage reference used in step 2 to the value shown in Table 3. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for pin 7 tied high or between 0000 0000 0001 and 0000 0000 0000 for pin 7 tied low.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 4.

Table 2. Input Connections

INPUT VOLTAGE RANGE	INPUT PIN	CONNECT PIN 2 (RANGE) TO PIN:
0 to +10V dc	3	3
0 to +20V dc	3	16
±10V dc	3	1

Table 3. Zero and Gain Adjust

FSR	ZERO ADJUST +1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to +10V dc	+1.22 mV	+909963V dc
0 to +20V dc	+2.44 mV	+19.9927V dc
±10V dc	+2.44 mV	+9.9927V dc

Table 4. Output Coding

			STRAIGHT BIN. COMP. BINARY			
UNIPOLAR	INPUT RANGES, V dc		OUTPUT CODING		INPUT RANGE	BIPOLAR
SCALE	0 to +10V	0 to +20V	MSB LSB	MSB LSB	±10V dc	SCALE
+FS -1 LSB	+9.9976V	+19.9951V	1111 1111 1111	0000 0000 0000	+9.9951V	+FS -1 LSB
7/8 FS	+8.7500V	17.500V	1110 0000 0000	0001 1111 1111	+7.5000V	+3/4 FS
3/4 FS	+7.5000V	15.000V	1100 0000 0000	0011 1111 1111	+5.0000V	+1/2 FS
1/2 FS	+5.0000V	+10.000V	1000 0000 0000	0111 1111 1111	0.0000V	0
1/4 FS	+2.5000V	+5.0000V	0100 0000 0000	1011 1111 1111	-5.0000V	-1/2 FS
1/8 FS	+1.2500V	+2.5000V	0010 0000 0000	1101 1111 1111	-7.5000V	-3/4 FS
1 LSB	+0.0024V	+0.0049V	0000 0000 0001	1111 1111 1110	-9.9951V	-FS +1 LSB
0	0.0000V	0.0000V	0000 0000 0000	1111 1111 1111	-10.000V	-FS
			OFF. BINARY COMP. OFF. BIN.			

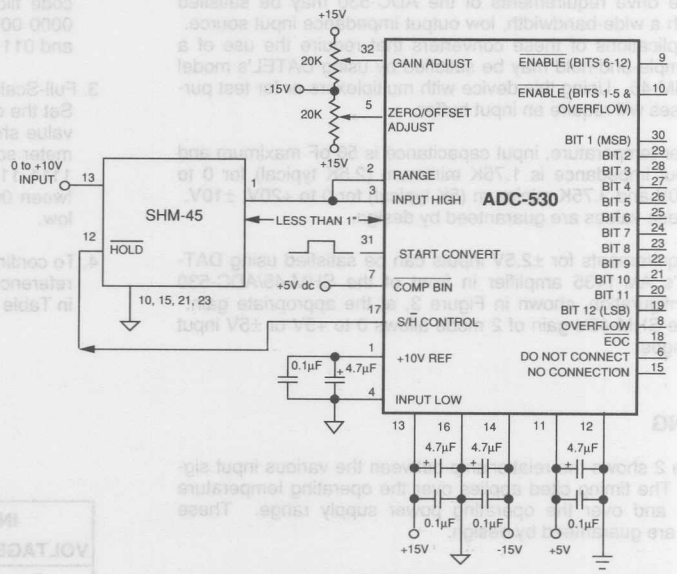
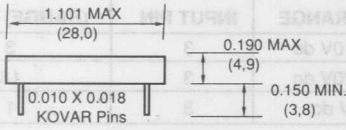
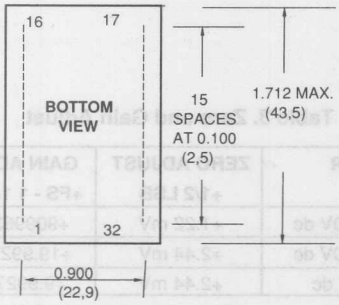


Figure 3. ADC-530 Calibration Setup

MECHANICAL DIMENSIONS INCHES (MM)





NOTE: Pins have a 0.025 inch, ±0.01 stand-off from case.

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	SEAL
ADC-530 MC	0 to +70 °C	Hermetic
ADC-530 MM	-55 to +125 °C	Hermetic

Receptacle for PC board mounting can be ordered through AMP Incorporated, #3-331272-8 (Component Lead Socket), 32 required.

For availability of MIL-STD-883B versions, contact DATEL.

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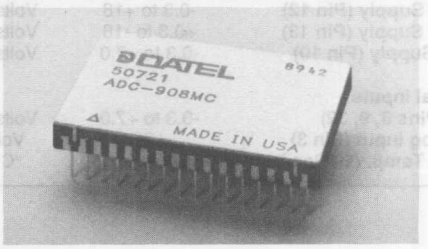
ADC-908
High-Resolution Ultra-Fast A/D Converter

FEATURES

- 14-Bit resolution
- 1.0 μSec. conversion time
- Functionally complete
- Small 32-pin DIP
- Low-power, 2.9 Watts maximum
- Three-state output buffers
- No missing codes



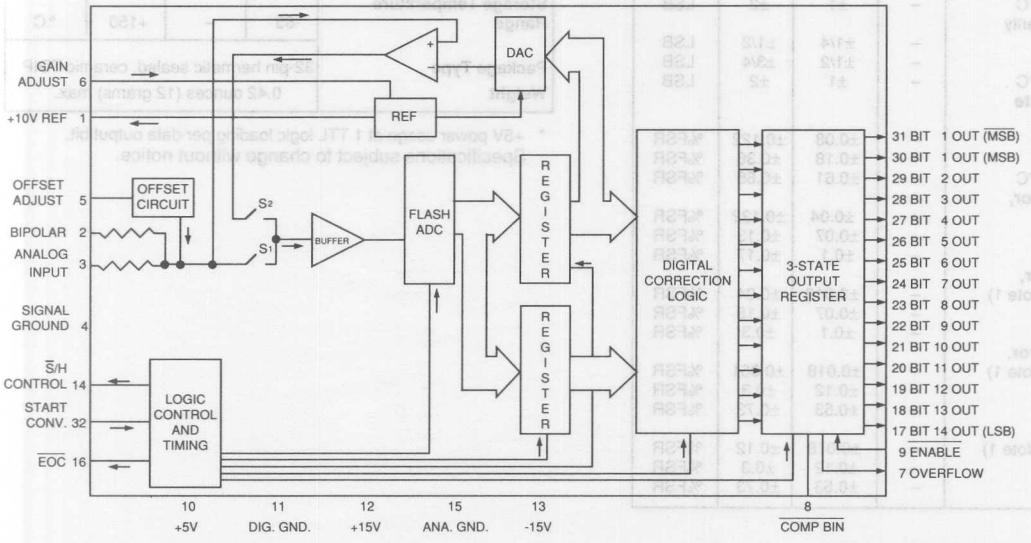
GENERAL DESCRIPTION

DATEL's ADC-908 is a 14-bit, 1.0 microsecond conversion time, functionally complete A/D converter.

Packaged in a small 32-pin DIP, power requirements are ±15 volts and +5 volts with a 2.9 Watts maximum power dissipation.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+10V REF. OUT	17	BIT 14 OUT (LSB)
2	BIPOLAR	18	BIT 13 OUT
3	ANALOG INPUT	19	BIT 12 OUT
4	SIGNAL GROUND	20	BIT 11 OUT
5	OFFSET ADJUST	21	BIT 10 OUT
6	GAIN ADJUST	22	BIT 9 OUT
7	OVERFLOW	23	BIT 8 OUT
8	COMP. BIN	24	BIT 7 OUT
9	ENABLE	25	BIT 6 OUT
10	+5V	26	BIT 5 OUT
11	DIGITAL GROUND	27	BIT 4 OUT
12	+15V	28	BIT 3 OUT
13	-15V	29	BIT 2 OUT
14	S/H CONTROL	30	BIT 1 OUT (MSB)
15	ANALOG GROUND	31	BIT 1 OUT (MSB)
16	EOC	32	START CONVERT



ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 12)	-0.3 to +18	Volts dc
-15V Supply (Pin 13)	+0.3 to -18	Volts dc
+5V Supply (Pin 10)	-0.3 to +7.0	Volts dc
Digital Inputs (Pins 8, 9, 32)	-0.3 to +7.0	Volts dc
Analog Input (Pin 3)	±25	Volts
Lead Temp. (10 Sec.)	300 max.	°C

FUNCTIONAL SPECIFICATIONS

Apply over theoperating temperature range and at ±15V dc and +5V dc power supply voltages unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range				
	–	0 to +10	–	Volts
	–	0 to +20	–	Volts
	–	±5	–	Volts
Input Impedance	1	–	–	K Ohms
Input Capacitance	–	7	15	pf
DIGITAL INPUTS				
Logic Levels				
Logic "1"	2.0	–	–	Volts dc
Logic "0"	–	–	0.8	Volts dc
Logic Loading "1"	–	–	5	µA
Logic Loading "0"	–	–	-200	µA
A/D PERFORMANCE				
Integral Non-Linearity				
+25 °C	–	±1/2	±3/4	LSB
0 °C to +70 °C	–	±3/4	±1	LSB
-55 °C to +125 °C	–	±1	±2	LSB
Differential Non-Linearity				
+25 °C	–	±1/4	±1/2	LSB
0 °C to +70 °C	–	±1/2	±3/4	LSB
-55 °C to +125 °C	–	±1	±2	LSB
Full Scale Absolute Accuracy				
+25 °C.	–	±0.08	±0.122	%FSR
0 °C to +70 °C	–	±0.18	±0.36	%FSR
-55 °C to +125 °C	–	±0.61	±0.85	%FSR
Unipolar Zero Error,				
+25 °C	–	±0.04	±0.122	%FSR
0 to +70 °C	–	±0.07	±0.13	%FSR
-55 to +125 °C	–	±0.1	±0.17	%FSR
Bipolar Zero Error,				
+25 °C (Tech Note 1)	–	±0.012	±0.04	%FSR
0 to +70 °C	–	±0.07	±0.18	%FSR
-55 to +125 °C	–	±0.1	±0.3	%FSR
Bipolar Offset Error,				
+25 °C (Tech Note 1)	–	±0.018	±0.061	%FSR
0 to +70 °C	–	±0.12	±0.3	%FSR
-55 to +125 °C	–	±0.53	±0.73	%FSR
Gain Error,				
+25 °C (Tech Note 1)	–	±0.018	±0.12	%FSR
0 to +70 °C	–	±0.12	±0.3	%FSR
-55 to +125 °C	–	±0.53	±0.73	%FSR

A/D PERFORMANCE	MIN.	TYP.	MAX.	UNITS
A/D Conversion Times				
+25 °C	–	–	1.0	µSec.
0 °C to +70 °C	–	–	1.08	µSec.
-55 °C to +125 °C	–	–	1.15	µSec.
No Missing Codes				
(14 Bits)	0 to +70 °C			
(13 Bits)	-55 to +125 °C			
OUTPUTS				
Resolution	14 Bits			
Output Coding				
(Pin 8 Hi)	Straight binary/offset binary			
(Pin 8 Low)	Complementary binary			
Logic Levels				
Logic "1"	2.4	–	–	Volts dc
Logic "0"	–	–	0.4	Volts dc
Logic Loading "1"	–	–	-160	µA
Logic Loading "0"	–	–	6.4	mA
Internal Reference				
Voltage, +25 °C	+9.98	+10.0	+10.02	Volts dc
Drift	–	±13	±30	ppm/ °C
External Current	–	–	2	mA
POWER REQUIREMENTS				
Power Supply Range				
+15V dc Supply	+14.25	+15.0	+15.75	Volts dc
-15V dc Supply	-14.25	-15.0	-15.75	Volts dc
+5V dc Supply	+4.75	+5.0	+5.25	Volts dc
Power Supply Current				
+15V dc Supply	–	+85	+95	mA
-15V dc Supply	–	-71	-80	mA
+5V dc Supply *	–	+80	+100	mA
Power Dissipation	–	2.7	2.9	Watts
Power Supply Rejection	–	–	0.02	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range				
-MC	0	–	+70	°C
-MM	-55	–	+125	°C
Storage Temperature Range	-65	–	+150	°C
Package Type	32-pin hermetic sealed, ceramic TDIP			
Weight	0.42 ounces (12 grams) max.			

* +5V power usage at 1 TTL logic loading per data output bit.

Specifications subject to change without notice.

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TECHNICAL NOTES

1. Use external potentiometers to remove system errors or the small initial errors to zero. Use a 20K trimming potentiometer for gain adjustment with the wiper tied to pin 6 (ground pin 6 for operation without adjustments). Use a 20K trimming potentiometer with the wiper tied to pin 5 for zero/offset adjustment (ground pin 5 for operation without adjustment).

2. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

3. Bypass the analog and digital supplies and the +10V reference (pin 1) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 1) to analog ground (pin 15).

4. Obtain straight binary/offset binary or 2's complement output coding by tying $\overline{\text{COMP BIN}}$ (pin 8) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary, complementary off set binary, or complementary 2's complement output coding, tie pin 8 to ground. The $\overline{\text{COMP BIN}}$ signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

5. To enable the three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 9) to a logic "0" (low). To disable, connect pin 9 to a logic "1" (high).

6. The $\overline{\text{SAMPLE}}$/HOLD CONTROL, pin 14, is low on power-up. The START CONVERT pulse should be given at a time delay equal to the desired acquisition time minus the 10 nanosecond delay from START CONVERT high to $\overline{\text{S}}$/H CONTROL high. This assures the sample-hold has the minimum required acquisition time for the particular application mode.

   The $\overline{\text{SAMPLE}}$/HOLD CONTROL pin goes high following the rising edge of a START CONVERT pulse and low 30 nanoseconds minimum before $\overline{\text{EOC}}$ goes low. This indicates the converter can accept a new analog input.

7. Retriggering the START CONVERT pulse before $\overline{\text{EOC}}$ goes low will not initiate a new conversion.

Table 1. Input Connections

INPUT RANGE	INPUT PIN	TIE TOGETHER
0 to +10V	Pin 3	Pins 2 and 4
0 to +20	Pin 2	Pins 3 and 4
±5V	Pin 3	Pins 2 and 1

Table 2. Zero and Gain Adjust

FSR	ZERO ADJUST +1/2 LSB	GAIN ADJUST FS - 1/2 LSB
0 to +10V	+305 µV	+9.999085V
0 to +20V	+610 µV	+19.99817V
±5V	+305 µV	+4.999085V

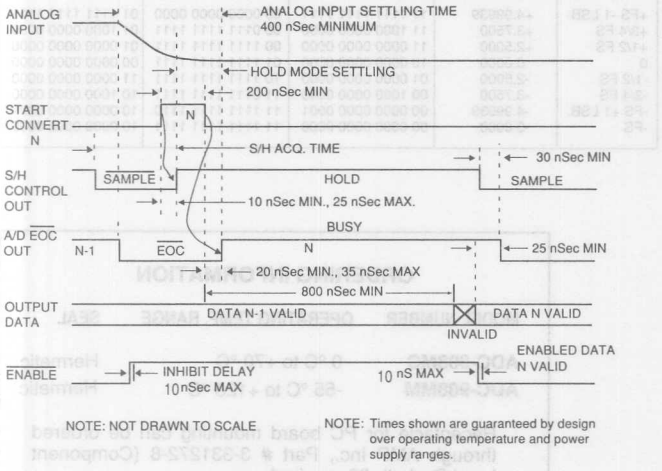


Figure 2. ADC-908 Timing Diagram

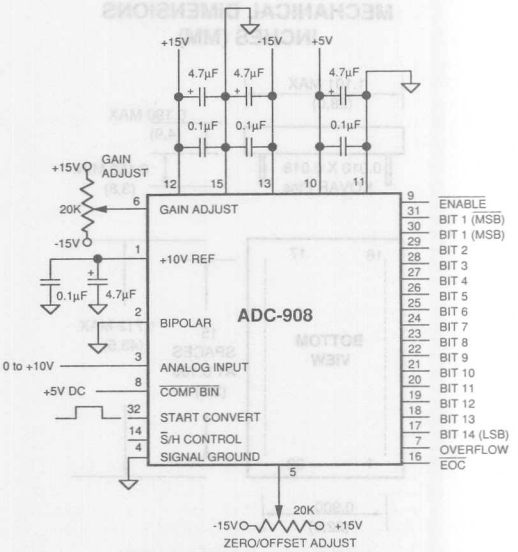


Figure 3. Typical ADC-908 Connection Diagram

CALIBRATION PROCEDURE

1. Connect the converter per Figure 3, and Table 1 for the appropriate full-scale range (FSR). Apply a pulse of 200 nanoseconds minimum to the START CONVERT input (pin 31) at a rate of 250 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments
   Apply a precision voltage reference source between the analog input (pin 3) and ground (pin 4). Adjust the output of the reference source per Table 2.

   For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 00 0000 0000 0000 and 00 0000 0000 0001 with the COMP BIN (pin 8) tied high (straight binary) or between 11 1111 1111 1111 and 11 1111 1111 1110 with pin 8 tied low (complementary binary).

   For bipolar operation, adjust the potentiometer such that the code flickers equally between 10 0000 0000 0000 and 10 0000 0000 0001 with pin 8 tied high (offset binary) or between 01 1111 1111 1111 and 01 1111 1111 1110 with pin 8 tied low (complementary offset binary).

   Two's complement coding requires use of the $\overline{\text{MSB}}$ (pin 31) with pin 8 tied high, adjusting the potentiometer such that the code flickers between 00 0000 0000 0000 and 00 0000 0000 0001.

3. Full-Scale Adjustment
   Set the output of the voltage reference used in step 2 to the value shown in Table 2.

   Adjust the gain trimming potentiometer so that the output code flickers equally between 11 1111 1111 1110 and 11 1111 1111 1111 with pin 8 tied high (straight binary) or between 00 0000 0000 0000 and 00 0000 0000 0001 pin 8 tied low (complementary binary).

   Two's complement coding requires use of the $\overline{\text{MSB}}$ (pin 31) with the pin 8 tied high, adjusting the gain trimming potentiometer so that the output code flickers equally between 01 1111 1111 1110 and 01 1111 1111 1111.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Tables 3 and 4.

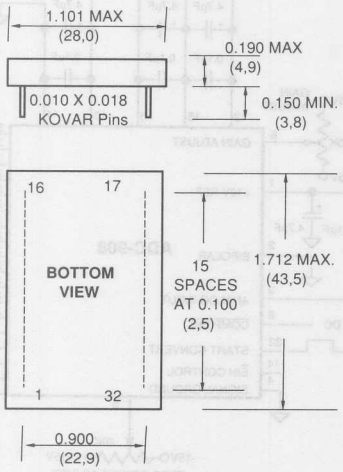
Table 3. Output Coding for Unipolar Operation

UNIPOLAR SCALE	INPUT RANGE (Volts) 0 to +10V	INPUT RANGE (Volts) 0 to +20V	OUTPUT CODING STRAIGHT BIN. MSB LSB	OUTPUT CODING COMP. BINARY MSB LSB
+FS-1LSB	+9.99939	+19.99878	11 1111 1111 1111	00 0000 0000 0000
7/8 FS	+8.7500	+17.500	11 1000 0000 0000	00 0111 1111 1111
3/4 FS	+7.5000	+15.00	11 0000 0000 0000	00 1111 1111 1111
1/2 FS	+5.0000	+10.00	10 0000 0000 0000	01 1111 1111 1111
1/4 FS	+2.5000	+5.000	01 0000 0000 0000	10 1111 1111 1111
1/8 FS	+1.2500	+2.500	00 1000 0000 0000	11 0111 1111 1111
1 LSB	+0.00061	+0.00122	00 0000 0000 0001	11 1111 1111 1110
0	0.0000	0.000	00 0000 0000 0000	11 1111 1111 1111

Table 4. Output Coding for Bipolar Operation

BIPOLAR SCALE	INPUT RANGE (Volts) ±5V	OUTPUT CODING OFFSET BIN. MSB LSB	OUTPUT CODING COMP OFF. BIN. MSB LSB	OUTPUT CODING TWO'S COMP. MSB LSB
+FS -1 LSB	+4.99939	11 1111 1111 1111	00 0000 0000 0000	01 1111 1111 1111
+3/4 FS	+3.7500	11 1000 0000 0000	00 0111 1111 1111	01 1000 0000 0000
+1/2 FS	+2.5000	11 0000 0000 0000	00 1111 1111 1111	01 0000 0000 0000
0	0.0000	10 0000 0000 0000	01 1111 1111 1111	00 0000 0000 0000
-1/2 FS	-2.5000	01 0000 0000 0000	10 1111 1111 1111	11 0000 0000 0000
-3/4 FS	-3.7500	00 1000 0000 0000	11 0111 1111 1111	10 1000 0000 0000
-FS +1 LSB	-4.99939	00 0000 0000 0001	11 1111 1111 1110	10 0000 0000 0001
-FS	-5.0000	00 0000 0000 0000	11 1111 1111 1111	10 0000 0000 0000

MECHANICAL DIMENSIONS INCHES (MM)



NOTE: Pins have a 0.025 inch, ±0.01 stand-off from case.

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	SEAL
ADC-908MC	0 °C to +70 °C	Hermetic
ADC-908MM	-55 °C to +125 °C	Hermetic

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 32 required.

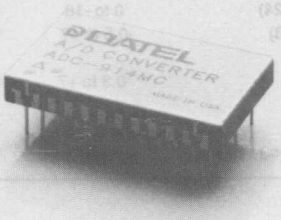
For availability of MIL-STD-883 versions, contact DATEL.

ADC-914
14-Bit, High-Speed, Low-Power A/D Converter

PRODUCT DATA

FEATURES

- **14-Bit resolution**
- **2.4 Microsecond maximum conversion time**
- **Low-power, 925 milliwatts**
- **Three-state output buffers**
- **Functionally complete**
- **Small 24-pin DIP**



GENERAL DESCRIPTION

DATEL's ADC-914 uses an advanced design to provide a high-speed, functionally complete 14-bit A/D converter in a small 24-pin DIP. The ADC-914 delivers a conversion speed of 2.4 microsecond while consuming only 925 milliwatts of power.

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 14 OUT (LSB)	13	+5V
2	BIT 13 OUT	14	$\overline{\text{ENABLE}}$
3	BIT 12 OUT	15	$\overline{\text{EOC}}$
4	BIT 11 OUT	16	START CONVERT
5	BIT 10 OUT	17	BIT 2 OUT
6	BIT 9 OUT	18	BIT 1 (MSB)
7	BIT 8 OUT	19	ANALOG INPUT
8	BIT 7 OUT	20	BIPOLAR
9	BIT 6 OUT	21	+10V REF
10	BIT 5 OUT	22	+15V
11	BIT 4 OUT	23	GROUND
12	BIT 3 OUT (MSB)	24	-15V

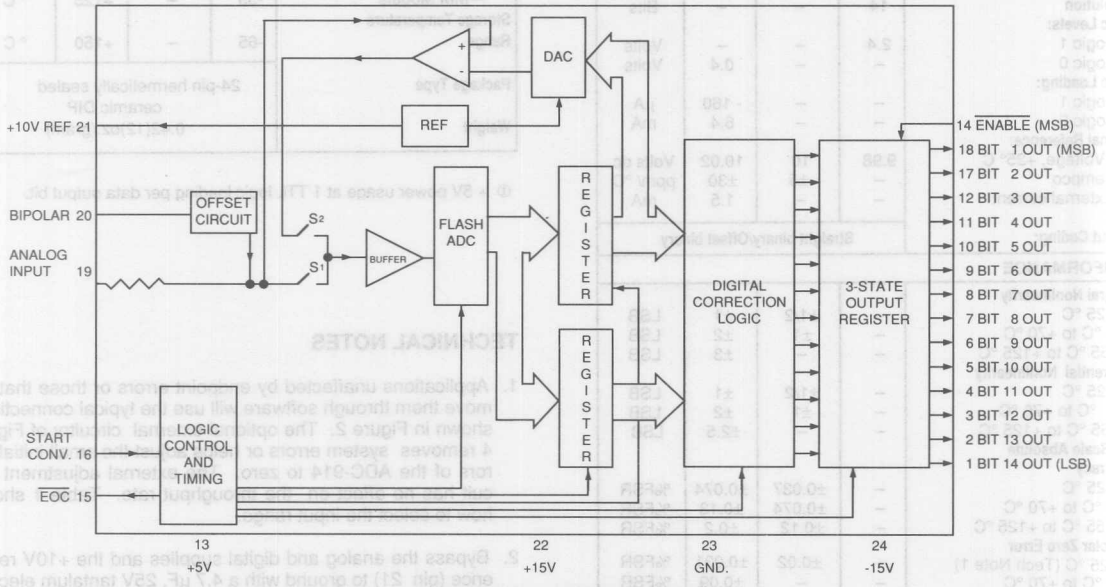


Figure 1. ADC-914 Simplified Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (Pin 22)	0 to +18	Volts dc
-15V Supply (Pin 24)	0 to -18	Volts dc
+5V Supply(Pin 13)	-0.5 to +7	Volts dc
Digital inputs (Pins 14 and 16)	-0.3 to +7	Volts dc
Analog input	-25 to +25	Volts dc
Lead temp. (10 sec.)	300	° C max.

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and +5V dc unless otherwise specified.

INPUTS	MIN.	TYP.	MAX.	UNITS
Analog Signal Range	–	0 to +10	–	Volts
(See Table 5 also)	–	±5	–	Volts
Input Impedance				
Resistance	2	2.5	–	K Ohms
Capacitance	–	–	50	pF
Logic Levels:				
Logic 1	2.0	–	–	Volts
Logic 0	–	–	0.8	Volts
Logic Loading:				
Logic 1	–	–	2.5	µA
Logic 0	–	–	-100	µA
OUTPUTS				
Resolution	14	–	–	Bits
Logic Levels:				
Logic 1	2.4	–	–	Volts
Logic 0	–	–	0.4	Volts
Logic Loading:				
Logic 1	–	–	- 160	µA
Logic 0	–	–	6.4	mA
Internal Reference:				
+Voltage, +25° C	9.98	10	10.02	Volts dc
Tempco	–	±5	±30	ppm/ °C
External current	–	–	1.5	mA
Output Coding:	Straight binary/Offset binary			
PERFORMANCE				
Integral Nonlinearity				
+25 °C	–	±1/2	±1	LSB
0 °C to +70 °C	–	±1	±2	LSB
-55 °C to +125 °C	–	–	±3	LSB
Differential Nonlinearity				
+25 °C	–	±1/2	±1	LSB
0 °C to +70 °C	–	±1	±2	LSB
-55 °C to +125 °C	–	–	±2.5	LSB
Full-Scale Absolute Accuracy				
+25 °C	–	±0.037	±0.074	%FSR
0 °C to +70 °C	–	±0.074	±0.13	%FSR
-55 °C to +125 °C	–	±0.12	±0.2	%FSR
Unipolar Zero Error				
+25 °C (Tech Note 1)	–	±0.02	±0.031	%FSR
0 °C to +70 °C	–	–	±0.09	%FSR
-55 °C to +125 °C	–	–	±0.12	%FSR

PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Bipolar Zero Error				
+25 °C (Tech Note 1)	–	±0.02	±0.031	%FSR
0 °C to +70 °C	–	–	±0.09	%FSR
-55 °C to +125 °C	–	–	±0.12	%FSR
Bipolar Offset Error				
+25 °C (Tech Note 1)	–	±0.02	±0.061	%FSR
0 °C to +70 °C	–	–	±0.12	%FSR
-55 °C to +125 °C	–	–	±0.15	%FSR
Gain Error				
+25 °C (See Tech Note 1)	–	±0.02	±0.061	%FSR
0 °C to +70 °C	–	–	±0.12	%FSR
-55 °C to +125 °C	–	–	±0.15	%FSR
Conversion Time				
+25 °C	–	–	2.4	µSec.
0 °C to +70 °C	–	–	2.4	µSec.
-55 °C to +125 °C	–	–	2.4	µSec.
No missing codes				
+25 °C	14	–	–	Bits
0 °C to +70 °C	13	–	–	Bits
-55 °C to +125 °C	12	–	–	Bits
POWER REQUIREMENTS				
Power Supply Range				
+15V dc Supply	+14.25	+15	+15.75	Volts dc
-15V dc Supply	-14.25	-15	-15.75	Volts dc
+5V dc Supply	+4.75	+5	+5.25	Volts dc
Supply Current				
+15V Supply	–	+20	+25	mA
-15V Supply	–	-20	-28	mA
+5V Supply ①	–	+65	+75	mA
Power Dissipation	–	925	1200	mW
Supply Rejection	–	–	±0.01	%FSR/%V
PHYSICAL/ENVIRONMENTAL				
Operating Temperature Range				
—MC Models	0	–	+70	° C
—MM Models	-55	–	+125	° C
Storage Temperature Range	-65	–	+150	° C
Package Type	24-pin hermetically sealed ceramic DIP			
Weight	0.42(12)oz.(gram)			

① + 5V power usage at 1 TTL logic loading per data output bit.

TECHNICAL NOTES

1. Applications unaffected by endpoint errors or those that remove them through software will use the typical connections shown in Figure 2. The optional external circuitry of Figure 4 removes system errors or helps adjust the small initial errors of the ADC-914 to zero. The external adjustment circuit has no affect on the throughput rate. Table 1 shows how to select the input range.

2. Bypass the analog and digital supplies and the +10V reference (pin 21) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 21) to ground (pin 23).

CALIBRATION

1. Apply a pulse 200 nanoseconds minimum to the START CONVERT input (pin 16) at a rate of 250 KHz. That rate is chosen to reduce flicker if LED's are used on the outputs for calilbration purposes.

   Connect the converter per Figure 2, Figure 4, and Table 1 for the appropriate full scale range (FSR).

2. Zero Adjustments:
   Apply a precision voltage reference source between the amplifier's signal input and analog ground. Use a very low-noise signal source for accurate calibration.

   Adjust the output of the reference source per Table 4. For unipolar operation, adjust the zero trimming potentiometer so that the output code flickers between 00 0000 0000 0000 and 00 0000 0000 0001. For bipolar operation, adjust the potentiometer such that the code flickers equally between 10 0000 0000 0000 and 10 0000 0000 0001.

3. Full-Scale Adjustment:
   Set the output of the voltage reference used in step 2 to the value shown in Table 4. Adjust the gain trimming potentiometer so that the output code flickers between 11 1111 1111 1110 and 11 1111 1111 1111.

   To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in table 6.

Table 1. Input Connections

INPUT RANGE	INPUT PIN	JUMPER THESE PINS:
0 to -10V dc	Pin 19	Pin 20 to GROUND
±5V dc	Pin 19	Pin 20 to Pin 21

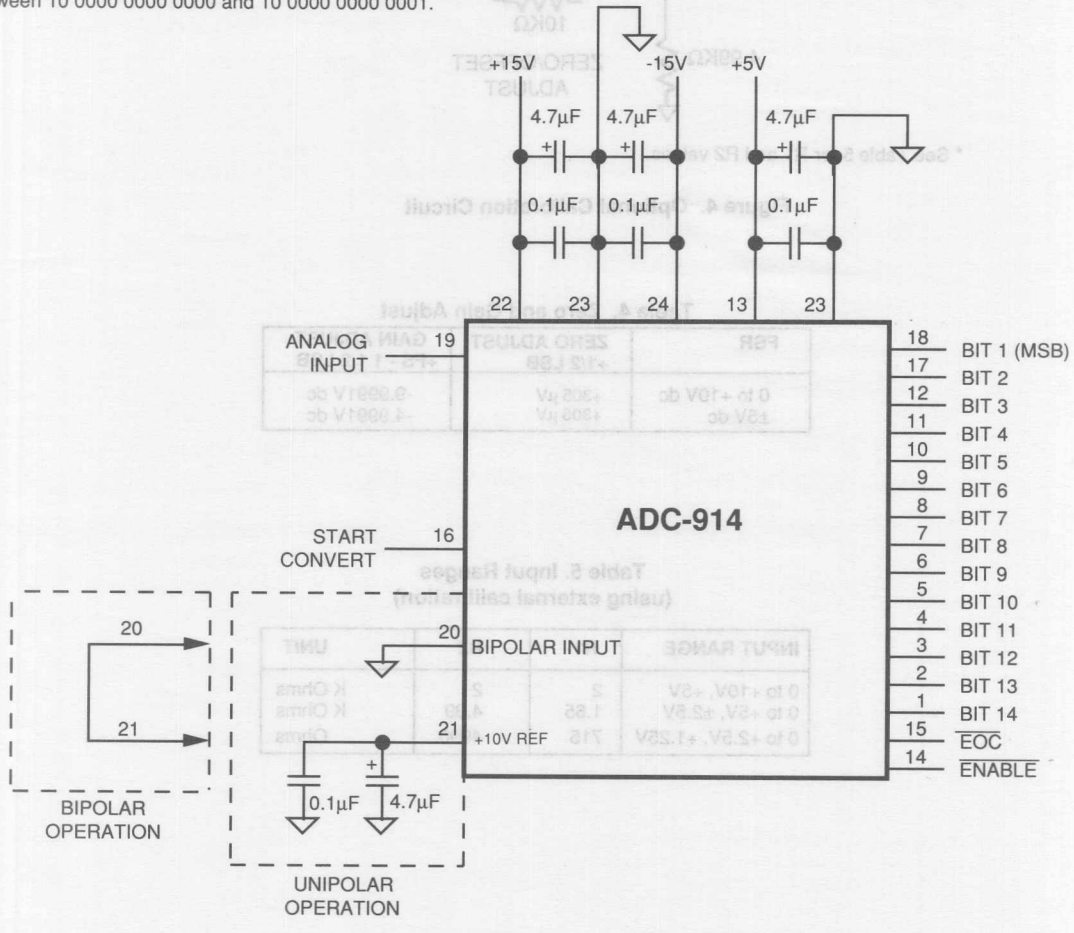
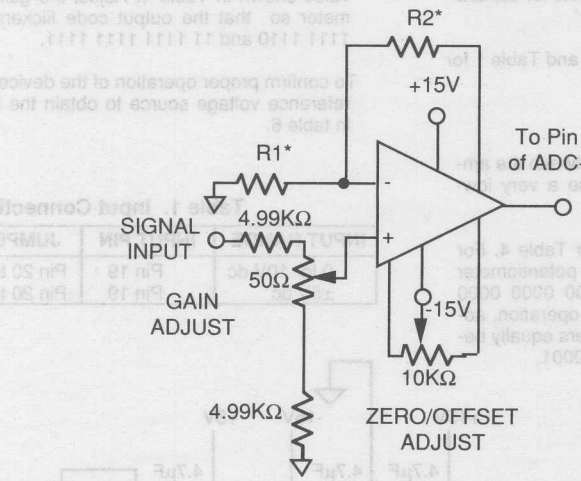


Figure 2. Typical Input Connections for the ADC-914

Optional Calibration Circuit



* See Table 5 for R1 and R2 values.

Figure 4. Optional Calibration Circuit

Table 4. Zero and Gain Adjust

FSR	ZERO ADJUST +1/2 LSB	GAIN ADJUST +FS - 1 1/2 LSB
0 to +10V dc	+305 µV	-9.9991V dc
±5V dc	+305 µV	-4.9991V dc

Table 5. Input Ranges (using external calibration)

INPUT RANGE	R1	R2	UNIT
0 to +10V, +5V	2	2	K Ohms
0 to +5V, ±2.5V	1.65	4.99	K Ohms
0 to +2.5V, +1.25V	715	4990	Ohms

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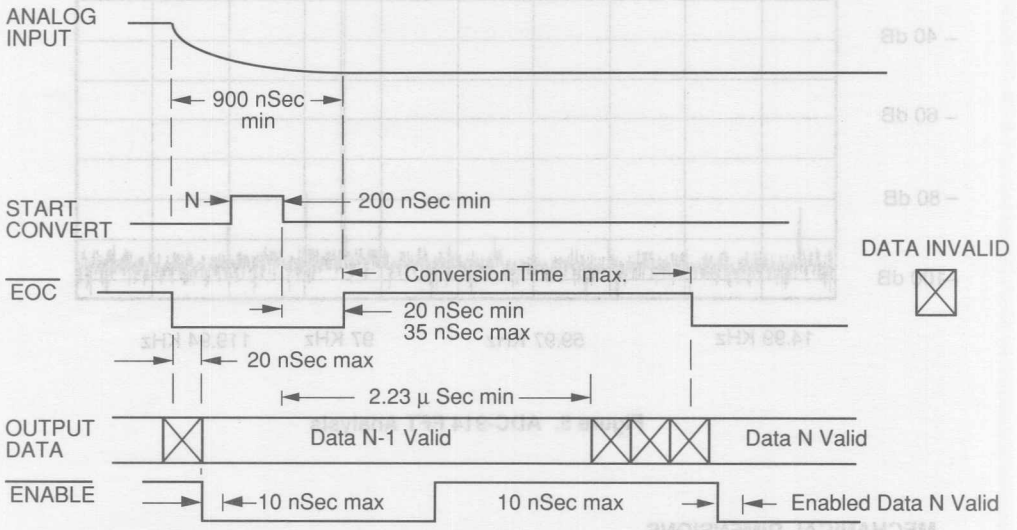
TIMING

Figure 3 shows the relationship between the various input signals. The timing shown applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.



NOTE: NOT DRAWN TO SCALE

Figure 3. ADC-914 Timing Diagram

Table 6. Output Coding

		STRAIGHT BIN.		
UNIPOLAR SCALE	**INPUT RANGES, V dc 0 to +10V**	**MSB LSB**	**INPUT RANGE ±5V**	**BIPOLAR SCALE**
+FS -1 LSB	+9.99939V	1111 1111 1111	+4.99939V	+FS -1 LSB
7/8 FS	+8.7500V	1110 0000 0000	+3.7500V	+3/4 FS
3/4 FS	+7.5000V	1100 0000 0000	+2.5000V	+1/2 FS
1/2 FS	+5.0000V	1000 0000 0000	0.0000V	0
1/4 FS	+2.5000V	0100 0000 0000	-2.5000V	-1/2 FS
1/8 FS	+1.2500V	0010 0000 0000	-3.7500V	-3/4 FS
1 LSB	+0.00061V	0000 0000 0001	-4.99939V	-FS +1 LSB
0	0.0000V	0000 0000 0000	-5.0000V	-FS
		OFF. BINARY		

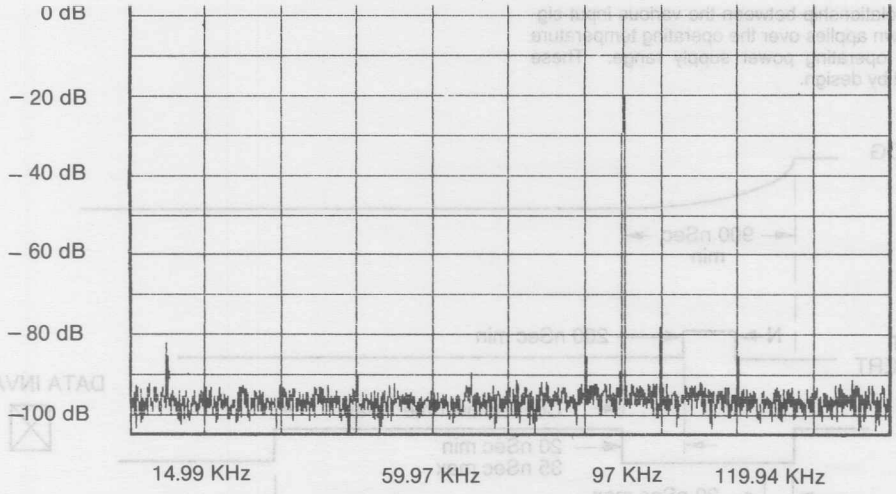
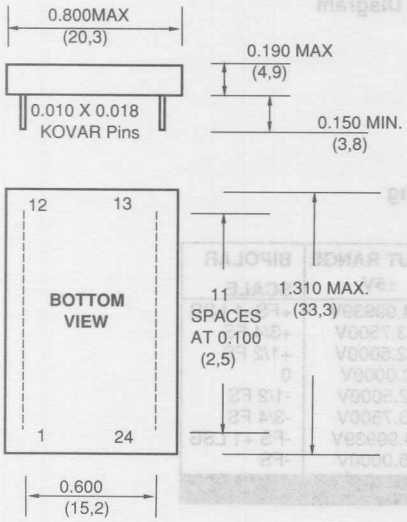


Figure 5. ADC-914 FFT Analysis

MECHANICAL DIMENSIONS
INCHES (MM)



NOTE: Pins have a 0.025 inch, ±0.01 stand-off from case.

ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	SEAL
ADC-914MC	0 °C to +70 °C	Hermetic
ADC-914MM	-55 °C to +125 °C	Hermetic

A receptacle for PC board mounting can be ordered through AMP Incorporated, #3-331272-8 (Component Lead Socket), 24 required.

For availability of MIL-STD-883 Versions, contact DATEL.

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ADC-HC12B

12-Bit, Low-Power A/D Converter

FEATURES

- **Single supply operation**
- **Automatic standby mode control**
- **Low power consumption**
- **Six input ranges**
- **MIL temperature ranges available**

GENERAL DESCRIPTION

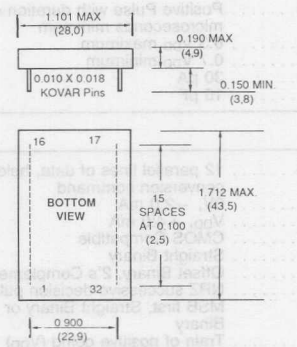
The ADC-HC is a complete, 12-bit, low-power, analog-to-digital converter utilizing CMOS technology. This hybrid IC incorporates active laser trimming of highly stable thin-film resistors to provide module performance with IC price, size and reliability.

The device is ideal for portable and remote applications such as seismology, oceanography, meteorology, and pollution monitoring. Other key applications include military and aerospace, requiring wide operating temperature ranges and high reliability.

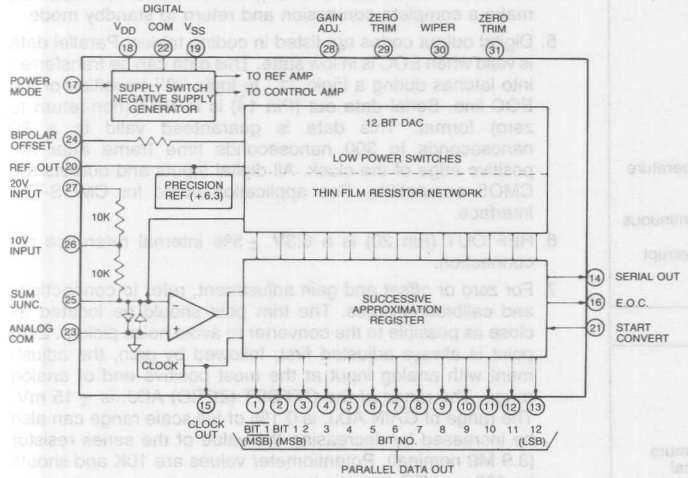
The ADC-HC converter can operate from either a single +9V dc to +15V dc power source (interrupt power mode) or from a ±9V dc to ±15V dc power source (continuous power mode) at a maximum conversion rate of 3.3 KHz.

A key feature of this unit when operating in the interrupt power mode is the extremely low quiescent power consumption (less than 10 µA at 12V, 25°C).

MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	17	POWER MODE
2	BIT 1 (MSB)	18	V_{DD}
3	BIT 2	19	V_{SS}
4	BIT 3	20	REF OUT
5	BIT 4	21	START CONVERT
6	BIT 5	22	DITITAL COM.
7	BIT 6	23	ANALOG COM.
8	BIT 7	24	BIPOLAR OFFSET
9	BIT 8	25	SUM. JUNC.
10	BIT 9	26	10V INPUT
11	BIT 10	27	20V INPUT
12	BIT 11	28	GAIN ADJ.
13	BIT 12 (LSB)	29	ZERO TRIM
14	SERIAL OUT	30	ZERO ADJ (WIPER)
15	CLOCK OUT	31	ZERO TRIM
16	E.O.C. (STATUS)	32	N.C.

ABSOLUTE MAXIMUM RATINGS	
Positive Supply (V_{DD})	+18V
Negative Supply (V_{SS})	−18V
Analog Inputs	±25V
Digital Inputs	0 to V_{DD}

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±12V, unless otherwise noted.

INPUTS	
Analog Input Ranges, unipolar	0 to +5V, 0 to +10V, 0 to +20V
Analog Input Ranges, bipolar	±2.5V, ±5V, ±10V
Input Impedance	5K (0 to +5V, ±2.5V) 10K (0 to +10V, ±5V) 20K (0 to +20V, ±10V)
Start Convert, Interrupt Mode	Positive Pulse with duration of 50 microseconds minimum
Start Convert, Continuous Mode	Positive Pulse with duration of 5 microseconds minimum
V_{IL} (Logic "0")	0.3 V_{DD} maximum
V_{IH} (Logic "1")	0.7 V_{DD} minimum
Input Current	30 pA
Input Capacitance	15 pF

OUTPUTS	
Parallel Output Data	12 parallel lines of data, held until next conversion command
V_{OL} (Logic "0")	0V, −2.0 mA
V_{OH} (Logic "1")	V_{DD}, +4.0 mA
All Digital Outputs	CMOS Compatible
Coding, unipolar	Straight Binary
Coding, bipolar	Offset Binary, 2's Complement
Serial Output	NRZ successive decision pulses out MSB first, Straight Binary or Offset Binary
Clock Output	Train of positive going (V_{DD}) 25 microseconds pulses, 40 kHz
E.O.C. (Status)	Conversion Status Signal, Logic "1" during reset and conversion, Logic "0" when conversion complete (data valid)

PERFORMANCE	
Resolution	12 Bits
Nonlinearity	±½ LSB maximum
Differential Nonlinearity	±½ LSB maximum
Gain Error	Adjust to zero
Offset or Zero Error	Adjust to zero
Gain Tempco	±30 ppm/°C maximum
Offset Tempco	±20 ppm/°C of FSR maximum
Zero Tempco	±10 ppm/°C of FSR
Diff. Nonlinearity Tempco	±2 ppm/°C of FSR
No Missing Codes	Guaranteed over operating temperature range
Conversion Time	300 microseconds maximum
Throughput Time	305 microseconds maximum continuous power mode 350 microseconds maximum interrupt power mode
Power Supply Rejection	003%/% Supply

POWER REQUIREMENTS	
Continuous Power Mode	
V_{DD}	+9.0V to +15.0V
V_{SS}	−9.0V to −15.0V
Interrupt Power Mode V_{DD}	+9V to +15.0V
Power Consumption, Continuous Mode	165 mW typical, 200 mW maximum
Power Consumption, Quiescent Mode	150 µW maximum, 15 µW typical

PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0 °C to +70 °C (BMC) -55 °C to +125 °C (BMM, BMM-QL)
Storage Temperature Range	−65°C to +150°C
Package Type	Ceramic
Pins	0.010 x 0.018 inch Kovar
Weight	0.5 ounces (14 g.)

TECHNICAL NOTES

1. The ADC-HC contains CMOS components and must be properly handled to prevent damage from static pick-up. Proper anti-static handling procedures should be observed including storage in conductive foam or shorting all pins together with aluminum foil. Do not connect in circuit under "power on" conditions. Digital signals should be applied after the converter's power has been turned on.
2. For single supply (+12V nominal) or dual supply (±12V nominal) operation, bypass the power input pins to ground with a 0.1 µF ceramic capacitor. It is not critical that the supplies be balanced.
3. Analog and digital grounds should be kept separate whenever possible to prevent digital signals from flowing in the analog ground circuit and inducing spurious analog signal noise. Analog Common (Pin 23) and Digital Ground (Pin 22) are not connected internally and must be tied together externally.
4. The ADC-HC can operate from either a single or dual supply. When using dual supplies, tie POWER MODE (Pin 17) to V_{DD} (Pin 18). In this continuous power mode, an A/D conversion will take place when a 5 microseconds or greater positive going pulse is applied to START CONVERT (Pin 21). For single supply operation (interrupt power mode), tie Power Mode (Pin 17) to E.O.C. (Pin 16). When EOC goes low, the converter is switched to standby mode (power is disconnected to analog circuitry) and digital output data becomes valid and remains valid until next start pulse is applied. Upon receipt of a 50 microseconds minimum, 500 microseconds maximum pulse on START CONVERT (Pin 21), the converter will stabilize, make a complete conversion and return to standby mode.
5. Digital output codes are listed in coding tables. Parallel data is valid when EOC is in low state. This data can be transferred into latches during a logic "1" to logic "0" transition of the EOC line. Serial data out (Pin 14) is in NRZ (non-return to zero) format. This data is guaranteed valid in a 50 nanoseconds to 300 nanoseconds time frame after the positive edge of the clock. All digital inputs and outputs are CMOS compatible. See application notes for CMOS-TTL interface.
6. REF OUT (Pin 20) is a 6.3V ±5% internal reference pin connection.
7. For zero or offset and gain adjustment, refer to connections and calibration notes. The trim pots should be located as close as possible to the converter to avoid noise pickup. Zero point is always adjusted first, followed by gain, the adjustment with analog input at the most positive end of analog range. The range of the OFFSET (ZERO) ADJ. is ±15 mV. The range of GAIN ADJ. is 0.1% of full scale range can also be increased by decreasing the value of the series resistor (3.9 MΩ nominal). Potentiometer values are 10K and should be 100 ppm/°C ceramic type.

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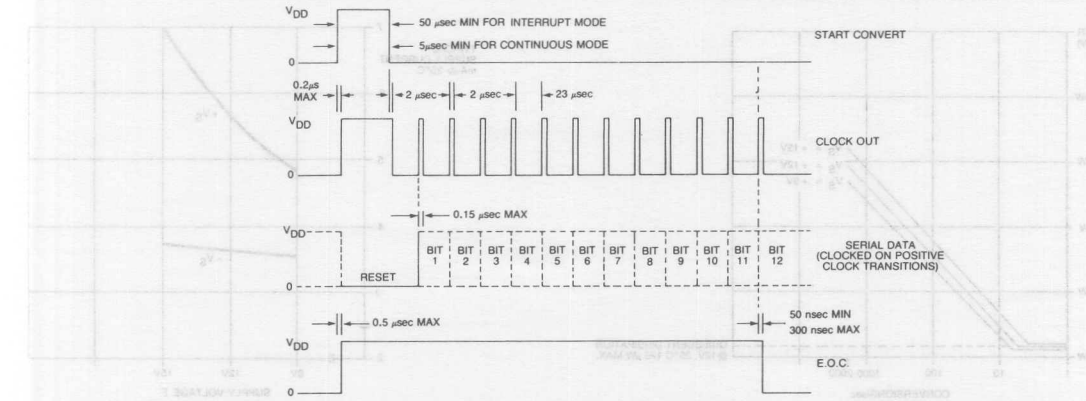
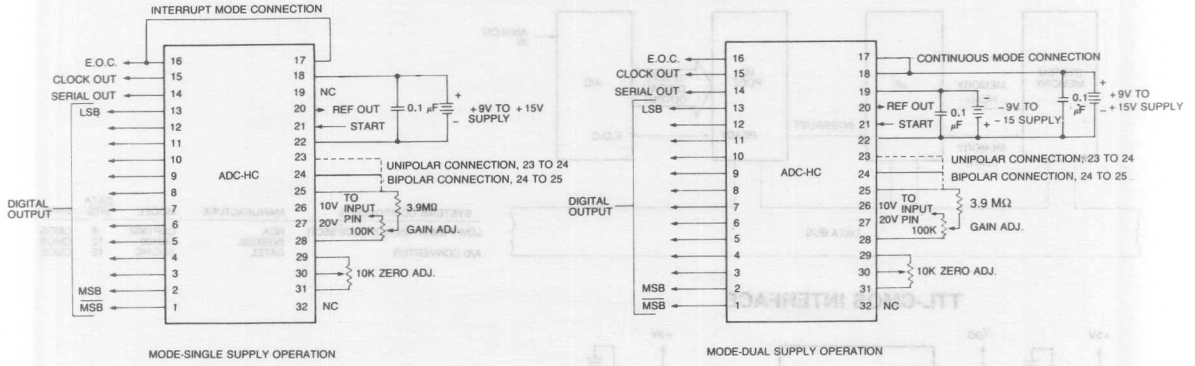
CONNECTIONS AND CALIBRATION

ADC-HC TIMING DIAGRAM



CONNECTIONS DIAGRAM



OUTPUT CODING

INPUT VOLTAGE RANGE				CODING	
	UNIPOLAR			STRAIGHT BINARY	
	0 to +20V	0 to +10V	0 to +5V	MSB	LSB
+FS – 1 LSB	+19.9951	+9.9976	+4.9988	1111 1111	1111
+½FS	+10.0000	+5.0000	+2.5000	1000 0000	0000
+1 LSB	+0.0049	+0.0024	+0.0012	0000 0000	0001
ZERO	0.0000	0.0000	0.0000	0000 0000	0000

	BIPOLAR			OFFSET BINARY*	
	±10V	±5V	±2.5V	MSB	LSB
+FS – 1 LSB	+9.9951	+4.9976	+2.4988	1111 1111	1111
+½FS	+5.0000	+2.5000	+1.2500	1100 0000	0000
+1 LSB	+0.0049	+0.0024	+0.0012	1000 0000	0001
ZERO	0.0000	0.0000	0.0000	1000 0000	0000
–FS – 1 LSB	–9.9951	–4.9976	–2.4988	0000 0000	0001
–FS	–10.0000	–5.0000	–2.5000	0000 0000	0000

*For 2's COMPLEMENT, MSB is inverted, use $\overline{\text{MSB}}$ (pin 1)

INPUT PIN CONNECTIONS

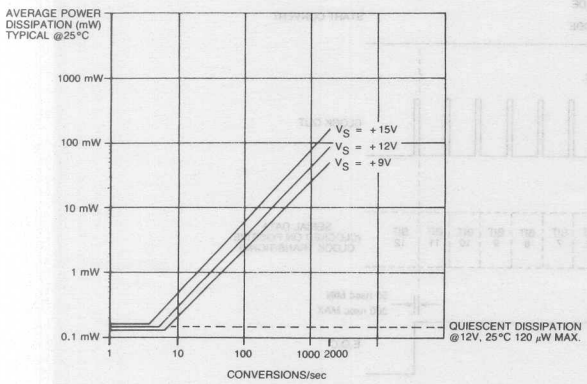
INPUT VOLTAGE RANGE	INPUT PIN	CONNECT THESE PINS TOGETHER
0 to +5V	26	23 to 24, 25 to 27
0 to +10V	26	23 to 24
0 to +20V	27	23 to 24
±2.5V	26	24 to 25, 25 to 27
±5V	26	24 to 25
±10V	27	24 to 25

CALIBRATION PROCEDURE

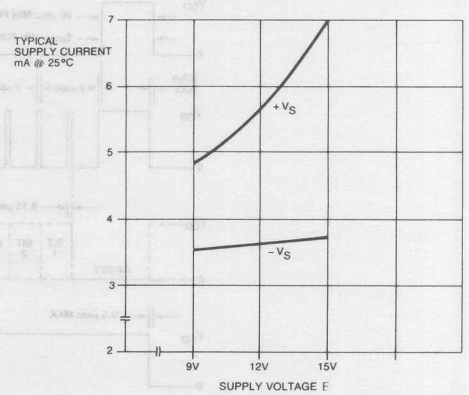
1. Connect the converter as shown in the Connection Diagram. Use the Input Pin Connections table for the desired input voltage range. Apply start conversion pulses to start pin.
2. **Zero and Offset Adjustment**
   Apply a precision voltage reference source between the selected analog input range and ground. Adjust the output of the reference source to +½ LSB. Adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 for unipolar and 1000 0000 0000 and 1000 0000 0001 for bipolar mode.
3. **Full Scale Adjustment**
   Change the output of the precision reference source for +FS – 1½ LSB. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111.
4. For bipolar operation, the offset and Full Scale Adjustment are interactive. Repeat the offset and Full Scale Adjustment procedure as necessary until both points are set.

APPLICATIONS

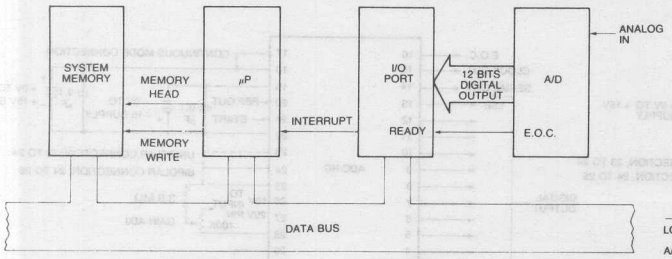
ADC-HC INTERRUPT POWER MODE



ADC-HC CONTINUOUS POWER MODE

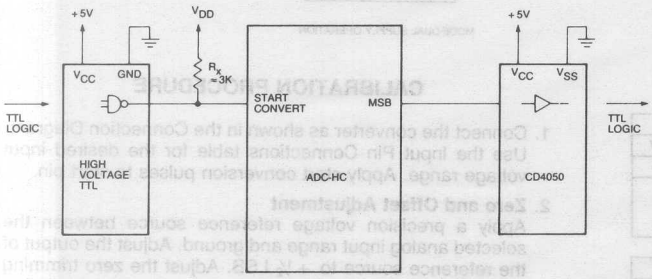


LOW POWER MICRO-PROCESSOR INTERFACE



SYSTEMS COMPONENTS	MANUFACTURE	MODEL	DATA BITS	TYPE
LOW POWER MICROPROCESSOR	RCA	CDP1802	8	CMOS
	INTERSIL	IM6100	12	CMOS
A/D CONVERTER	DATEL	ADC-HC	12	CMOS

TTL-CMOS INTERFACE



CMOS and TTL logic are not compatible due to different threshold levels. They can, however, be interfaced by simple techniques.

The START CONVERT (Pin 21) can be driven directly from an open collector, high voltage TTL gate. Resistor Rx is used to source current and bring the TTL output up to the CMOS threshold level. Typical values of Rx are 3.3K to 10K ohms.

CMOS to TTL interface requires sufficient sink current in the low state. The CD4049 (inverting) and CD4050 (noninverting) buffers, powered from +5V logic supply can accept input voltage swings of +5 to +15V from the CMOS system. Each buffer gate can drive at least one input from any TTL family.

ORDERING INFORMATION

MODEL	TEMP. RANGE	SEAL
ADC-HC12BMC	0 to +70 °C	Hermetic
ADC-HC12BMM	-55 to +125 °C	Hermetic
ADC-HC12BMM-QL	-55 to +125 °C	Hermetic

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ADC-HS12B

12-Bit A/D Converter With Sample-Hold

FEATURES

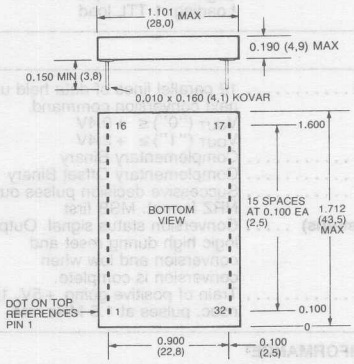
- **12-Bit resolution**
- **Internal sample and hold**
- **6 Microseconds acquisition time**
- **9 Microseconds conversion time**
- **Programmable input ranges**
- **Parallel & serial outputs**

GENERAL DESCRIPTION

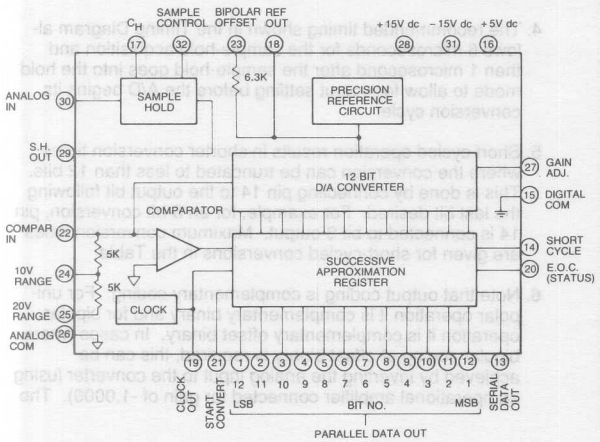
The ADC-HS12B is a high performance 12-bit hybrid A/D converter with a self-contained sample-hold. It is specifically designed for systems applications where the sample-hold is an integral part of the conversion process. The internal sample-hold has a 6 microseconds acquisition time for a full 10V dc input change; the A/D converter has a fast 9 microseconds conversion time. Five input voltage ranges are programmable by external pin connection; 0 to +5V, 0 to+10V, ±2.5V, ±5V, and ±10V. Input impedance to the sample-hold is 100 megohms. Output coding is complementary binary for unipolar operation and complimentary offset binary for bipolar operation, with both parallel and serial outputs brought out.

The ADC-HS12B uses a fast 12-bit monolithic DAC which includes a precision zener reference source. The circuit also contains a fast monolithic 12-bit successive approximation register, a clock and a monolithic sample-hold.

MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 OUT (LSB)	17	C_H
2	BIT 11 OUT	18	REF OUT
3	BIT 10 OUT	19	CLOCK OUT
4	BIT 9 OUT	20	E.O.C. (STATUS)
5	BIT 8 OUT	21	START CONVERT
6	BIT 7 OUT	22	COMPAR INPUT
7	BIT 6 OUT	23	BIPOLAR OFFSET
8	BIT 5 OUT	24	10V RANGE
9	BIT 4 OUT	25	20V RANGE
10	BIT 3 OUT	26	ANALOG COM
11	BIT 2 OUT	27	GAIN ADJ.
12	BIT 1 OUT (MSB)	28	+15V POWER
13	SERIAL DATA OUT	29	S.H. OUTPUT
14	SHORT CYCLE	30	ANALOG IN
15	DIGITAL COM	31	-15V POWER
16	+5V POWER	32	SAMPLE CONTROL

Logic Supply Voltage, pin 16	+5.5V
Digital Input Voltage, pins 14, 21, 32	+5.5V
Analog Input Voltage, pin 30	±15V

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V and +5V supplies unless otherwise noted.

INPUTS	
Analog Input Ranges, unipolar	0 to +5V, 0 to +10V
Analog Input Ranges, bipolar	±2.5V, ±5V, ±10V
Input Impedance[1]	100 megohms
Input Bias Current[1]	50 nA typical, 200 nA max.
Start Conversion	2V min. to +5.5V max. positive pulse with 100 nsec. duration min. Rise and fall times <30 nsec. Logic high to low transition resets converter and initiates next conversion. Loading: 2 TTL loads
Sample Control Input	Logic high = hold Logic low = sample Loading: 1 TTL load
OUTPUTS[2]	
Parallel Output Data	12 parallel lines of data held until next conversion command. V_{OUT} ("0") ≤ +0.4V V_{OUT} ("1") ≥ +2.4V
Coding, unipolar	Complementary Binary
Coding, bipolar	Complementary Offset Binary
Serial Output Data	Successive decision pulses out, NRZ format. MSB first
End of Conversion (status)	Conversion status signal. Output is logic high during reset and conversion and low when conversion is complete.
Clock Output	Train of positive going +5V, 100 nsec. pulses at 1.5 MHz rate.
SAMPLE-HOLD PERFORMANCE[3]	
Input Offset Drift	25 μV/°C
Acquisition Time, 10V to 0.01%	6 μsec.
Bandwidth	1 MHz
Aperture Delay Time	100 nsec.
Aperture Uncertainty Time	10 nsec.
Sample to Hold Error	2.5 mV max.
Hold Mode Droop	200 nV/μsec. max.
Hold Mode Feedthrough	0.01% max.
CONVERTER PERFORMANCE	
Resolution	12 bits (1 part in 4096)
Nonlinearity	±½ LSB max.
Differential Nonlinearity	±¾ LSB max.
Temp. Coefficient of Gain	±20 ppm/°C max.
Temp. Coefficient of Zero, unipolar	±5 ppm/°C of FSR max.
Temp. Coefficient of Offset, bipolar	±10 ppm/°C of FSR max.
Differential Nonlinearity Tempco	±2 ppm/°C of FSR
Missing Codes	None over oper. temp. range
Conversion Time	9 μsec. max.
Power Supply Rejection	0.004%/% max.
POWER REQUIREMENTS	
Power Suppy Voltage	+15V dc ±0.5V at 20 mA −15V dc ±0.5V at 25 mA +5V dc ±0.25V at 85 mA

Storage Temperature Range	−65°C to +150°C
Package Type	32 pin ceramic
Pins	0.010 x 0.018 inch Kovar
Weight	0.5 ounce (14 grams)

FOOTNOTES:

1. For sample-hold input
2. All digital outputs can drive 2 TTL loads
3. For 1000 pF external hold capacitor

TECHNICAL NOTES

1. It is recommended that the ±15V power input pins both be bypassed to ground with a 0.01 μF ceramic capacitor in parallel with a 1 μF electrolytic capacitor and the +5V power input pin be bypassed to ground with a 1 μF electrolytic capacitor as shown in the connection diagrams. In addition, pin 27 should be bypassed to ground with a 0.01 μF ceramic capacitor. These precautions will assure noise free operation of the converter.

2. Digital Common (pin 15) and Analog Common (pin 26) are not connected together internally, and therefore must be connected as directly as possible externally. It is recommended that a ground plane be run underneath the case between the two commons. Analog ground and ±15V power ground should be run to pin 26 whereas digital ground and +5V dc ground should be run to pin 15.

3. External adjustment of zero or offset and gain are provided for by trimming potentiometers connected as shown in the connection diagrams. The potentiometer values can be between 10K and 100K ohms and should be 100 ppm/°C, cermet types. The adjustment range is ±0.5% of FSR for zero or offset and ±0.3% for gain. The trimming pots should be located as close as possible to the converter to avoid noise pickup. Calibration of the ADC-HS12B is performed with the sample-hold connected and operating dynamically. This results in adjusting out the sample-hold errors along with the A/D converter. For slow throughput applications it is recommended that a 0.01 μF hold capacitor be used for best accuracy. With this value the acquisition time becomes 25 microseconds and the external timing must be adjusted accordingly.

4. The recommended timing shown in the Timing Diagram allows 6 microseconds for the sample-hold acquisition and then 1 microsecond after the sample-hold goes into the hold mode to allow for output settling before the A/D begins its conversion cycle.

5. Short cycled operation results in shorter conversion times where the conversion can be truncated to less than 12 bits. This is done by connecting pin 14 to the output bit following the last bit desired. For example, for an 8-bit conversion, pin 14 is connected to bit 9 output. Maximum conversion times are given for short-cycled conversions in the Table.

6. Note that output coding is complementary coding. For unipolar operation it is complementary binary and for bipolar operation it is complementary offset binary. In cases where bipolar coding of offset binary is required, this can be achieved by inverting the analog input to the converter (using an operational amplifier connected for gain of -1.0000). The

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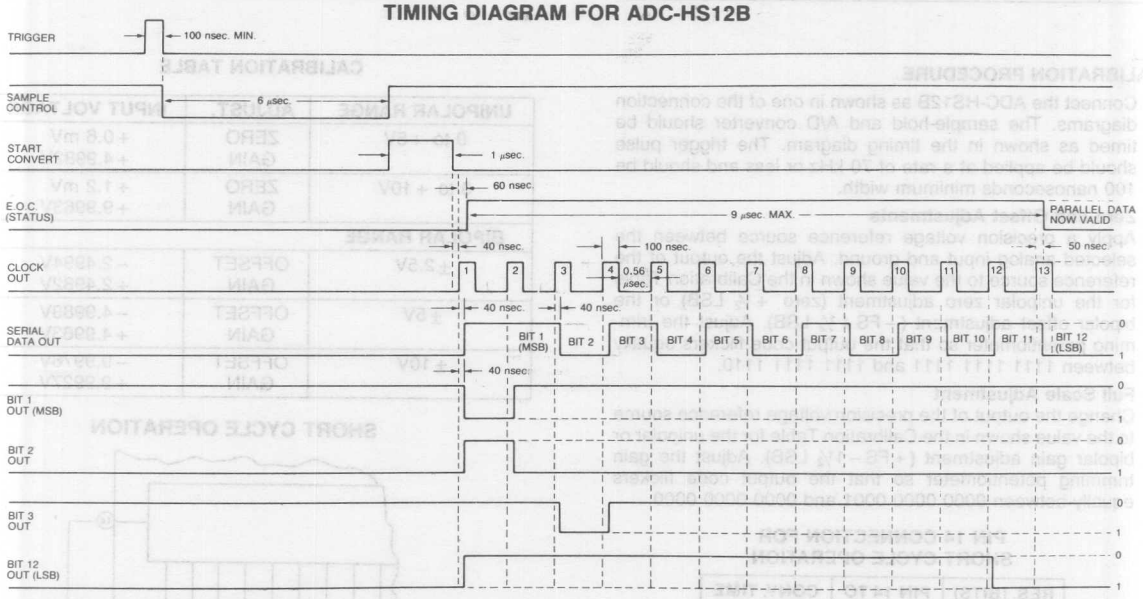
converter is then calibrated so that –FS analog input gives an output code of 0000 0000 0000, and +FS – 1 LSB gives 1111 1111 1111.

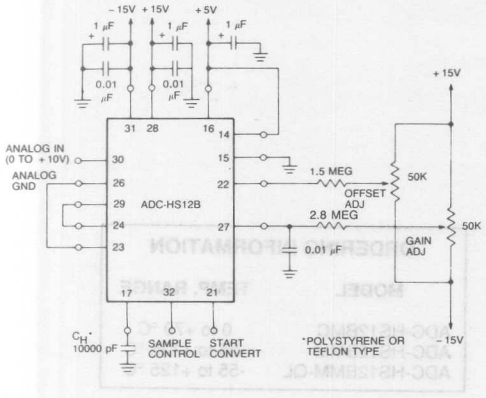
7. These converters dissipate 1.81 watts maximum of power. The case to ambient thermal resistance is approximately 25°C per watt. For ambient temperatures above 50°C, care should be taken not to restrict air circulation in the vicinity of the converter.
8. These converters can be operated with an external clock. To accomplish this, a negative pulse train is applied to START CONVERT (Pin 21). The rate of the external clock must be lower than the rate of the internal clock. The pulse width of the external clock should be between 100 nanoseconds and 300 nanoseconds. Each N bit conversion cycle requires a pulse train of N + 1 clock pulses for completion, e.g., an 8-bit conversion requires 9 clock pulses for completion. A continuous pulse train may be used for consecutive conversions, resulting in an N bit conversion every N + 1 pulses, or the E.O.C. output may be used to gate a continuous pulse train for single conversions.

TIMING DIAGRAM FOR ADC-HS12B

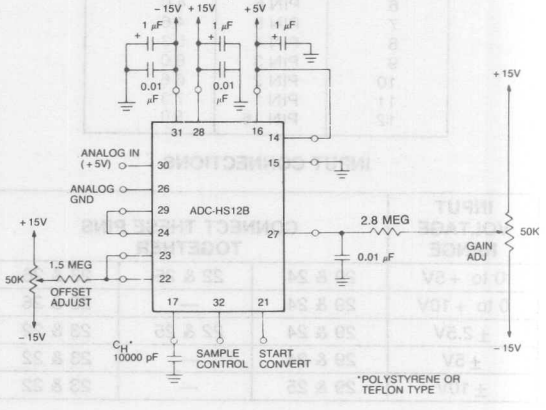


NOTE: TRIGGER, SAMPLE CONTROL, AND START CONVERT PULSES MUST BE EXTERNALLY GENERATED

UNIPOLAR OPERATION, 0 TO +10V



BIPOLAR OPERATION, ±5V



CODING TABLES

UNIPOLAR OPERATION

INPUT RANGE		COMP. BINARY CODING	
0 TO +10V	0 TO +5V	MSB	LSB
+9.9976V	+4.9988V	0000 0000 0000	
+8.7500	+4.3750	0001 1111 1111	
+7.5000	+3.7500	0011 1111 1111	
+5.0000	+2.5000	0111 1111 1111	
+2.5000	+1.2500	1011 1111 1111	
+1.2500	+0.6250	1101 1111 1111	
+0.0024	+0.0012	1111 1111 1110	
0.0000	0.0000	1111 1111 1111	

BIPOLAR OPERATION

INPUT VOLTAGE RANGE			COMP. OFFSET BINARY	
±10V	±5V	±2.5V	MSB	LSB
+9.9951V	+4.9976V	+2.4988V	0000 0000 0000	
+7.5000	+3.7500	+1.8750	0001 1111 1111	
+5.0000	+2.5000	+1.2500	0011 1111 1111	
0.0000	0.0000	0.0000	0111 1111 1111	
−5.0000	−2.5000	−1.2500	1011 1111 1111	
−7.5000	−3.7500	−1.8750	1101 1111 1111	
−9.9951	−4.9976	−2.4988	1111 1111 1110	
−10.0000	−5.0000	−2.5000	1111 1111 1111	

CALIBRATION PROCEDURE

1. Connect the ADC-HS12B as shown in one of the connection diagrams. The sample-hold and A/D converter should be timed as shown in the timing diagram. The trigger pulse should be applied at a rate of 70 kHz or less and should be 100 nanoseconds minimum width.
2. **Zero and Offset Adjustments**
   Apply a precision voltage reference source between the selected analog input and ground. Adjust the output of the reference source to the value shown in the Calibration Table for the unipolar zero adjustment (zero +½ LSB) or the bipolar offset adjustment (−FS+½ LSB). Adjust the trimming potentiometer so that the output code flickers equally between 1111 1111 1111 and 1111 1111 1110.
3. **Full Scale Adjustment**
   Change the output of the precision voltage reference source to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (+FS−1½ LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 0000 0000 0001 and 0000 0000 0000.

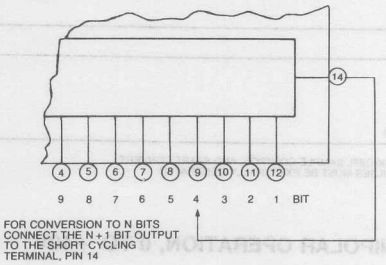
CALIBRATION TABLE

UNIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
0 to +5V	ZERO GAIN	+0.6 mV +4.9982V
0 to +10V	ZERO GAIN	+1.2 mV +9.9963V
BIPOLAR RANGE		
±2.5V	OFFSET GAIN	−2.4994V +2.4982V
±5V	OFFSET GAIN	−4.9988V +4.9963V
±10V	OFFSET GAIN	−9.9976V +9.9927V

PIN 14 CONNECTION FOR SHORT CYCLE OPERATION

RES. (BITS)	PIN 14 TO	CONV. TIME
1	PIN 11	0.7 µsec
2	PIN 10	1.3
3	PIN 9	2.0
4	PIN 8	2.6
5	PIN 7	3.3
6	PIN 6	4.0
7	PIN 5	4.6
8	PIN 4	5.3
9	PIN 3	6.0
10	PIN 2	6.6
11	PIN 1	7.3
12	PIN 16	9.0

SHORT CYCLE OPERATION



INPUT CONNECTIONS

INPUT VOLTAGE RANGE	CONNECT THESE PINS TOGETHER		
0 to +5V	29 & 24	22 & 25	23 & 26
0 to +10V	29 & 24	—	23 & 26
±2.5V	29 & 24	22 & 25	23 & 22
±5V	29 & 24	—	23 & 22
±10V	29 & 25	—	23 & 22

ORDERING INFORMATION

MODEL	TEMP. RANGE
ADC-HS12BMC	0 to +70 °C
ADC-HS12BMM	-55 to +125 °C
ADC-HS12BMM-QL	-55 to +125 °C

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ADC-HX, ADC-HZ Series
12-Bit, Analog-to-Digital Converters

FEATURES

- 12-Bit resolution
- 8-or 20-Microseconds conversions
- 5 Input ranges
- Internal high Z buffer
- Short-cycle operation

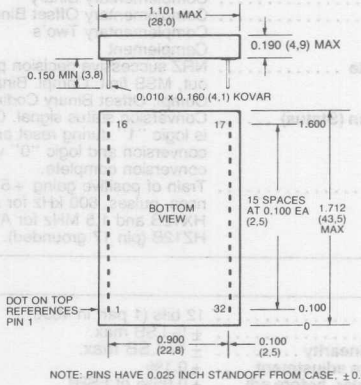
GENERAL DESCRIPTION

The ADC-HX12B and ADC-HZ12B are self-contained, high performance, 12-bit A/D converters manufactured with thick-and thin-film hybrid technology. They use the successive approximation conversion technique to achieve a 12-bit conversion in 20 and 8 microseconds respectively. Five input voltage ranges are programmable by external pin connection: 0 to +5V, 0 to +10V, ±2.5V, ±5V, and ±10V. An internal buffer amplifier is also provided for applications where 100 megohm input impedance is required.

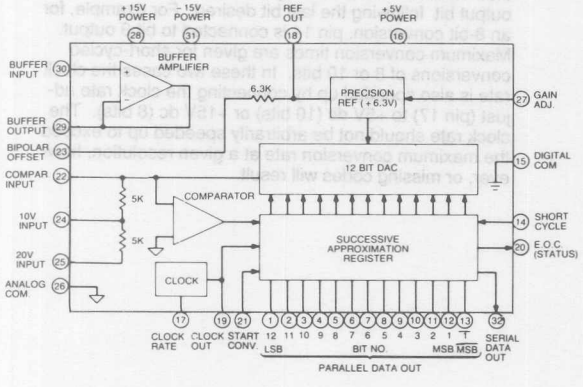
These converters utilize a fast 12-bit monolithic DAC which includes a precision zener reference source. The circuit also contains a fast monolithic comparator, a monolithic 12-bit successive approximation register, a clock and a monolithic buffer amplifier. Nonlinearity is specified at ±1/2 LSB maximum.

Both models have identical operation except for conversion speed. They can be short-cycled to give faster conversion in lower resolution applications. Use of the internal buffer amplifier increases conversion time by 3 microseconds, the settling time of the amplifier. Output coding is complementary binary, complementary offset binary, or complementary two's complement. Serial data is also brought out. The package is a 32-pin ceramic case.

MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 12 OUT (LSB)	17	CLOCK RATE
2	BIT 11 OUT	18	REF OUT
3	BIT 10 OUT	19	CLOCK OUT
4	BIT 9 OUT	20	E.O.C. (STATUS)
5	BIT 8 OUT	21	START CONVERT
6	BIT 7 OUT	22	COMPAR INPUT
7	BIT 6 OUT	23	BIPOLAR OFFSET
8	BIT 5 OUT	24	10V RANGE
9	BIT 4 OUT	25	20V RANGE
10	BIT 3 OUT	26	ANALOG COM
11	BIT 2 OUT	27	GAIN ADJ.
12	BIT 1 OUT (MSB)	28	+15V POWER
13	BIT 1 OUT (MSB)	29	BUFFER OUTPUT
14	SHORT CYCLE	30	BUFFER INPUT
15	DIGITAL COM	31	-15V POWER
16	+5V POWER	32	SERIAL OUTPUT

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V and +5V supplies unless otherwise noted.

INPUTS	ADC-HX12B ADC-HZ12B
Analog Input Ranges, unipolar	0 to +5V, 0 to +10V FS
Analog Input Ranges, bipolar	±2.5V, ±5V, ±10V FS
Input Impedance	2.5K (0 to +5V, ±2.5V) 5K (0 to +10V, ±5V) 10K (±10V)
Input Impedance with Buffer	100 Megohms
Input Bias Current of Buffer	125 nA typical, 250 nA max.
Input Overvoltage	±15V
Start Conversion	2V min. to 5.5V max. positive pulse with duration of 100 nsec. min. Rise and fall times <30 nsec. Logic "1" to "0" transition resets converter and initiates next conversion. Loading: 2 TTL loads
OUTPUTS[1]	
Parallel Output Data	12 parallel lines of data held until next conversion command. V_{OUT} ("0") ≤ +0.4V V_{OUT} ("1") ≥ +2.4V
Coding, unipolar	Complementary Binary
Coding, bipolar	Complementary Offset Binary Complementary Two's Complement
Serial Output Data	NRZ successive decision pulses out, MSB first. Compl. Binary or Compl. Offset Binary Coding
End of Conversion (Status)	Conversion status signal. Output is logic "1" during reset and conversion and logic "0" when conversion complete.
Clock Output	Train of positive going +5V 100 nsec. pulses. 600 kHz for ADC-HX12B and 1.5 MHz for ADC-HZ12B (pin 17 grounded).
PERFORMANCE	
Resolution	12 bits (1 part in 4096)
Nonlinearity	±½ LSB max.
Differential Nonlinearity	±¾ LSB max.
Gain Error, before adjustment	±0.1%
Zero Error, unipolar, before adj.	±0.05% of FSR[3]
Offset Error, bipolar, before adj.	±0.1% of FSR[3]
Temp. Coeff. of Gain	±20 ppm/°C max.
Temp. Coeff. of Zero, unipolar	±5 ppm/°C of FSR max.[3]
Temp. Coeff. of Offset, bipolar	±10 ppm/°C of FSR max.[3]
Diff. Nonlinearity Tempco	±2 ppm/°C of FSR[3]
No Missing Codes	Over oper. temp. range
Conversion Time[2], 12 bits	20 μsec. max. 8.0 μsec. max.
10 bits[4]	15 μsec. max. 6.0 μsec. max.
8 bits[4]	10 μsec. max. 4.0 μsec. max.
Buffer Settling Time, 10V step	3.0 μsec. to 0.01%
Power Supply Rejection	0.004%/% Supply max.
POWER REQUIREMENTS	
Power Supply Voltage	+15V dc ±0.5V dc at 20 mA −15V dc ±0.5V dc at 25 mA + 5V dc ±0.25V dc at 85 mA

PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0 to +70°C or −55 to +125°C
Storage Temperature Range	−65°C to +150°C
Package Size	1.700 x 1.100 x 0.160 inches
Package Type	32 pin ceramic
Pins	0.010 x 0.018 inch Kovar
Weight	0.5 ounces (14 grams)

FOOTNOTES:

1. All digital outputs can drive 2 TTL loads.
2. Without buffer amplifier used. ADC-HZ12B may require external adjustment of clock rate.
3. FSR is full scale range and is 10V for 0 to +10V or ±5V input and 20V for ±10V input.
4. Short cycled operation.

TECHNICAL NOTES

1. It is recommended that the ±15V power input pins both be bypassed to ground with a 0.01 μF ceramic capacitor in parallel with a 1 μF electrolytic capacitor and the +5V power input pin be bypassed to ground with a 10 μF electrolytic capacitor as shown in the connection diagrams. In addition, pin 27 should be bypassed to ground with a 0.01 μF ceramic capacitor. These precautions will assure noise free operation of the converter.

2. Digital Common (pin 15) and Analog Common (pin 26) are not connected together internally, and therefore must be connected as directly as possible externally. It is recommended that a ground plane be run underneath the case between the two commons. Analog ground and ±15V power ground should be run to pin 26 whereas digital ground and +5V dc ground should be run to pin 15.

3. External adjustment of zero or offset and gain are provided for by trimming potentiometers connected as shown in the connection diagrams. The potentiometer values can be between 10K and 100K ohms and should be 100 ppm/ °C cermet types. The adjustment range is ±0.2% of FSR for zero or offset and ±0.3% for gain. The trimming pots should be located as close as possible to the converter to avoid noise pickup. In some cases, for example 8 bit short-cycled operation, external adjustment may not be necessary.

4. Short-cycled operation results in shorter conversion times where the conversion can be truncated to less than 12 bits. This is done by connecting pin 14 to the output bit following the last bit desired. For example, for an 8-bit conversion, pin 14 is connected to bit 9 output. Maximum conversion times are given for short-cycled conversions of 8 or 10 bits. In these two cases the clock rate is also speeded up by connecting the clock rate adjust (pin 17) to +5V dc (10 bits) or +15V dc (8 bits). The clock rate should not be arbitrarily speeded up to exceed the maximum conversion rate at a given resolution, however, or missing codes will result.

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2's complement. In cases where bipolar coding of offset binary or 2's complement is required, this can be achieved by inverting the analog input to the converter (using an op amp connected for gain of −1.0000). The converter is then calibrated so that −FS analog input gives an output code of 0000 0000 0000, and +FS − 1 LSB gives 1111 1111 1111.

6. These converters dissipate 1.7 watts maximum of power. The case to ambient thermal resistance is approximately 25°C per watt. For ambient temperatures above 50°C, care should be taken not to restrict air circulation in the vicinity of the converter.
7. These converters can be operated with an external clock. To accomplish this, a negative pulse train is applied to START CONVERT (Pin 21). The rate of the external clock must be lower than the rate of the internal clock as adjusted (see clock rate adjustment diagram) for the converter resolution selected. The pulse width of the external clock should be between 100 nanoseconds and 300 nanoseconds. Each N-bit conversion cycle requires a pulse train of N + 1 clock pulses for completion, e.g., an 8-bit conversion requires 9 clock pulses for completion. A continuous pulse train may be used for consecutive conversions, resulting in an N-bit conversion every N + 1 pulses, or the E.O.C. output may be used to gate a continuous pulse train for single conversions.
8. When the input buffer amplifier is used, a delay equal to its settling time must be allowed between the input level change, such as a multiplexer channel change, and the negative-going edge of the START CONVERSION pulse. If the buffer is not required, its input (pin 30) should be tied to ANALOG GROUND (pin 26). This prevents the unused amplifier from introducing noise into the converter. For applications not using the internal buffer, the converter must be driven from a source with an extremely low input impedance.

Input Connections

INPUT VOLT. RANGE	WITHOUT BUFFER			WITH BUFFER			
	INPUT PIN	CONNECT THESE PINS TOGETHER		INPUT PIN	CONNECT THESE PINS TOGETHER		
0 to +5V	24	22 & 25	23 & 26	30	22 & 25	23 & 26	29 & 24
0 to +10V	24	—	23 & 26	30	—	23 & 26	29 & 24
±2.5V	24	22 & 25	23 & 22	30	22 & 25	23 & 22	29 & 24
±5V	24	—	23 & 22	30	—	23 & 22	29 & 24
±10V	25	—	23 & 22	30	—	23 & 22	29 & 25

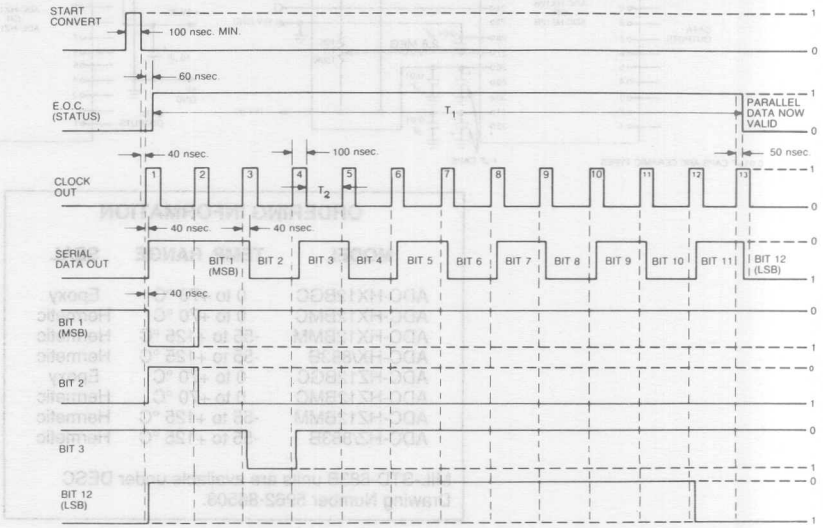
CALIBRATION PROCEDURE

1. Connect the converter for bipolar or unipolar operation. Use the input connection table for the desired input voltage range and input impedance. Apply Start Convert pulses of 100 nanoseconds minimum duration to pin 21. The spacing of the pulses should be no less than the maximum conversion time.
2. **Zero and Offset Adjustments**
   Apply a precision voltage reference source between the selected analog input and ground. Adjust the output of the reference source to the value shown in the Calibration Table for the unipolar zero adjustment (zero +½ LSB) or the bipolar offset adjustment (−FS+½ LSB). Adjust the trimming potentiometer so that the output code flickers equally between 1111 1111 1111 and 1111 1111 1110.
3. **Full Scale Adjustment**
   Change the output of the precision voltage reference source to the value shown in the Calibration Table for the unipolar or bipolar gain adjustment (+FS − 1½ LSB). Adjust the gain trimming potentiometer so that the output code flickers equally between 0000 0000 0001 and 0000 0000 0000.

TIMING DIAGRAM OPERATING PERIODS

	ADC-HX12B	ADC-HZ12B
T_1	20 μsec.	8.0 μsec.
T_2	1.56 μsec.	0.56 μsec.

TIMING DIAGRAM FOR ADC-HX12B, ADC-HZ12B OUTPUT: 101010101010



Calibration Table

UNIPOLAR RANGE	ADJUST.	INPUT VOLTAGE
0 to +5V	ZERO GAIN	+0.6 mV +4.9982V
0 to +10V	ZERO GAIN	+1.2 mV +9.9963V
BIPOLAR RANGE		
±2.5V	OFFSET GAIN	−2.4994V +2.4982V
±5V	OFFSET GAIN	−4.9988V +4.9963V
±10V	OFFSET GAIN	−9.9976V +9.9927V

Coding Table, Unipolar Operation

INPUT RANGE		COMP. BINARY CODING	
0 TO +10V	0 TO +5V	MSB	LSB
+9.9976V	+4.9988V	0000	0000 0000
+8.7500	+4.3750	0001	1111 1111
+7.5000	+3.7500	0011	1111 1111
+5.0000	+2.5000	0111	1111 1111
+2.5000	+1.2500	1011	1111 1111
+1.2500	+0.6250	1101	1111 1111
+0.0024	+0.0012	1111	1111 1110
0.0000	0.0000	1111	1111 1111

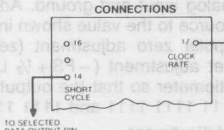
Coding Table, Bipolar Operation

INPUT VOLTAGE RANGE			COMP. OFFSET BINARY		COMP. TWO'S COMPLEMENT	
±10V	±5V	2.5V	MSB	LSB	MSB	LSB
+9.9951V	+4.9976V	+2.4988V	0000 0000	0000	1000 0000	0000
+7.5000	+3.7500	+1.8750	0001 1111	1111	1001 1111	1111
+5.0000	+2.5000	+1.2500	0011 1111	1111	1011 1111	1111
0.0000	0.0000	0.0000	0111 1111	1111	1111 1111	1111
−5.0000	−2.5000	−1.2500	1011 1111	1111	0011 1111	1111
−7.5000	−3.7500	−1.8750	1101 1111	1111	0101 1111	1111
−9.9951	−4.9976	−2.4988	1111 1111	1110	0111 1111	1110
−10.0000	−5.0000	−2.5000	1111 1111	1111	0111 1111	1111

SHORT CYCLE OPERATION

Refer to Technical Note 4 for methods of reducing the ADC-HX or ADC-HZ conversion times.

CONNECTIONS



CLOCK RATE VS. VOLTAGE

PIN 17 VOLTAGE	CLOCK RATE ADC-HX12B	CLOCK RATE ADC-HZ12B
0V	600 kHz	1.5MHz
+5V	720 kHz	1.8MHz
+15V	880 kHz	2.2MHz

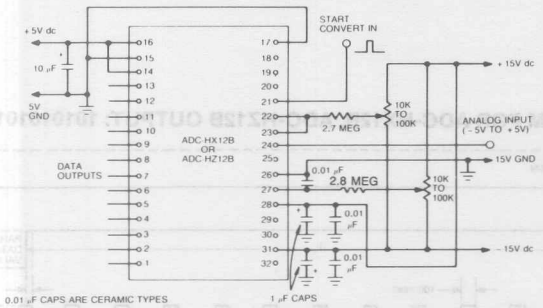
8, 10, & 12 BIT CONVERSION

RESOLUTION	12 BITS	10 BITS	8 BITS
ADC-HX12B CONV. TIME	20 µsec.	15 µsec.	10 µsec.
ADC-HZ12B CONV. TIME	8 µsec.	6 µsec.	4 µsec.
CONNECT THESE PINS TOGETHER	17 & 15	17 & 16	17 & 28
	14 & 16	14 & 2	14 & 4

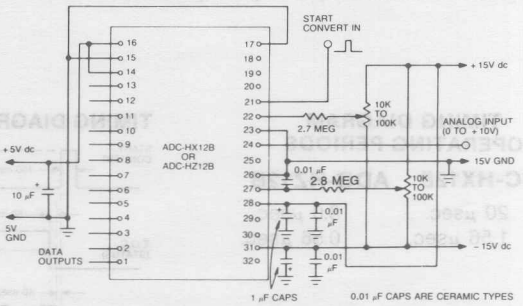
PIN 14 CONNECTION

RES. (BITS)	PIN 14 TO	RES. (BITS)	PIN 14 TO
1	PIN 11	7	PIN 5
2	PIN 10	8	PIN 4
3	PIN 9	9	PIN 3
4	PIN 8	10	PIN 2
5	PIN 7	11	PIN 1
6	PIN 6	12	PIN 16

BIPOLAR OPERATION, −5V TO +5V



UNIPOLAR OPERATION, 0 TO +10V



ORDERING INFORMATION

MODEL	TEMP. RANGE	SEAL
ADC-HX12BGC	0 to +70 °C	Epoxy
ADC-HX12BMC	0 to +70 °C	Hermetic
ADC-HX12BMM	-55 to +125 °C	Hermetic
ADC-HX/883B	-55 to +125 °C	Hermetic
ADC-HZ12BGC	0 to +70 °C	Epoxy
ADC-HZ12BMC	0 to +70 °C	Hermetic
ADC-HZ12BMM	-55 to +125 °C	Hermetic
ADC-HZ/883B	-55 to +125 °C	Hermetic

MIL-STD-883B units are available under DESC Drawing Number 5962-88508.

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D/A CONVERTERS

Model	Resolution (Bits)	Settling Time	Linearity Error	Power (Watts)	Case	Page
DAC-HF8	8	25 ns	±1/2 LSB	0.750	24-Pin DIP	3-1
DAC-HF10	10	25 ns	±1/2 LSB	0.900	24-Pin DIP	3-1
DAC-HF12	12	50 ns	±1/2 LSB	0.900	24-Pin DIP	3-1
DAC-HK12	12	3 µs	±1/2LSB	0.700	24-Pin DIP	3-5
DAC-HZ12	12	3 µs	±1/2 LSB	0.390	24-Pin DIP	3-13
DAC-HP16	16	15 µs	±0.003% FSR	0.600	24-Pin DIP	3-9

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DAC-HF Series
Ultra-Fast D/A Converters

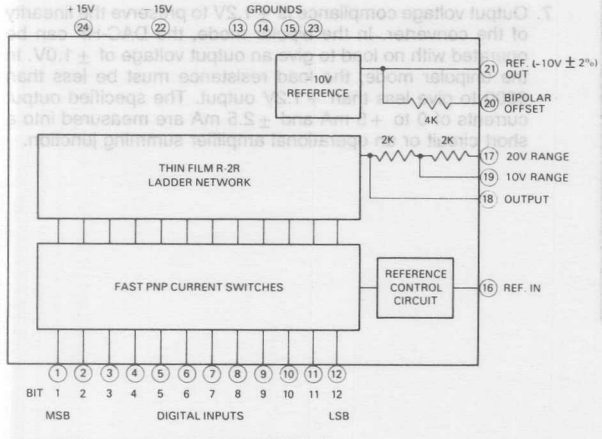
FEATURES

- 8-, 10-, 12-Bit resolution
- Settling times to 25 nanoseconds
- 20 ppm/°C tempco
- Unipolar or bipolar operation
- Current output
- Internal feedback resistor

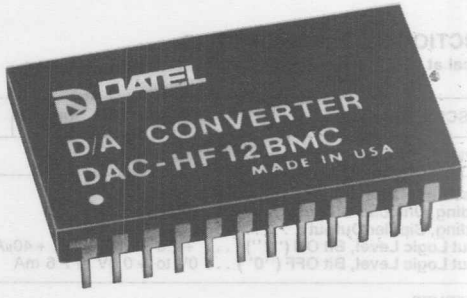
GENERAL DESCRIPTION

The DAC-HF Series of hybrid DAC's are ultra high-speed, current output devices. They incorporate state-of-the-art performance in a miniature package, achieving maximum output settling times of 25 nanoseconds for the 8- and 10-bit models and 50 nanoseconds for the 12-bit model. They can be used to drive a resistor load directly for up to ± 1V output or a fast operational amplifier (such as DATEL's AM-500) for higher voltage outputs with sub-microsecond settling times. A tapped feedback resistor and a bipolar offset resistor are included internally to give five programmable output voltage ranges with an external operational amplifier.

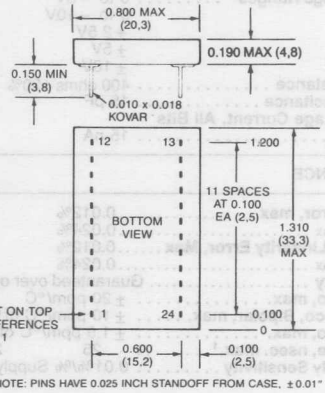
The DAC-HF design combines proven hybrid production techniques with advanced circuit design to realize high speed current switching. The design incorporates fast PNP current switches driving a low impedance R-2R thin-film ladder network. The nichrome thin-film resistor network is deposited by electron beam evaporation on a low capacitance substrate to assure high-speed performance. The resistors are then functionally trimmed by laser for optimum linearity.



NOTE: FOR DAC-HF10B PINS 11 & 12 ARE NO CONNECTION
FOR DAC-HF8B PINS 9, 10, 11 & 12 ARE NO CONNECTION



MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 IN (MSB)	13	GROUND
2	BIT 2 IN	14	GROUND
3	BIT 3 IN	15	GROUND
4	BIT 4 IN	16	REF. IN
5	BIT 5 IN	17	20 V RANGE
6	BIT 6 IN	18	OUTPUT
7	BIT 7 IN	19	10 V RANGE
8	BIT 8 IN	20	BIPOLAR OFFSET
9	BIT 9 IN	21	REF. OUT
10	BIT 10 IN	22	−15 VDC
11	BIT 11 IN	23	GROUND
12	BIT 12 IN (LSB)	24	+15 VDC

ABSOLUTE MAXIMUM RATINGS, ALL MODELS	
Positive Supply, Pin 24	+18V
Negative Supply, Pin 22	−18V
Digital Input Voltage, Pins 1 to 12	+15V

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V supplies unless otherwise specified.

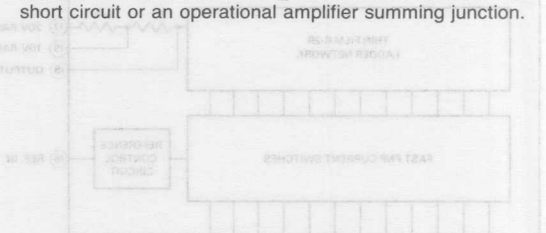
DESCRIPTION	8B	10B	12B
INPUTS			
Resolution, Bits	8	10	12
Coding, Unipolar Output	Straight Binary		
Coding, Bipolar Output	Offset Binary		
Input Logic Level, Bit ON ("1")	+2.0 to +5.5V at +40μA		
Input Logic Level, Bit OFF ("0")	0V to +0.8V at 2.6 mA		
OUTPUTS			
Output Current Range, Unipolar	0 to +5 mA		
Output Current Range, Bipolar	±2.5 mA		
Output Voltage Compliance	±1.2V		
Output Voltage Ranges[2]	0 to −5V 0 to −10V ±2.5V ±5V ±10V		
Output Resistance	400 ohms ±20%		
Output Capacitance	15 pF		
Output Leakage Current, All Bits OFF	15 nA		
PERFORMANCE			
Linearity Error, max	0.012%		
TMIN to TMAX	0.024%		
Differential Linearity Error, Max	0.012%		
TMIN to TMAX	0.024%		
Monotonicity	Guaranteed over oper. temp. range		
Gain Tempco, max.	±20 ppm/°C		
Offset Tempco, Bipolar, max.	±10 ppm/°C of F.S.R.[3]		
Zero Tempco, max.	±1.5 ppm/°C of F.S.R.[3]		
Settling Time, nsec. max.[1]	25	25	50
Power Supply Sensitivity	0.01%/% Supply		
POWER REQUIREMENTS			
Supply Voltage	±15V dc ±0.5V		
Positive Quiescent Current, max.	35mA	40mA	45mA
Negative Quiescent Current, max.	15mA	15mA	15mA
PHYSICAL/ENVIRONMENTAL			
Operating Temperature Range	0°C to +70°C (BMC)		
Storage Temperature Range	-55 °C to +125 °C (BMM, 883B)		
Package Type	24-Pin Ceramic DIP		
Pins	0.010 × 0.018 inch Kovar		
Weight	0.2 oz (6g.)		

FOOTNOTES:

1. Full scale current change to 1 LSB with 400Ω load.
2. With External Operational Amplifier.
3. F.S.R. is Full Scale Range, or the difference between minimum and maximum output values.

TECHNICAL NOTES

1. Proper operation of the DAC-HF series converters is dependent on good board layout and connection practices. Bypass supplies as shown in the connection diagrams. Mount bypass capacitors close to the converter, directly to the supply pins where possible.
2. Use of a ground plane is particularly important in high speed D to A converters as it reduces high frequency noise and aids in decoupling the digital inputs from the analog output. Avoid ground loop problems by connecting all grounds on the board to the ground plane. The remainder of the ground plane should include as much of the circuit board as possible.
3. When the converter is configured for voltage output with an external operational amplifier, keep the leads from the converter to the ouptut amplifier as short as possible.
4. The high speed current switching technique used in the DAC-HF series inherently reduces the amplitude and duration of large transient spikes at the output ("glitches"). The most severe glitches occur at half-scale, the major carry transition from 011 ... 1 to 100 ... 0 or vice versa. At this time, a skewing of the input codes can create a transition state code of 111 ... 1. The duration of the "transition state code" is dependent on the degree of skewing but its effect is dependent on the speed of the DAC (an ultra-fast DAC will respond to these brief spurious inputs to a greater degree than a slow DAC). Minimize the effects of input skewing by using a high-speed input register to match input switching times. The input register recommended for use with the DAC-HF is easily implemented with two Texas Instruments SN74S174 hex D-type flip-flops. This register will reduce glitches to a very low level and ensure fast output settling times.
5. Test the DAC-HF using a low capacitance test probe (such as a 10X probe). Take care to assure the shortest possible connection between probe ground and circuit ground. Long probe ground leads may pick up environmental E.M.I. causing artifacts on the scope display, i.e., signals that do not originate at the unit under test.
6. Passive components used with the DAC-HF may be as indicated here: 0.1 μF and 1 μF bypass capacitors should be ceramic type and tantalum type respectively; the 400Ω output load is a 0.1% 10 ppm/°C metal film type; adjustment potentiometers are ceremet types: other resistors may be ±10% carbon composition types.
7. Output voltage compliance is ±1.2V to preserve the linearity of the converter. In the bipolar mode, the DAC-HF can be operated with no load to give an output voltage of ±1.0V. In the unipolar mode, the load resistance must be less than 600Ω to give less than +1.2V output. The specified output currents of 0 to +5 mA and ±2.5 mA are measured into a short circuit or an operational amplifier summing junction.



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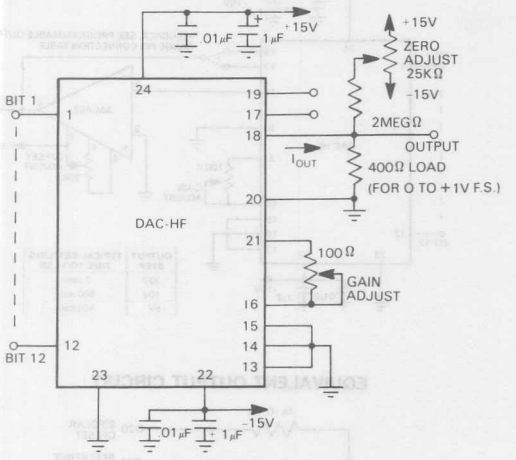
CONNECTION AND CALIBRATION

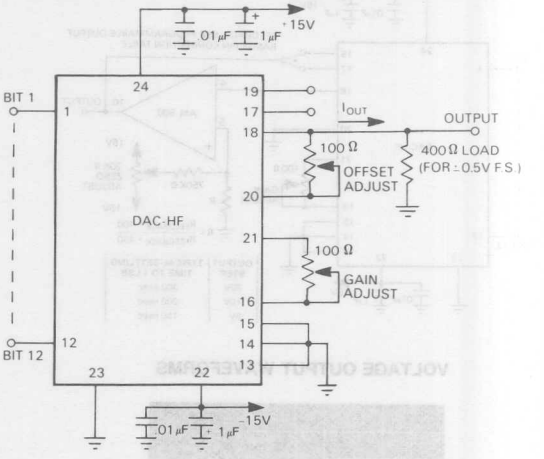
UNIPOLAR CURRENT OUTPUT CONNECTIONS



UNIPOLAR CURRENT OUTPUT CALIBRATION PROCEDURE

1. Connect the converter as shown in the connection diagram.
2. Set all inputs low and adjust the ZERO ADJUST potentiometer for a reading of 0V at the output.
3. Set all inputs high and adjust the GAIN ADJUST potentiometer for a reading of −F.S. +1 LSB (given in the coding table for 12-bit units).

BIPOLAR CURRENT OUTPUT CONNECTIONS



BIPOLAR CURRENT OUTPUT CALIBRATION PROCEDURE

1. Connect the converter as shown in the connection diagram.
2. Set all inputs low and adjust the OFFSET ADJUST potentiometer for an output reading of +F.S., (given in the coding table for 12-bit units).
3. Set all inputs high and adjust the GAIN ADJUST potentiometer for an output reading of −F.S. +1 LSB, (given in the coding table for 12-bit units).

CODING TABLES
UNIPOLAR OUTPUT

UNIPOLAR SCALE	INPUT CODING STRAIGHT BINARY	ANALOG OUTPUT 0 to +1V F.S	0 to −5V F.S	0 to −10V F.S
−F.S. +1 LSB	1111 1111 1111	+0.9998V	−4.9988V	−9.9976V
−¾ F.S.	1100 0000 0000	+0.7500V	−3.7500V	−7.5000V
−½ F.S.	1000 0000 0000	+0.5000V	−2.5000V	−5.0000V
−¼ F.S.	0100 0000 0000	+0.2500V	−1.2500V	−2.5000V
−1 LSB	0000 0000 0001	+0.0002V	−0.0012V	−0.0024V
0	0000 0000 0000	+0.0000V	+0.0000V	0.0000V

BIPOLAR OUTPUT

BIPOLAR SCALE	INPUT CODING OFFSET BINARY	ANALOG OUTPUT ±0.5V F.S.	±2.5V F.S.	±5V F.S.	±10V F.S.
−F.S. +1LSB	1111 1111 1111	+0.4998V	−2.4988V	−4.9976V	−9.9951V
−½ F.S.	1100 0000 0000	+0.1250V	−1.2500V	−2.5000V	−5.0000V
−1 LSB	1000 0000 0001	+0.0002V	−0.0012V	−0.0024V	−0.0049V
0	1000 0000 0000	0.0000V	0.0000V	0.0000V	0.0000V
+½ F.S.	0100 0000 0000	−0.1250V	+1.2500V	+2.500V	+5.0000V
+F.S. −1LSB	0000 0000 0001	−0.4998V	+2.4988V	+4.9976V	+9.9951V
+F.S.	0000 0000 0000	−0.5000V	+2.5000V	+5.0000V	+10.0000V

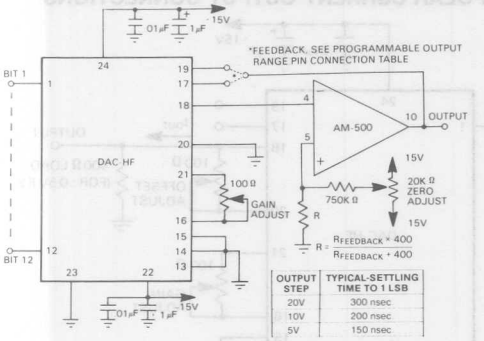
PROGRAMMABLE OUTPUT RANGE PIN CONNECTIONS

OUTPUT VOLTAGE RANGE	FEEDBACK CONNECTION	CONNECT THESE PINS TOGETHER
0 to −5V	PIN 19	PIN 17 to PIN 18 PIN 20 to PIN 23
0 to −10V	PIN 19	PIN 20 to PIN 23
±2.5V	PIN 19	PIN 17 to PIN 18 PIN 20 to PIN 18
±5V	PIN 19	PIN 20 to PIN 18
±10V	PIN 17	PIN 20 to PIN 18

In all programmable output ranges pin 18 connects to external operational amplifier inverting input

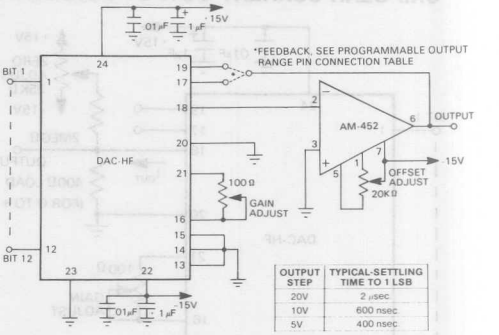
APPLICATIONS

UNIPOLAR ULTRA-FAST VOLTAGE OUTPUT



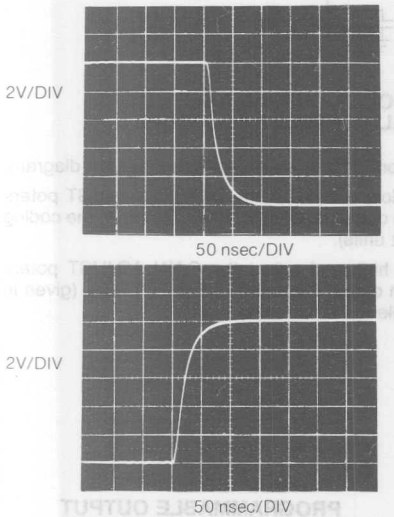
OUTPUT STEP	TYPICAL-SETTLING TIME TO 1 LSB
20V	300 nsec
10V	200 nsec
5V	150 nsec

UNIPOLAR FAST VOLTAGE OUTPUT CIRCUIT



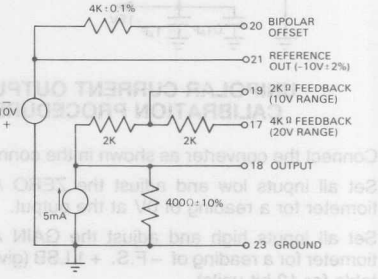
OUTPUT STEP	TYPICAL-SETTLING TIME TO 1 LSB
20V	2 μsec
10V	600 nsec
5V	400 nsec

VOLTAGE OUTPUT WAVEFORMS

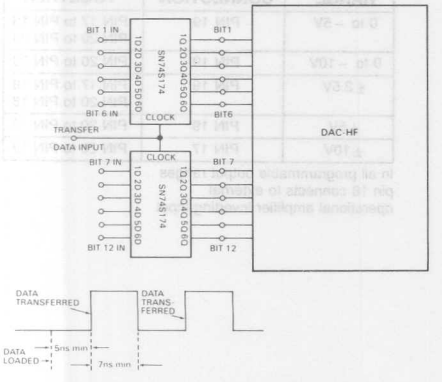


DAC-HF with AM-500, ±5V output full scale (10V) step

EQUIVALENT OUTPUT CIRCUIT



HIGH SPEED INPUT REGISTER



ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	SEAL
DAC-HF8BMC	0 to +70 °C	Hermetic
DAC-HF8BMM	-55 to +125 °C	Hermetic
DAC-HF8/883B	-55 to +125 °C	Hermetic
DAC-HF10BMC	0 to +70 °C	Hermetic
DAC-HF10BMM	-55 to +125 °C	Hermetic
DAC-HF10/883B	-55 to +125 °C	Hermetic
DAC-HF12BMC	0 to +70 °C	Hermetic
DAC-HF12BMM	-55 to +125 °C	Hermetic
DAC-HF12/883B	-55 to +125 °C	Hermetic

DAC-HK Series
12-Bit Hybrid DAC's with Input Register

FEATURES

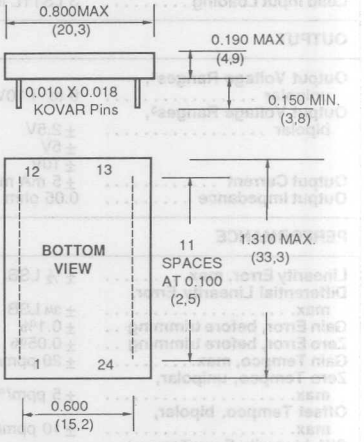
- **12-Bit resolution**
- **20 ppm/°C Tempco**
- **Input register**
- **2 Coding options**
- **Fast settling time**

GENERAL DESCRIPTION

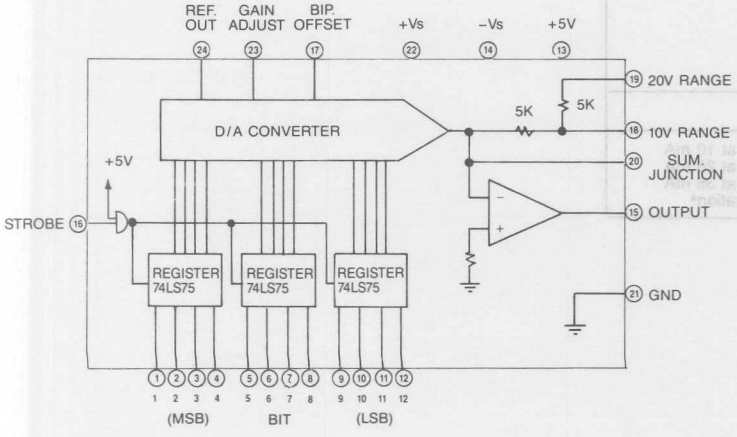
The DAC-HK Series hybrid D/A converters are high performance 12-bit devices with a fast settling voltage output. They incorporate a level controlled input storage register and are specifically designed for systems applications such as data bus interfacing with computers. When the "load" input is high, data in the storage register is held and when the load input is low, date is transferred through to the DAC. There are two basic models available by coding option: binary, and two's complement. The output voltage ranges are externally pin-programmable and include: 0 to +2.5V, 0 to +5V, 0 to +10V, ±2.5V, ±5V, and ±10V.

The DAC-HK Series contains a precision zener reference circuit. This eliminates code-dependent ground currents by routing current from the positive supply to the internal ground node a determined by the R-2R ladder network. The internal feedback resistors for the on-board amplifier track the ladder network resistors, enhancing temperature performance. The excellent tracking of the resistors results in a differential nonlinearity tempco of 2 ppm/°C maximum. The temperature coefficient of gain is 20 ppm/°C maximum and tempco of zero is ±3 ppm/°C maximum.

MECHANICAL DIMENSIONS
INCHES (mm)



NOTE: Pins have a 0.025 inch, ±0.01 stand-off from case.



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 IN (MSB)	13	+5 VDC
2	BIT 2 IN	14	–15 VDC
3	BIT 3 IN	15	OUTPUT
4	BIT 4 IN	16	LOAD
5	BIT 5 IN	17	BIPOLAR OFF
6	BIT 6 IN	18	10 V RANGE
7	BIT 7 IN	19	20 V RANGE
8	BIT 8 IN	20	SUM JUNCTION
9	BIT 9 IN	21	GROUND
10	BIT 10 IN	22	+15 VDC
11	BIT 11 IN	23	GAIN ADJ
12	BIT 12 IN (LSB)	24	REF OUT

ABSOLUTE MAXIMUM RATINGS	DAC-HK12B
Positive Supply, pin 22	+18V
Negative Supply, pin 14	−18V
Logic Supply, pin 13	+5.25V
Digital Input Voltage, pins 1-12 & 16	+5.5V
Output Current, pin 15	±20 mA

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V and +5V supplies unless otherwise noted.

INPUTS	
Resolution	12 bits
Coding, unipolar output	Straight Binary
Coding, bipolar output	Offset Binary Two's Complement[1]
Input Logic Level, bit ON ("1")	+2.0V to +5.5V
Input Logic Level, bit OFF ("0")	0V to +0.8V
Logic Loading	1 LSTTL load
Load Input[2]	High ("1") = hold data Low ("0") = transfer data
Load Input Loading	3 LSTTL loads

OUTPUT	
Output Voltage Ranges[3], unipolar	0 to +10V
Output Voltage Ranges[3], bipolar	±2.5V ±5V ±10V
Output Current	±5 mA min.
Output Impedance	0.05 ohm

PERFORMANCE	
Linearity Error, max.	±½ LSB
Differential Linearity Error, max.	±¾ LSB
Gain Error, before trimming	±0.1%
Zero Error, before trimming	±0.05%
Gain Tempco, max.	±20 ppm/°C
Zero Tempco, unipolar, max.	±5 ppm/°C of FSR
Offset Tempco, bipolar, max.	±10 ppm/°C of FSR
Diff. Linearity Error Tempco, max.	±2 ppm/°C of FSR
Monotonicity	Guaranteed over oper. temp. range
Settling Time, 5V change	3 µsec.
Settling Time, 10V change	3 µsec.
Settling Time, 20V change	4 µsec.
Settling Time, 1 LSB change	800 nsec.
Slew Rate	20V/µsec.
Power Supply Rejection	±0.002% FSR/%

POWER REQUIREMENTS	
Power Supply Voltage	+15V dc ±0.5V dc at 10 mA −15V dc ±0.5V dc at 25 mA +5V dc ±0.25V dc at 35 mA ±12V dc, +5V operation[4]

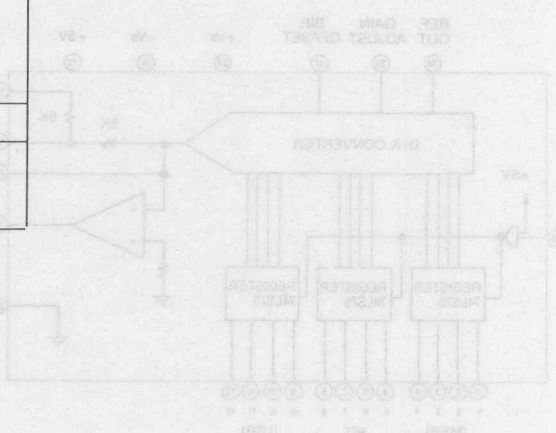
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0°C to +70°C (BGC, BMC) -55 °C to +125 °C (BMM/883B)
Storage Temperature Range	−65°C to +125°C
Package Type	24-pin Ceramic DIP
Pins	0.010 x 0.018 inch Kovar
Weight	0.2 ounces (6 grams)

FOOTNOTES:

1. For two's complement coding order the model described under ordering information.
2. Logic levels are the same as for data inputs.
3. By external pin connection.
4. For ±12V dc, +5V dc operation, contact factory.

TECHNICAL NOTES

1. It is recommended that these converters be operated with local supply bypass capacitors of 1 µF (tantalum type) at the +15, −15, and +5V supply pins. The capacitors should be connected as close to the pins as possible. In high RFI noise environments these capacitors should be shunted with 0.01 µF ceramic capacitors.
2. The analog, digital, and power grounds should be separated from each other as close as possible to pin 21 where they all must come together.
3. The "load" control pin is a level triggered input which causes the register to hold data with a high input and transfer data to the DAC with a low input.
4. A setup time of 50 nanoseconds minimum must be allowed for the input data. The DAC output voltage begins to change when the register output changes.
5. The external gain adjustment shown in the Connection Diagrams has a range of ±0.2% of full scale. If a wider range is desired the 18-Megohm resistor can be decreased slightly in value. The full-scale output is typically accurate within ±0.1% with no adjustment. The zero, or offset, adjustment has a range of ±0.35% of FS.
6. If the reference output terminal (pin 24) is used, an operational amplifier in non-inverting mode should be used as a buffer. Current drawn from pin 24 should be limited to ±10 µA in order not to affect the T.C. of the reference.



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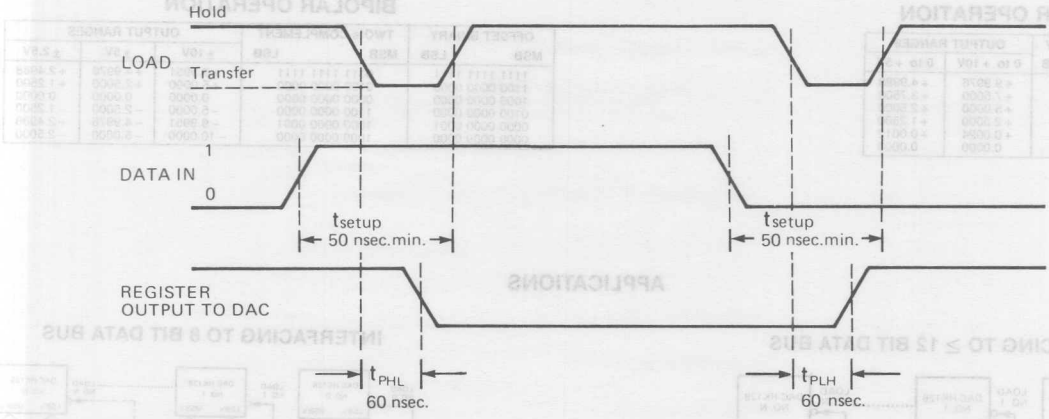
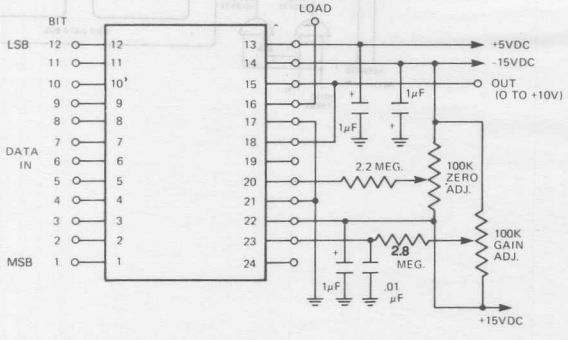
TIMING DIAGRAM



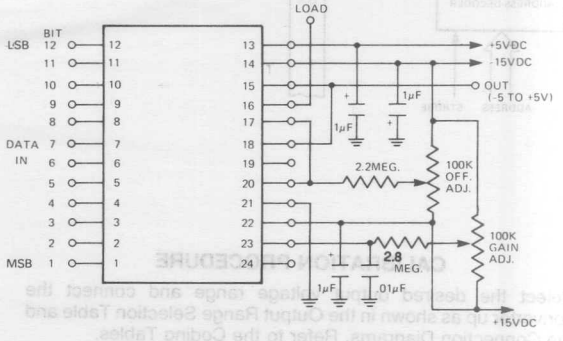
All rise and fall times ≤10 nsec.

CONNECTION DIAGRAMS

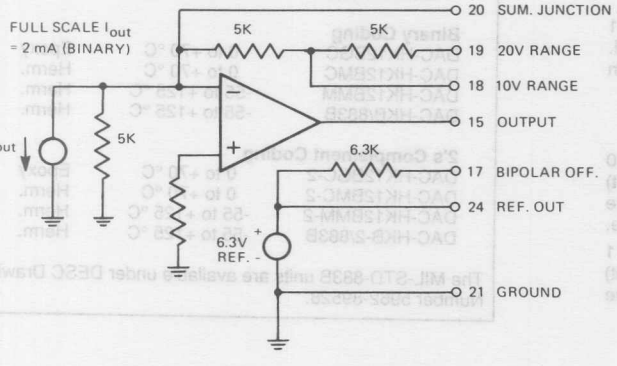
UNIPOLAR OPERATION (0 to +10V)



BIPOLAR OPERATION (±5 V)



OUTPUT CIRCUIT



OUTPUT RANGE SELECTION

RANGE	CONNECT THESE PINS TOGETHER		
±10 V	15 & 19	17 & 20	
±5 V	15 & 18	17 & 20	
±2.5 V	15 & 18	17 & 20	19 & 20
+10 V	15 & 18	17 & 21	
+5 V	15 & 18	17 & 21	19 & 20

CODING TABLES

UNIPOLAR OPERATION

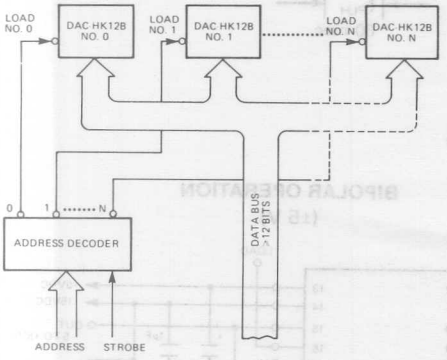
STRAIGHT BINARY MSB LSB	OUTPUT RANGES 0 to +10V	0 to +5V
1111 1111 1111	+9.9976	+4.9988
1100 0000 0000	+7.5000	+3.7500
1000 0000 0000	+5.0000	+2.5000
0100 0000 0000	+2.5000	+1.2500
0000 0000 0001	+0.0024	+0.0012
0000 0000 0000	0.0000	0.0000

BIPOLAR OPERATION

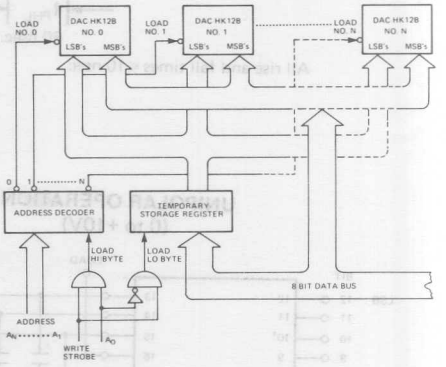
OFFSET BINARY MSB LSB	TWO's COMPLEMENT MSB LSB	OUTPUT RANGES ±10V	±5V	±2.5V
1111 1111 1111	0111 1111 1111	+9.9951	+4.9976	+2.4988
1100 0000 0000	0100 0000 0000	+5.0000	+2.5000	+1.2500
1000 0000 0000	0000 0000 0000	0.0000	0.0000	0.0000
0100 0000 0000	1100 0000 0000	−5.0000	−2.5000	−1.2500
0000 0000 0001	1000 0000 0001	−9.9951	−4.9976	−2.4988
0000 0000 0000	1000 0000 0000	−10.0000	−5.0000	−2.5000

APPLICATIONS

INTERFACING TO ≥ 12 BIT DATA BUS



INTERFACING TO 8 BIT DATA BUS



CALIBRATION PROCEDURE

Select the desired output voltage range and connect the converter up as shown in the Output Range Selection Table and the Connection Diagrams. Refer to the Coding Tables.

UNIPOLAR OPERATION

1. **Zero Adjustment.** Set the input digital code to 0000 0000 0000 and adjust the ZERO ADJ. potentiometer to give 0.0000V output.
2. **Gain Adjustment.** Set the input digital code to 1111 1111 1111 (straight binary) and adjust the GAIN ADJ. potentiometer to give the full-scale output voltage shown in the Coding Table.

BIPOLAR OPERATION

1. **Offset Adjustment.** Set the digital input code to 0000 0000 0000 (offset binary) or 1000 0000 0000 (two's complement) and adjust the OFFSET ADJ. potentiometer to give the negative full-scale output voltage shown in the Coding Table.
2. **Gain Adjustment.** Set the digital input code to 1111 1111 1111 (offset binary) or a 0111 1111 1111 (two's complement) and adjust the GAIN ADJ. potentiometer to give the positive full-scale output voltage shown in the Coding Table.

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE	SEAL
Binary Coding		
DAC-HK12BGC	0 to +70 °C	Epoxy
DAC-HK12BMC	0 to +70 °C	Herm.
DAC-HK12BMM	-55 to +125 °C	Herm.
DAC-HKB/883B	-55 to +125 °C	Herm.
2's Complement Coding		
DAC-HK12BGC-2	0 to +70 °C	Epoxy
DAC-HK12BMC-2	0 to +70 °C	Herm.
DAC-HK12BMM-2	-55 to +125 °C	Herm.
DAC-HKB-2/883B	-55 to +125 °C	Herm.

The MIL-STD-883B units are available under DESC Drawing Number 5962-89528.

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DAC-HP16B

16-Bit, Micro-electronic Digital-to-Analog Converter

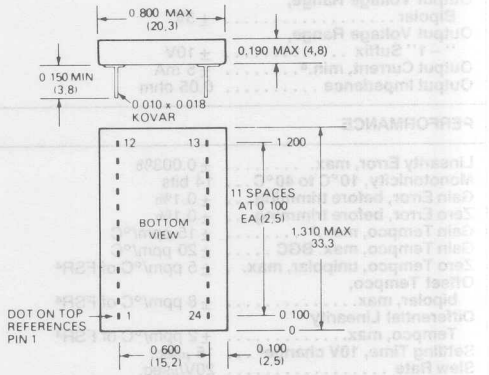
FEATURES

- **16-Bit binary model**
- **Voltage outputs**
- **15 ppm/°C Maximum gain tempco**
- **Linearity to ± 0.003%**

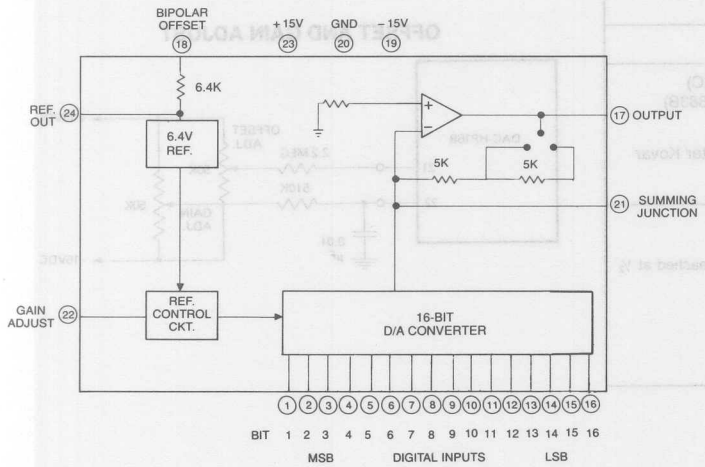
GENERAL DESCRIPTION

The DAC-HP series are high resolution hybrid D/A converters with voltage output. They are self-contained, including a low tempco zener reference circuit and output operational amplifier, all in a miniature 24-pin double spaced ceramic DIP package. The DAC-HP16B has 16-bit binary resolution with ±0.003% linearity. Input coding is complementary binary and complementary offset binary for the DAC-HP16B. This device operates in both unipolar and bipolar modes with output voltages of 0 to +10V dc and ±5V dc respectively. Binary versions with a bipolar output voltage range of ±10V dc are available, denoted by the suffix "-1" after the model designation.

MECHANICAL DIMENSIONS
INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 IN (MSB)	13	BIT 13 IN
2	BIT 2 IN	14	BIT 14 IN
3	BIT 3 IN	15	BIT 15 IN
4	BIT 4 IN	16	BIT 16 IN (LSB)
5	BIT 5 IN	17	OUTPUT
6	BIT 6 IN	18	BIPOLAR OFF
7	BIT 7 IN	19	−15VDC
8	BIT 8 IN	20	GROUND
9	BIT 9 IN	21	SUM JUNCTION
10	BIT 10 IN	22	GAIN ADJ
11	BIT 11 IN	23	+15VDC
12	BIT 12 IN	24	REF OUT

ABSOLUTE MAXIMUM RATINGS	
Positive Supply, pin 23	+18V
Negative Supply, pin 19	−18V
Digital Input Voltage, pins 1-16	+5.5V
Output Current, pin 17	±20 mA

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, and ±15V supplies unless otherwise noted.

INPUTS	
Resolution	16 bits
Coding, unipolar output	Comp. Binary
Coding, bipolar output	Comp. Off. Binary
Input Logic Level, bit ON ("0")[1]	0V to +0.8V at −1 mA
Input Logic Level, bit OFF ("1")[1]	+2.4V to +5.5V at +40 μA
Logic Loading	1 TTL load

OUTPUTS	
Output Voltage Range, Unipolar[2]	0 to +10V
Output Voltage Range, Bipolar	±5V
Output Voltage Range, "−1" Suffix	±10V
Output Current, min.[6]	±5 mA
Output Impedance	0.05 ohm

PERFORMANCE	
Linearity Error, max.	±0.003%
Monotonicity, 10°C to 40°C	14 bits
Gain Error, before trimming	±0.1%
Zero Error, before trimming	±0.1%
Gain Tempco, max.[3]	±15 ppm/°C
Gain Tempco, max. BGC	±20 ppm/°C
Zero Tempco, unipolar, max.	±5 ppm/°C of FSR[4]
Offset Tempco, bipolar, max.	±8 ppm/°C of FSR[4]
Differential Linearity Tempco, max.	±2 ppm/°C of FSR[4]
Settling Time, 10V change[5]	15 μsec.
Slew Rate	20V/μsec.
Power Supply Rejection	±0.002% FSR/%

POWER REQUIREMENTS	
(Quiescent, all bits high)	+15V dc, ±0.5V dc at 20 mA −15V dc, ±0.5V dc at 25 mA ±12V dc operation[7]

PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0°C to +70°C (BMC, BGC) -55 °C to +125 °C (BMM, 883B)
Storage Temperature Range	−65°C to +150°C
Package Type	24 pin ceramic
Pins	0.010 x 0.018 inch diameter Kovar
Weight	0.2 ounces (6 grams)

FOOTNOTES:

1. Drive from TTL output with only the DAC-HP as load.
2. Unipolar output range for suffix "−1" models, 0 to +10V, is reached at ½ scale input.
3. For all models except DAC-HP16BGC.
4. FSR is 0 to +FS or −FS to +FS voltage.
5. To 0.005% FSR.
6. Pin 17.
7. For ±12V dc operation, consult factory.

TECHNICAL NOTES

1. It is recommended that these converters be operated with local supply bypass capacitors of 1 μF (tantalum type) at the +15V and −15V supply pins. The capacitors should be connected as close to the pins as possible. In high frequency noise environments an additional 0.01 μF ceramic capacitor should be used in parallel with each tantalum bypass.
2. When laying out the circuit board for this device, isolate the analog, digital, and power grounds as much as possible from each other before joining them at pin 20.
3. The external gain adjustment shown in the diagrams gives an adjustment of ±0.2% of full-scale range. The converters are internally trimmed to ±0.1% at full scale. A wider range of adjustment may be achieved by decreasing the value of the the 510 Kohm resistor.
4. The zero adjustment, or offset adjustment, has an adjustment range of ±0.35% of full-scale range. The unipolar zero is internally set to zero within ±0.1% of full-scale range.
5. If the reference output (pin 24) is used, it must be buffered by an operational amplifier in the noninverting mode. Current drawn from pin 24 should be limited to ±10 μA in order that the temperature coefficient of the reference circuit not be affected. This is sufficient current for the bias current of most of the popular operational amplifier types.

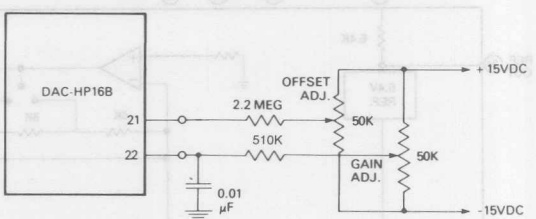
CALIBRATION PROCEDURE

For bipolar operation connect Bipolar Offset (pin 18) to Summing Junction (pin 21). For unipolar operation connect Bipolar Offset (pin 18) to Ground (pin 20). In making the following adjustments, refer to the coding tables.

1. **Zero Adjusment.** Set the input digital code to 1111 1111 1111 1111 and adjust the ZERO ADJ. potentiometer to give 0.00000V output unipolar or -FS bipolar operation.

2. **Gain Adjustment.** Set the input digital code to 0000 0000 0000 0000 (complementary binary) and adjust the GAIN ADJ. potentiometer to give +9.99985V output unipolar or +FS - 1 LSB output bipolar operation.

OFFSET AND GAIN ADJUST



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CONNECTION AND CALIBRATION

CODING TABLES
BIPOLAR OUTPUT — Complementary Offset Binary

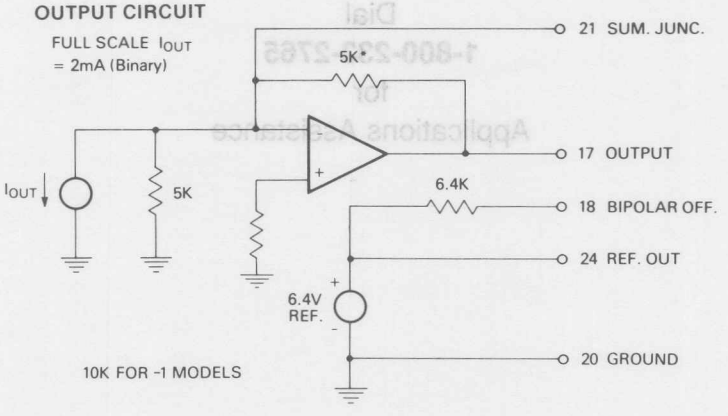
INPUT CODE MSB LSB	SCALE	OUTPUT VOLTAGE	OUTPUT VOLTAGE SUFFIX "–1" MODELS
0000 0000 0000 0000	+FS – 1 LSB	+4.99985V	+9.99969V
0011 1111 1111 1111	+½FS	+2.50000	+5.00000
0111 1111 1111 1111	0	0.00000	0.00000
1011 1111 1111 1111	–½FS	–2.50000	–5.00000
1111 1111 1111 1110	–FS + 1 LSB	–4.99985	–9.99969
1111 1111 1111 1111	–FS	–5.00000V	–10.00000V

UNIPOLAR OUTPUT — Complementary Binary

INPUT CODE MSB LSB	SCALE	OUTPUT VOLTAGE
0000 0000 0000 0000	+FS – 1 LSB	+9.99985V
0011 1111 1111 1111	+¾ FS	+7.50000
0111 1111 1111 1111	+½ FS	+5.00000
1011 1111 1111 1111	+¼ FS	+2.50000
1111 1111 1111 1110	+1 LSB	+153 μV
1111 1111 1111 1111	0	0

APPLICATION

OUTPUT CIRCUIT



ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE	SEAL
DAC-HP16BMC	0 to +70 °C	Herm.
DAC-HP16BMM	-55 to +125 °C	Herm.
DAC-HPB/883B	-55 to +125 °C	Herm.
DAC-HP16BMC-1	0 to +70 °C	Herm.
DAC-HP16BMM-1	-55 to +125 °C	Herm.
DAC-HPB-1/883B	-55 to +125 °C	Herm.
DAC-HP16BGC-1	0 to +70 °C	Epoxy
DAC-HP16BGC	0 to +70 °C	Epoxy

The MIL-STD-883B units are available under DESC Drawing Number 5962-89531.

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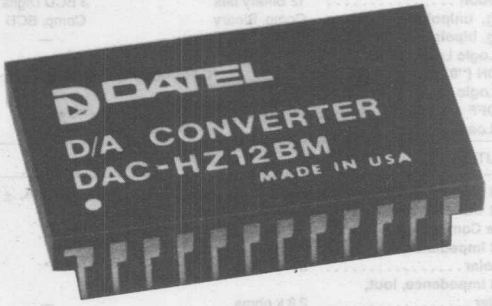
FEATURES

- **12-Bit binary**
- **5 Output ranges**
- **3 Microseconds settling time**
- **Internal reference and output amplifier**
- **High performance**

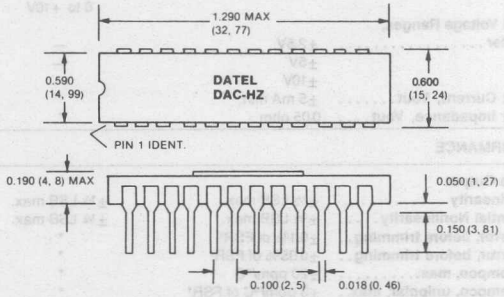
GENERAL DESCRIPTION

The DAC-HZ Series are high performance, hybrid 12-bit binary digital-to-analog converters. These converters are manufactured using thin- and thick-film technology. They are complete and self-contained with a precision internal reference and fast output operational amplifier. Pin-programmable output voltage ranges are provided for a high degree of application flexibility; the output voltage ranges are 0 to ±5V dc, 0 to +10V dc, ±2.5V dc, —5V dc, and ±10V dc. Current output is also provided.

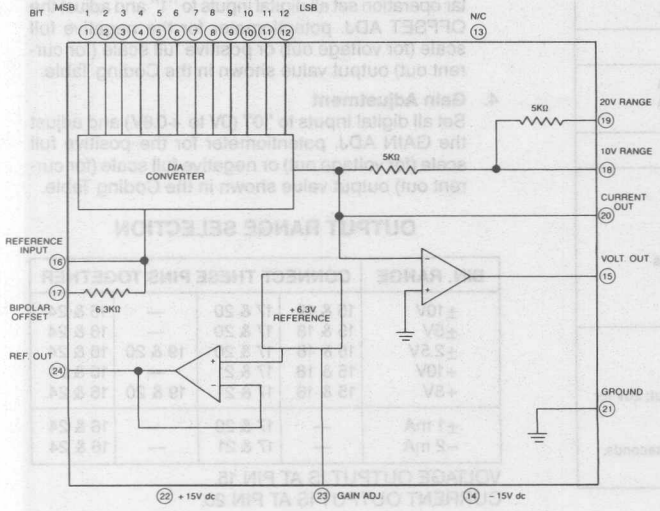
The DAC-HZ Series contains a precision zener reference circuit. This eliminates code-dependent ground currents by routing current from the positive supply to the internal ground node as determined by the R-2R ladder network. The internal feedback resistors for the on-board amplifier track the ladder network resisters, enhancing temperature performance. The excellent tracking of the resistors results in a differential nonlinearity tempco of 2 ppm/°C maximum. The temperature coefficient of gain is 20 ppm/°C maximum and tempco of zero is ±3 ppm/°C maximum.



MECHANICAL DIMENSIONS
INCHES (MM)



ALL DIMENSIONS ARE IN INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 IN	13	NO CONNECTION
2	BIT 2 IN	14	-15V dc
3	BIT 3 IN	15	VOLT. OUT
4	BIT 4 IN	16	REFERENCE IN
5	BIT 5 IN	17	BIPOLAR OFFSET
6	BIT 6 IN	18	10V RANGE
7	BIT 7 IN	19	20V RANGE
8	BIT 8 IN	20	CURRENT OUT
9	BIT 9 IN	21	GROUND
10	BIT 10 IN	22	+15V dc
11	BIT 11 IN	23	GAIN ADJUST
12	BIT 12 IN	24	REFERENCE OUT

FUNCTIONAL SPECIFICATIONS

Typical at 25°C and ±15V supplies unless otherwise noted.

INPUTS	DAC-HZ12B (Binary)	DAC-HZ12D (BCD)
Resolution	12 Binary bits	3 BCD Digits
Coding, unipolar output	Comp. Binary	Comp. BCD
Coding, bipolar output	Comp. Off. Binary	—
Input Logic Level, bit ON ("0")	0V to +0.8V at −1 mA	
Input Logic Level, bit OFF ("1")	+2.4V to +5.5V at +40 μA	
Logic Loading	1 TTL load	
OUTPUTS		
Output Current, unipolar	0 to −2 mA, ±20%	0 to −1.25 mA, ±10%
Output Current, bipolar	±1 mA, ±20%	—
Voltage Compliance, Iout	±2.5V	*
Output Impedance, Iout, unipolar	5 k ohms	*
Output Impedance, Iout, bipolar	2.8 k ohms	—
Output Voltage Ranges, unipolar	0V to + 5V 0V to + 10V	0 to + 2.5V 0 to +5V 0 to +10V
Output Voltage Ranges, bipolar	±2.5V ±5V ±10V	— — —
Output Current, Vout	±5 mA min.	*
Output Impedance, Vout	0.05 ohm	*
PERFORMANCE		
Voltage Output Nonlinearity	±½ LSB max.	±¼ LSB max.
Differential Nonlinearity	±¾ LSB max.	±¼ LSB max.
Gain Error, before trimming	±0.1% of FSR[1]	*
Zero Error, before trimming	±0.05% of FSR[1]	*
Gain Tempco, max.	±20 ppm/°C	*
Zero Tempco, unipolar, max.	±3 ppm/°C of FSR[1]	*
Offset Tempco, bipolar, max.	±10 ppm/°C of FSR[1]	*
Diff. Nonlinearity Tempco, max.	±2 ppm/°C of FSR[1]	*
Monotonicity	Over oper. temp. range	*
Setting Time, Iout to ½ LSB[2]	300 nsec.	*
Settling Time, Vout to ½ LSB	3 μsec.[3]	*
Slew Rate	20V/μsec.	*
Power Supply Rejection	±0.002% FSR/% Supply[1]	*
POWER REQUIREMENTS		
Power Supply Voltage	+15V dc, ±0.5V dc at 10 mA −15V dc, ±0.5V dc at 16 mA ±12V dc operation[4]	
PHYSICAL/ENVIRONMENTAL		
Operating Temperature Ranges	0°C to +70°C and -55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	
Package Size	1.300 × 0.800 × 0.160 inches	
Package Type	24 Pin Ceramic DIP	
Pins	Kovar 0.010 × 0.018 inches	
Weight	0.22 ounces (63 grams)	

*Specifications same as first column

FOOTNOTES:

1. FSR is full scale range and is 10V for 0 to +10V or −5V to +5V output; 20V for ±10V output, etc.
2. Current output mode.
3. For 2.5k or 5k feedback. For 10k feedback the settling time is 4 microseconds.
4. For ±12V dc operation, contact factory.

TECHNICAL NOTES

1. The DAC-HZ12 series converters are designed and factory calibrated to give ±½ LSB linearity (binary version) with respect to a straight line between end points. This means that if zero and full scale are exactly adjusted externally, the relative accuracy will be ±½ LSB everywhere over the full output range without any additional adjustments.
2. These converters must be operated with local supply by-pass capacitors from +15V to ground and −15V to ground. Tantalum type capacitors of 1 μF are recommended and should be mounted as close as possible to the converter. If the converters are used in a high frequency noise environment a 0.01 μF ceramic capacitor should be used across each tantalum capacitor.
3. When operating in the current output mode the equivalent internal current source of 2 mA must drive both the internal source resistances and the external load resistor. A 300 nanosecond output settling time is achieved for the voltage across a 100 ohm load resistor; for higher value resistors the settling time becomes longer due to the output capacitance of the converter. For fastest possible voltage output for a large transition, an external fast settling amplifier such as DATEL's AM-500 should be used in the inverting mode. Settling time of less than 1 microsecond can be achieved. See application diagram.

CALIBRATION PROCEDURE

1. Select the desired output range and connect the converter up as shown in the Output Range Selection table and the Standard Connection diagrams.
2. To calibrate, refer to the Coding Tables. Note that complementary coding is used.
3. **Zero and Offset Adjustments**
   For unipolar operation set all digital inputs to "1" (+2.0 to +5.5V) and adjust the ZERO ADJ. potentiometer for zero output voltage or current. For bipolar operation set all digital inputs to "1" and adjust the OFFSET ADJ. potentiometer for the negative full scale (for voltage out) or positive full scale (for current out) output value shown in the Coding Table.
4. **Gain Adjustment**
   Set all digital inputs to "0" (0V to +0.8V) and adjust the GAIN ADJ. potentiometer for the positive full scale (for voltage out) or negative full scale (for current out) output value shown in the Coding Table.

OUTPUT RANGE SELECTION

BIN. RANGE	CONNECT THESE PINS TOGETHER			
±10V	15 & 19	17 & 20	—	16 & 24
±5V	15 & 18	17 & 20	—	16 & 24
±2.5V	15 & 18	17 & 20	19 & 20	16 & 24
+10V	15 & 18	17 & 21	—	16 & 24
+5V	15 & 18	17 & 21	19 & 20	16 & 24
±1 mA	—	17 & 20	—	16 & 24
−2 mA	—	17 & 21	—	16 & 24

VOLTAGE OUTPUT IS AT PIN 15.
CURRENT OUTPUT IS AT PIN 20.

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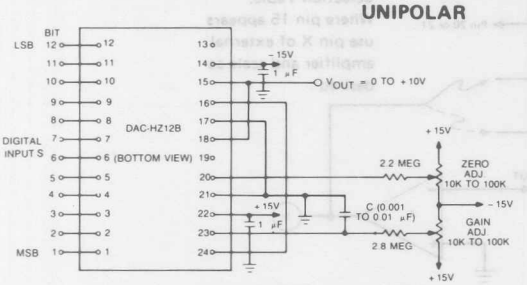
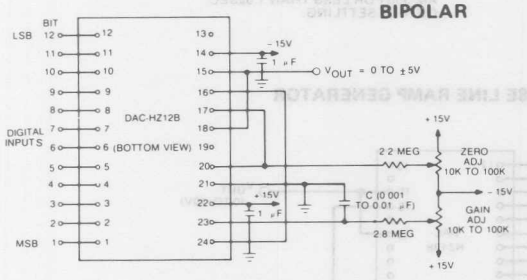
VOLTAGE OUTPUT CONNECTIONS

(FOR DIFFERENT OUTPUT SCALING REFER TO OUTPUT RANGE SELECTION TABLE)

UNIPOLAR

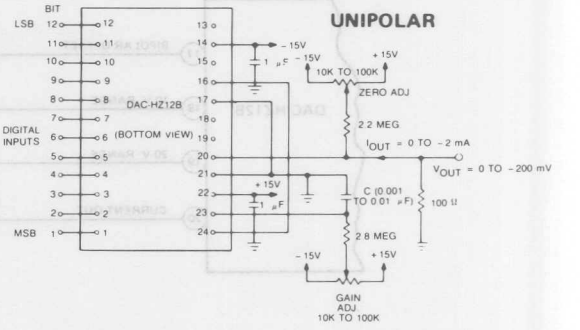


BIPOLAR



CURRENT OUTPUT CONNECTIONS

UNIPOLAR



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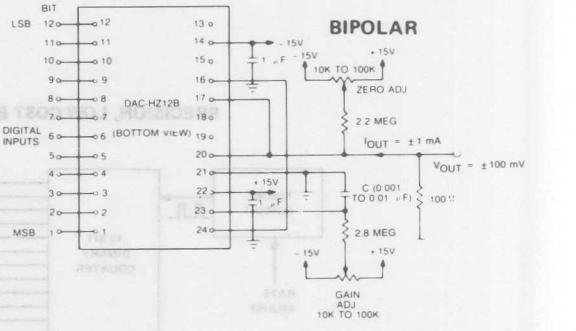


CODING TABLES

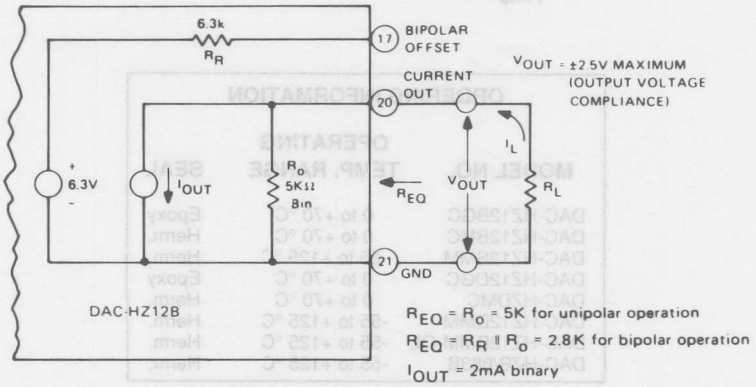
UNIPOLAR OUTPUT — COMPLEMENTARY BINARY

BINARY INPUT CODE			UNIPOLAR OUTPUT RANGES		
MSB		LSB	0 TO +10V	0 TO +5V	0 TO −2 mA
0000	0000	0000	+9.9976V	+4.9988V	−1.9995 mA
0011	1111	1111	+7.5000	+3.7500	−1.5000
0111	1111	1111	+5.0000	+2.5000	−1.0000
1011	1111	1111	+2.5000	+1.2500	−0.5000
1111	1111	1110	+0.0024	+0.0012	−0.0005
1111	1111	1111	0.0000	0.0000	0.0000

BIPOLAR OUTPUT — COMPLEMENTARY OFFSET BINARY

INPUT CODE			BIPOLAR OUTPUT RANGES			
MSB		LSB	±10V	±5V	±2.5V	±1 mA
0000	0000	0000	+9.9951V	+4.9976V	+2.4988V	−0.9995 mA
0011	1111	1111	+5.0000	+2.5000	+1.2500	−0.5000
0111	1111	1111	0.0000	0.0000	0.0000	0.0000
1011	1111	1111	−5.0000	−2.5000	−1.2500	+0.5000
1111	1111	1110	−9.9951	−4.9976	−2.4988	+0.9995
1111	1111	1111	−10.0000	−5.0000	−2.5000	+1.0000

EQUIVALENT CURRENT MODE OUTPUT CIRCUIT

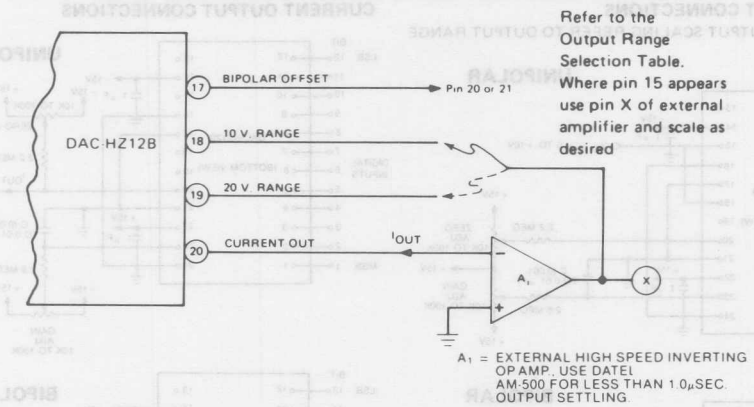


$R_{EQ} = R_o = 5K$ for unipolar operation

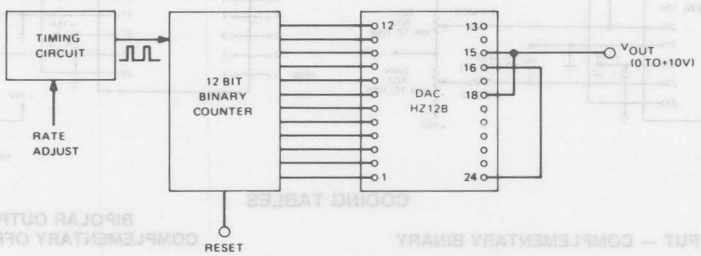
$R_{EQ} = R_R \parallel R_o = 2.8K$ for bipolar operation

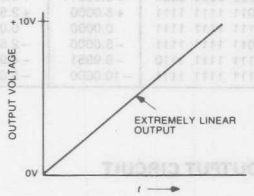
$I_{OUT} = 2mA$ binary

USE OF HIGH SPEED EXTERNAL OP AMP FOR FASTER SETTLING



PRECISION, LOW COST BASE LINE RAMP GENERATOR





THIS CIRCUIT DEVELOPS A HIGHLY LINEAR (.01%) OUTPUT VOLTAGE RAMP FROM 0 TO +10V. THE RAMP CAN BE MADE AS SLOW AS DESIRED WITHOUT AFFECTING LINEARITY BY SETTING THE PULSE RATE OF THE TIMING CIRCUIT TO THE PROPER VALUE. THE OUTPUT RAMP IS GENERATED IN DISCRETE STEPS OF .024% FS (4096 STEPS FOR FS CHANGE).

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE	SEAL
DAC-HZ12BGC	0 to +70 °C	Epoxy
DAC-HZ12BMC	0 to +70 °C	Herm.
DAC-HZ12BMM	-55 to +125 °C	Herm.
DAC-HZ12DGC	0 to +70 °C	Epoxy
DAC-HZDMC	0 to +70 °C	Herm.
DAC-HZ12DMM	-55 to +125 °C	Herm.
DAC-HZ12DMM-QL	-55 to +125 °C	Herm.
DAC-HZB/883B	-55 to +125 °C	Herm.

SAMPLE HOLD AMPLIFIERS

	Model	Linearity (%)	Acquisition Time	Aperture Delay	Aperture Jitter	Bandwidth (MHz)	Hold Mode Droop	Case	Page
	SHM-HU	0.1	25 ns	6 ns	10 ps	50	50 µV/µs	24-Pin DIP	4-23
	SHM-7	0.1	40 ns	3 ns	10 ps	40	100 µV/µs	24-Pin DIP	4-17
	SHM 40	0.1	40 ns	3 ns	10 ps	40	100 µV/µs	24-Pin DIP	4-5
	SHM-6	0.02	2 µs	20 ns	2 ns	5	10 µV/µs	32-Pin DIP	4-15
New	**SHM-43**	0.01	35 ns	5 ns	1 ps	150	5 µV/µs	24-Pin DIP	4-7
Preliminary	**SHM-49**	0.01	140 ns	6 ns	15 ps	16	1 µV/µs	8-Pin DIP	4-25
	SHM-45	0.01	200 ns	6 ns	±50 ps	16	0.5 µV/µs	24-Pin DIP	4-11
	SHM-4860	0.01	200 ns	6 ns	±50 ps	16	0.5 µV/µs	24-Pin DIP	4-13
	SHM-30	0.01	500 ns	-25 ns	0.1 ns	4.5	0.01 µV/µs	14-Pin DIP	4-3
	SHM-20	0.01	1 µs	30 ns	1 ns	2	0.8 µV/µs	14-Pin DIP	4-1
	SHM-91	0.003	2 µs	15 ns	300 ps	2	5 µV/µs	24-Pin DIP	4-19
New	**SHM-945**	0.0004	500 ns	5ns	10 ps	12	0.5 µV/µs	24-Pin DIP	4-21
Advanced	**MSH-840***	0.01	750 ns	6 ns	±1 ns	1	1 µV/µs	32-Pin DIP	4-27

* QUAD Simultaneous Sample-Hold with 4-Channel Multiplexer

Contact DATEL for your
Data Acquisition component
needs.

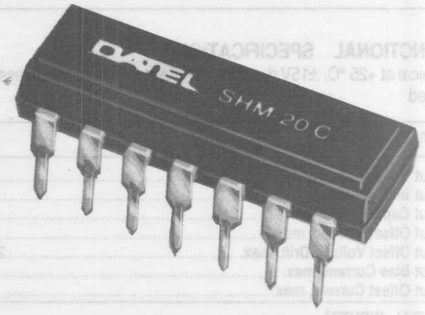
Dial
1-800-233-2765
for
Applications Assistance .

SHM-20

High-Speed, 0.01% Monolithic Sample-hold

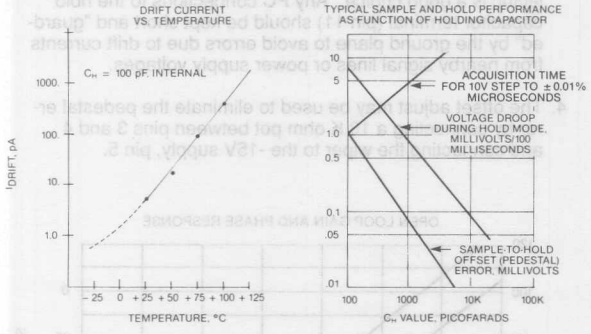
FEATURES

- **Internal hold capacitor**
- **1 Microsecond acquisition time**
- **1 Nanosecond aperture uncertainty**
- **0.01% Accuracy**
- **0.08 MicroV/microsecond droop rate**
- **Differential inputs**

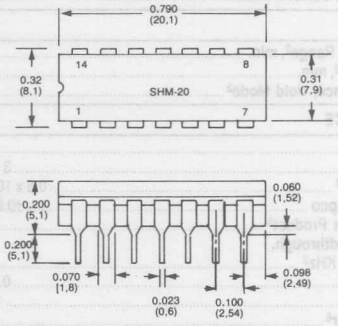


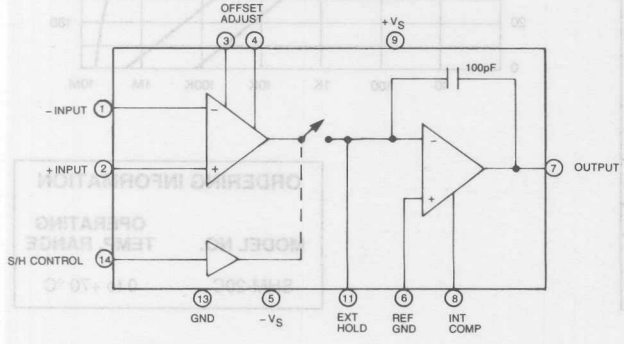
GENERAL DESCRIPTION

DATEL's SHM-20 is a low-cost, complete monolithic sample-hold amplifier which includes an internal 100 pF MOS hold capacitor. Primarily designed for high-speed analog signal processing applications, the SHM-20 features a typical acquisition time of 1.0 microsecond for a 10V input step to 0.01%. Aperture uncertainty is typically 1 nanosecond and droop rate is as low as 0.08 µV/microsecond.



MECHANICAL DIMENSIONS INCHES (MM) MAX.





INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	– INPUT
2	+ INPUT
3	OFFSET ADJUST
4	OFFSET ADJUST
5	– V_S
6	REFERENCE GROUND
7	OUTPUT
8	INTEGRATOR COMPENSATION
9	+ V_S
10	NO CONNECTION
11	EXTERNAL HOLD CAPACITOR
12	NO CONNECTION
13	SUPPLY VOLTAGE GROUND
14	S/H CONTROL

Differential Input Voltage	±24V
Digital Input Voltage, Pin 14	+8 to -15V
Output Current, Continuous[1]	±20 mA

FUNCTIONAL SPECIFICATIONS

Typical at +25 °C, ±15V dc, using internal hold capacitor, unless otherwise noted

ANALOG INPUTS	
Input Voltage Range[2], min.	±10V
Input Impedance, min.	1 MΩ
Input Capacitance, max.	3 pF
Input Offset Voltage, max.	1 mV
Input Offset Voltage Drift, max.	20 µV/ °C
Input Bias Current, max.	300 nA
Input Offset Current, max.	300 nA
DIGITAL INPUTS[2]	
Logic Level High, V_{IN} ("1") min., Hold Mode	2.0V
Logic Level Low, V_{IN} ("0"), max, Sample Mode	0.8V
High Level Inut Current, max.	0,1 µA
Low Level Input Current, max.	10 µA
OUTPUT	
Output Voltage Range[2], min.	±10V
Output Current[2], min.	±10 mA
Output Impedance, Hold Mode[2]	1Ω
PERFORMANCE	
Accuracy	0.01%
DC Gain, min.	3 x 10^5 V/V
Gain Accuracy[4]	0.5 x 10^{-4}% FSR
Gain Error Tempco	±0.6 ppm/ °C
Gain Bandwidth Product[5]	2 MHz
Hold Mode Feedthrough, 10V P-P, 100 KHz[2]	2 mV
Droop Rate	0.08 µV/µS
Droop Rate[2]	1.2 µV/µS
Charge Transfer[6]	0.1 pc
Pedestal Error[9]	1 mV
Total Output Noise, DC to 10 MHz, max.	200 µV RMS
Power Supply Rejection Ratio min.	
+VS	80 dB
-VS	65 dB
DYNAMIC CHARACTERISTICS	
Acquisition Time,	
10V to 0.1%	0.8 µS
10V to 0.01%	1.0 µS
Aperture Delay Time	30 nS
Aperture Uncertainty Time	1 nS
Aperture Time	25 nS
Hold Mode Settling Time, 0.01%[2]	185 nS
Rise Time	100 nS
Overshoot	15%
Slew Rate[7]	45 V/µS
POWER REQUIREMENTS[8]	
Positive Supply, Pin 9	+15V, ±0.5V at 11 mA
Negative Supply, Pin 5	-15V, ±0.5V at -11 mA
PHYSICAL/ENVIRONMENTAL	
Operating Temp. Range	0 to +70 °C
Storage Temp. Range	-65 to +150 °C
Package Type	14-pin, Ceramic DIP

3. Cannot tolerate even a momentary short circuit to ground or either supply.
4. Voltage gain = +1
5. Voltage gain = +1, load resistance = 1 kΩ, load capacitance = 50 pF, output voltage = 100 mV P-P.
6. Input voltage = 0V, digital input voltage = 3.5V.
7. Output voltage = 10V step.
8. A power supply voltage as low as ±12V may be used. However, this will cause some degradation in performance.
9. For C_H = 100 pF. For C_H = 1000 pF Pedestal Error is 0.1 mV. For C_H = 0.01 µF Pedestal Error is 0.01 mV.

TECHNICAL NOTES

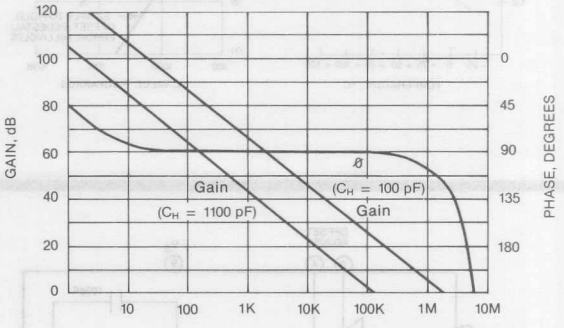
1. A printed circuit board with ground plane is recommended for best performance. The supply pins (pins 5, 9) should be bypassed to ground with a 0.01 to 0.1 µF ceramic capacitor as close to the pins as possible.

2. If an external hold capacitor (C_H) is connected to pins 7 and 11, then a noise bandwidth capacitor with a value of 10% of the value of the external hold capacitor should be connected from pin 8 to signal ground, pin 6. Exact value and type are not critical.

3. The Hold Capacitor (C_H) should have high insulation resistance and low dielectric absorption to minimize droop error. For operating temperatures up to +70 °C, polystyrene dielectric is a good choice. Any PC connections to the hold capacitor terminal (pin 11) should be kept short and "guarded" by the ground plane to avoid errors due to drift currents from nearby signal lines or power supply voltages.

4. The offset adjust may be used to eliminate the pedestal error by connecting a 10 K ohm pot between pins 3 and 4 and connecting the wiper to the -15V supply, pin 5.

OPEN LOOP GAIN AND PHASE RESPONSE



ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
SHM-20C	0 to +70 °C

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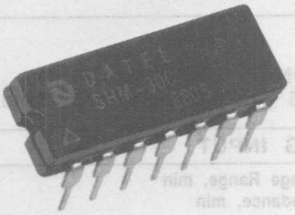
SHM-30C

Very High-Speed 0.01% Monolithic Sample-Hold

FEATURES

- **500 nS Acquisition time to 0.01%**
- **Droop rate of 0.01 μV/μS**
- **Internal hold capacitor**
- **90/V μS Slew rate**
- **Low 0.5 mV offset voltage**



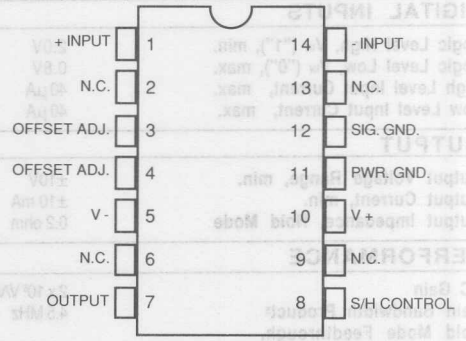
GENERAL DESCRIPTION

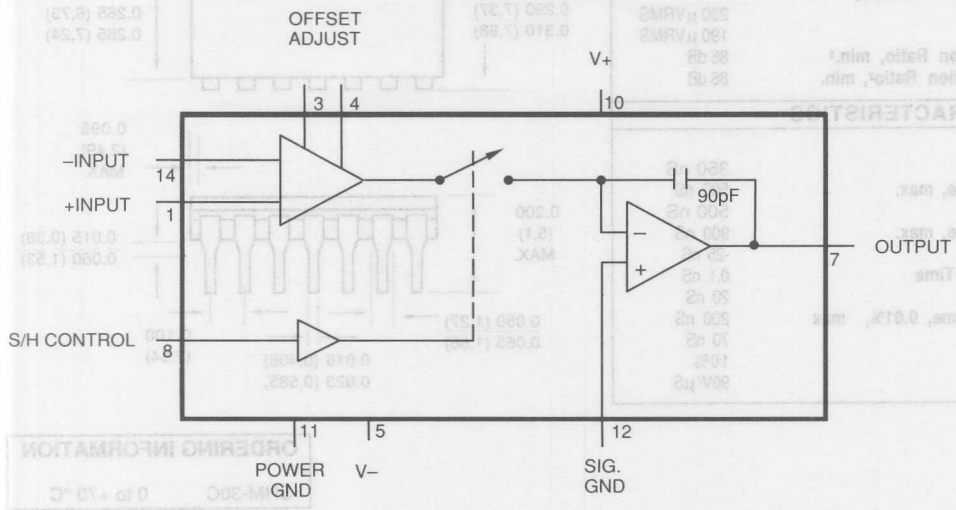
DATEL's SHM-30C is a complete monolithic sample-hold amplifier which includes an internal 90 pF MOS hold capacitor. Primarily designed to be used in precision, high speed data acquisition applications, the SHM-30C features an acquisition time of 500 nS typical to 0.01%, and a droop rate of 0.01 μV/μS, Other salient features of the SHM-30C include an aperture uncertainty time of 0.1 nS, a slew rate of 90 V/μS, and a fully differential input.

The SHM-30C is composed of an input amplifier designed to deliver large amounts of current, a low leakage switch, and an integrator. The low pedestal error of 0.5 mV can be trimmed to zero with a single potentiometer for demanding applications.

The SHM-30C is packaged in a 14-pin ceramic DIP and operates over the temperature of 0°C to +70°C.

Pinout for SHM-30





ABSOLUTE MAXIMUM RATINGS

Voltage between V+ and PWR/SIG GND	+20V
Voltage between V- and PWR/SIG GND	-20V
Differential Input Voltage	+24V
Digital Input Voltage	+8V to -6V
Output Current, Continuous[1]	+17 mA

FUNCTIONAL SPECIFICATIONS

Typical at 25 °C range unless otherwise noted.

ANALOG INPUT

Input Voltage Range, min	±10V
Input Impedance, min	5MΩ
Input Capacitance	3 pF
Input Offset Voltage, max.	1.5 mV
Input Offset Voltage Drift, max.	10 µV/ °C
Input Bias Current, max.	±300 nA
Input Offset Current, max.	300 nA

DIGITAL INPUTS

Logic Level High, V_{IN} ("1"), min.	2.0V
Logic Level Low, V_{IN} ("0"), max.	0.8V
High Level Input Current, max.	40 µA
Low Level Input Current, max.	40 µA

OUTPUT

Output Voltage Range, min.	±10V
Output Current, min.	±10 mA
Output Impedance, Hold Mode	0.2 ohm

PERFORMANCE

DC Gain	2 x 10^6 V/V
Gain Bandwidth Product[5]	4.5 MHz
Hold Mode Feedthrough,	
20V pk-pk, 100 KHz	-88 dB
Droop Rate	0.01 µV/µS
Over Full Temp Range, max.	10 µV/µS
Pedestal Error[4]	0.5 mV
Total Output Noise, DC to 4 MHz,	
Sample Mode	230 µVRMS
Hold Mode	190 µVRMS
Power Supply Rejection Ratio, min.[6]	86 dB
Common Mode Rejection Ratio[2], min.	86 dB

DYNAMIC CHARACTERISTICS

Acquisition Time	
10V to 0.1%	350 nS
over full temp. range, max.	500 nS
10V to 0.01%	500 nS
over full temp. range, max.	900 nS
Aperture Delay Time	-25 nS
Aperture Uncertainty Time	0.1 nS
Aperture Time	20 nS
Hold Mode Settling Time, 0.01%, max	200 nS
Rise Time[3]	70 nS
Overshoot[3]	10%
Slew Rate[5]	90V/µS

POWER REQUIREMENTS

Positive Supply, max. (Pin 10)	+15V @ 24 mA
Negative Supply, max. (Pin 5)	-15V @ 25 mA

PHYSICAL/ENVIRONMENTAL

Operating Temperature Range	0 °C to +70 °C
Storage Temperature Range	-55 °C to +150 °C
Package Type	14-pin, Cerdip

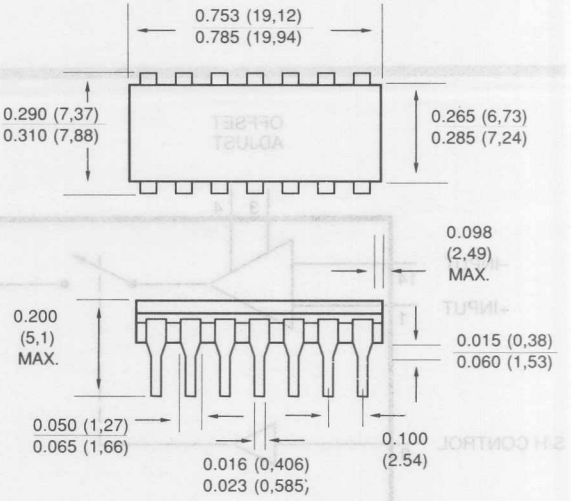
Notes:
1. Internal power dissipation may limit output power below +17 mA
2. V_{CM}= ±10V dc
3. V_O = 200 mV pk-pk, R_L = 2K , C_L = 50 pF
4. V_{IN} = 0V; S/H control signal 3.5V with 20 nS rise time from 0V to 3.5V
5. V_O = 20V Step, R_L = 2K , C_L = 50 pF
6. Based on a three volt delta in each supply, i.e. 15V = ±1.5V dc

TECHNICAL NOTES

1. A printed circuit board with ground plane is recommended for optimum performance. Bypass capacitors (0.01 to 0.1 µF ceramic) should be provided from each power supply terminal to the PWR GND terminal on Pin 11.
2. The internal hold capacitor is 90 pF MOS.
3. The output circuit is not short-circuit protected. Only momentary short-circuits to ground are permissable.

MECHANICAL DIMENSIONS

INCHES (mm) MIN.
INCHES(mm) MAX.



ORDERING INFORMATION

SHM-30C	0 to +70 °C

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SHM-40
Video Speed Sample-Hold

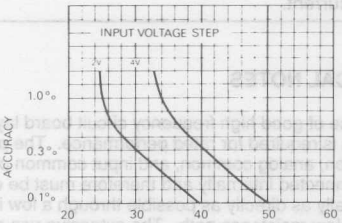
FEATURES

- 40 nSec Acquisition time
- Dual outputs
- 10 pSec Aperture uncertainty
- 40 MHz bandwidth
- 30 mA Output current

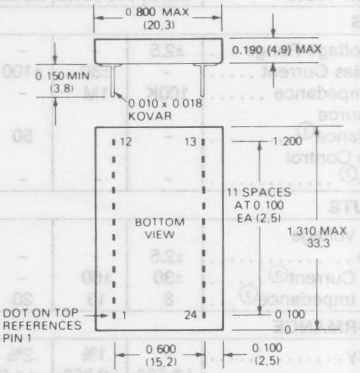
GENERAL DESCRIPTION

DATEL's SHM-40 is an ultra-fast sample and hold designed for high speed analog signal processing applications. The SHM-40 acquires a 2V input change to 0.1% in only 40 nSec and aperture uncertainty time is less than 10 pSec. sample-mode bandwidth is 40 MHz.

The SHM-40 is a complete sample-hold, containing an input buffer amplifier, a precision 53 pF MOS holding capacitor, and two output buffer amplifiers. The sampling switch is controlled by a series 10,000 complementary ECL input. An ECL differential line driver can be conveniently used for the sample control inputs.



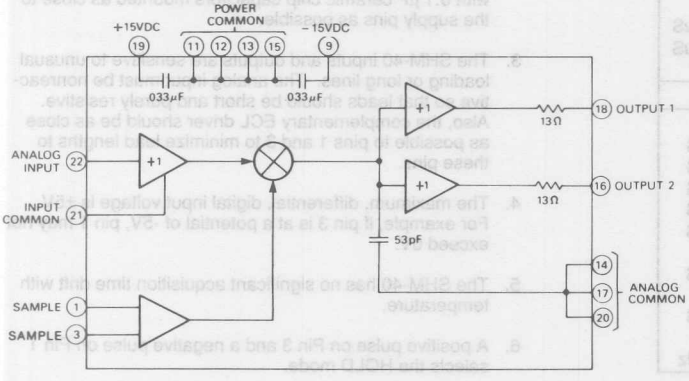
MECHANICAL DIMENSIONS
INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	SAMPLE	13	POWER COM.
2	N.C.	14	ANALOG COM.
3	SAMPLE	15	POWER COM.
4	N.C.	16	OUTPUT 2
5	N.C.	17	ANALOG COM.
6	N.C.	18	OUTPUT 1
7	N.C.	19	+ 15VDC
8	N.C.	20	ANALOG COM.
9	– 15VDC	21	INPUT COM.
10	N.C.	22	ANALOG INPUT
11	POWER COM.	23	N.C.
12	POWER COM.	24	N.C.



ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
SHM-40MC	0 to +70 °C
SHM-40MM	-55 to +125 °C

ABSOLUTE MAXIMUM RATINGS

Positive Supply	-0.5V dc to +18V dc
Negative Supply	+0.5V dc to -18V dc
Digital Input Voltage	-5.0V dc to +5.0V dc
Analog Input Voltage	-5.0V dc to +5.0V dc

FUNCTIONAL SPECIFICATIONS

The following specifications apply over the full operating temperature range and power supply range unless otherwise specified.

DESCRIPTION	MIN.	TYPICAL	MAX.	UNITS
INPUTS				
Input Voltage Range	±2.5	-	-	Vdc
Input Bias Current	-	±30	±100	μA
Input Impedance	100K	1M	-	Ω
Max Source Impedance①	-		50	Ω
Sample Control Inputs②	-	-	-	-
OUTPUTS				
Output Voltage Range	±2.5	-	-	Vdc
Output Current③	±30	±60	-	mA
Output Impedance③	8	13	20	Ω
PERFORMANCE				
Linearity	-	.1%	.2%	% of FS
Gain	+0.980	+0.993	+1.0	-
Gain Tempco	-60	-20	+20	ppm/°C
Sample to Hold Offset Error	-	±15	±50	mV
Sample Mode Offset Voltage	-	±10	±50	mV
Sample to Hold Offset Volt Drift	-	±25	±100	μV/°C
Sample Mode Offset Volt Drift	-	-	-	-
SHM-40MC	-	±143	±714	μV/°C
SHM-40MM	-	±56	±278	μV/°C
	-			
Hold Mode Feedthrough	-	-66	-60	dB
Hold Mode Droop	-	-	-	-
at 25°C	-	20	100	μV/μS
at 125°C	-	500	2500	μV/μS
DYNAMIC CHARACTERISTICS				
Acquisition Time 2V to 0.1%	-	-	40	nS
2V to 1.0%	-	-	25	nS
4V to 0.1%	-	-	50	nS
4V to 1.0%	-	-	35	nS
Aperture Delay Time	-	3	-	nS
Aperture Uncertainty Time	-	10	-	pS
Hold Mode Settling Time	-	20	40	nS
Sample Mode Bandwidth, -3dB	25	40	-	MHz

FUNCTIONAL SPECIFICATIONS (continued)

DESCRIPTION	MIN.	TYPICAL	MAX.	UNITS
POWER SUPPLY REQUIREMENTS				
Supply Voltage Range ±V	±14.5	±15	±15.5	Vdc
Power Supply Rej. Ratio	-20	-30	-	dB
Current Drain ±15V dc	-	60	80	mA
-15V dc	-	60	80	mA
Power Dissipation	-	1.8	2.4	Watts
PHYSICAL/ENVIRONMENTAL				
Thermal Resistance Junction to Case	-	.030	-	°C/mW
Case to Ambient	-	.035	-	°C/mW
Operating Temp. Range SHM-40MC	0°	+25°	+70°	°C
SHM-40MM	-55°	+25°	+125°	°C
Storage Temp.	-65°	+25°	+150°	°C
Package Type Pins	24 Pin, hermetically sealed, ceramic 0.010 x 0.018 in. kovar			

FOOTNOTES:

1. Should be purely resistive. See technical note 3.
2. Input logic voltage levels are V_{in} "0" = -1.5V to -1.4V, and V_{in} "1" = -0.7V to -1.05V. These are differential ECL 10,000.
3. Specified for each output, both outputs may be tied together for decreased output impedance and increased output current.

TECHNICAL NOTES

1. The use of good high frequency circuit board layout techniques is required for rated performance. The power common, analog common, and input common pins are not connected internally and therefore must be connected externally as directly as possible through a low inductance, low resistance path. The extensive use of a ground plane for all common connections is highly recommended.
2. Although they are internally bypassed with 0.033 μF capacitors the supply pins should be externally bypassed with 0.1 μF ceramic chip capacitors mounted as close to the supply pins as possible.
3. The SHM-40 inputs and outputs are sensitive to unusual loading or long lines. The analog input must be nonreactive so that leads should be short and purely resistive. Also, the complementary ECL driver should be as close as possible to pins 1 and 3 to minimize lead lengths to these pins.
4. The maximum, differential, digital input voltage is ±5V. For example, if pin 3 is at a potential of -5V, pin 1 may not exceed 0V.
5. The SHM-40 has no significant acquisition time drift with temperature.
6. A positive pulse on Pin 3 and a negative pulse on Pin 1 selects the HOLD mode.

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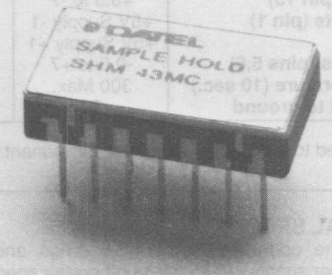
SHM-43

High Speed, 0.01% Hybrid Sample/Hold

FEATURES

- **35 nSec maximum acquisition time to 0.01%**
- **30 nS max. hold mode settling to 0.01%**
- **1 pSec aperture uncertainty**
- **75 MHz small-signal bandwidth**
- **520 mW maximum power dissipation**
- **Small 14-pin DIP package**
- **CMOS control signal**



GENERAL DESCRIPTION

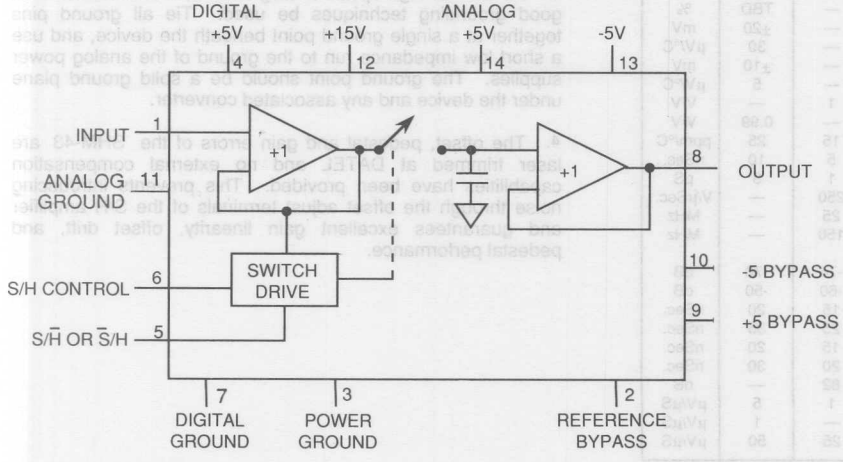
The SHM-43 sample-hold utilizes a proprietary architecture in delivering an acquisition time of 35 nanoseconds maximum to 0.01% and 20 nanoseconds maximum to 0.1% accuracy.

Operation requires ±15 and ±5V supplies and the analog input range is ±2V. Packaged in a small 14-pin DIP, the SHM-43 offers a CMOS compatible sample command while dissipating just 500 milliwatts.

The SHM-43 has been designed for applications that demand fast acquisition times (25 nS .01%), fast hold mode settling (20nS .01%), wide band width, and the ability to drive resistive (100Ω), and capacitive (60pF) loads with no compromise in performance. These features make the SHM-43 an ideal choice for driving flash A/D converters in applications such as radar and communications.

Two temperature ranges are offered; the commercial 0 to +70 °C and military -55 to +125 °C.

PIN	FUNCTION
1	INPUT
2	REF BYPASS
3	POWER GND
4	DIGITAL +5V
5	S/H OR $\overline{S/H}$
6	S/H CONTROL
7	DIGITAL GROUND
8	S/H OUT
9	+5 BYPASS
10	-5 BYPASS
11	ANALOG GROUND
12	+15V POWER
13	-5V
14	ANALOG +5V



ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (pin 12)	-0.5 to +18	V dc
+5V Supply (pin 4, 14)	-0.5 to +7	V dc
-5V Supply (pin 13)	+0.5 to -7	V dc
Analog Inputs (pin 1)	+5V Supply -1	V dc
	+5V Supply +1	V dc
Digital Inputs (pins 5,6)	-0.5 to +7	V dc
Lead Temperature (10 sec.)	300 Max.	°C
Short circuit to ground	70	mA

Output shorted to any supply will cause permanent damage.

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and over the operating power supply range unless otherwise specified.

PARAMETERS	MIN	TYP	MAX	UNITS
Input Voltage Ranges	-2	—	+2	VOLTS
Input Bias Current @25 °C	—	50	—	µA
Input Bias Current TC	—	200	—	nA/°C
Input Impedance	—	160	—	Kohms
Digital Inputs (Digital Supply = +5V)				
Logic Levels				
Logic 1	3.2	—	—	V dc
Logic 0	—	—	1.4	V dc
Logic Loading				
Logic 1	—	—	±1	µA
Logic 0	—	—	±1	µA
OUTPUTS				
Voltage Range	±2	—	—	V
Output Current	±30	—	—	mA
Output Impedance (DC)	—	0.2	—	Ohms
Stable Capacative Load	60	100	—	pF
PERFORMANCE				
Nonlinearity				
DC±1V	—	—	.01	%
DC±2V	—	—	TBD	%
Sample Mode Offset 25 °C	—	—	±20	mV
Sample Mode Offset TC	—	—	30	µV/°C
Pedestal 25 °C	—	—	±10	mV
Pedestal TC End Point Avg.	—	—	5	µV/°C
Gain 25 °C	—	1	—	V/V
Gain Error	0.99	—	0.99	V/V
Gain TC	—	15	25	ppm/°C
Aperture Delay	—	5	10	nSec.
Aperture Jitter	—	1	3	pS
Slew Rate	200	250	—	V/µSec.
Full Power BW ±1.5V	20	25	—	MHz
-3db BW .5VPP	100	150	—	MHz
Harmonic Distortion				
±1V 5MHz	—	-74	-70	dB
±1V 20MHz	—	-60	-50	dB
Acq.Time 0.1% ± 1V	—	15	20	nSec.
Acq.Time 0.01% ± 1V	—	25	35	nSec.
Hold Mode Settling 0.1%	—	15	20	nSec.
Hold Mode Settling 0.01%	—	20	30	nSec.
Feedthrough Rejection 2V Step	76	82	—	dB
Droop Rate, +25 °C	—	1	5	µV/µS
-55 °C	—	—	1	µV/µS
+125 °C	—	25	50	µV/µS

POWER SUPPLY REQUIREMENTS	MIN	TYP	MAX	UNITS
Range				
Analog +5V	+4.75	—	+5.25	V dc
Digital -5V	+4.75	—	+5.25	V dc
-5V	-4.75	—	-5.25	V dc
+15V	+14.25	—	+15.75	V dc
Currents				
Analog +5V	—	30	33	mA
Digital +5V	—	50	100	mA
-5V	—	38	41	mA
+15V	—	8	10	mA
Power Dissipation	—	460	520	mA
Power Supply Rejection	55	60	—	dB
ENVIRONMENTAL				
Operating Temp. Range				
-MC	0	—	+70	°C
-MM	-55	—	+125	°C
Storage Temp. Range	-65	—	+150	°C
Package Type	14-Pin Hermetic DIP			

TECHNICAL NOTES

1. Bypass the +5V analog, +5V digital, +15V supplies with a 1µF, 25V tantalum capacitor in parallel with a 0.01 µF ceramic capacitor mounted as close to the pin as possible.

2. Additional bypass capacitors are necessary, because of internal high switching speeds, and high slew rates of internal components. These additional points (pin 2-REFERENCE, pin 9, +5V, pin 10,-5V) are internal connections that must be bypassed with a minimum of a 1µF tantalum (polarity of connections are shown on the test circuit drawing) capacitor mounted as close to the pin as possible.

3. As with all high speed analog circuits, it is essential that good grounding techniques be used. Tie all ground pins together at a single ground point beneath the device, and use a short low impedance run to the ground of the analog power supplies. The ground point should be a solid ground plane under the device and any associated converter.

4. The offset, pedestal and gain errors of the SHM-43 are laser trimmed at DATEL and no external compensation capabilities have been provided. This prevents introducing noise through the offset adjust terminals of the S/H amplifier and guarantees excellent gain linearity, offset drift, and pedestal performance.

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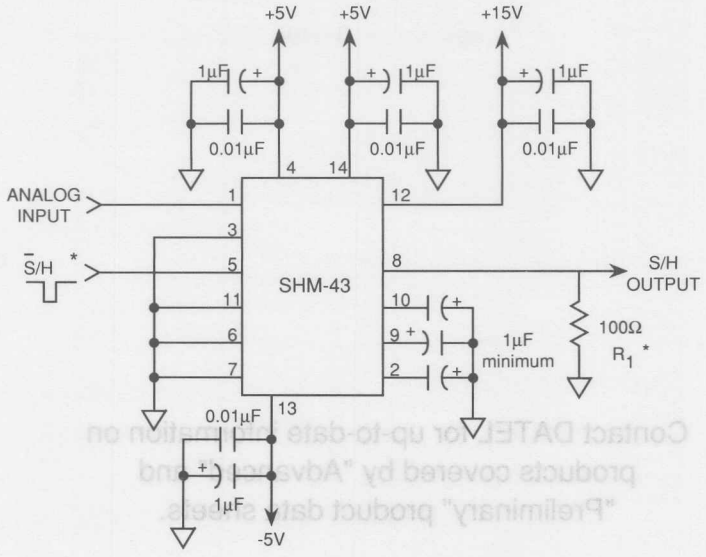
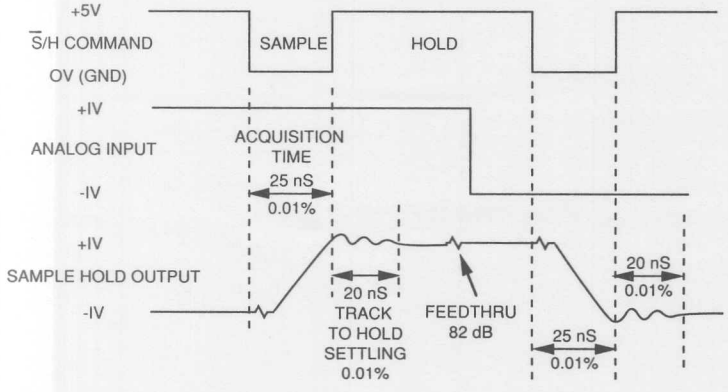
TEST CIRCUIT CONNECTIONS



* Connections shown for $\overline{S/H}$, if opposite polarity sample hold command is desired, connect pin 6 to +5V (pin 4). Using opposite polarity, S/H command will *not* effect speed or accuracy.

* The SHM-43 has been optimised for driving 100Ω loads, R1 should be chosen so that the total load on the S/H is 100Ω.

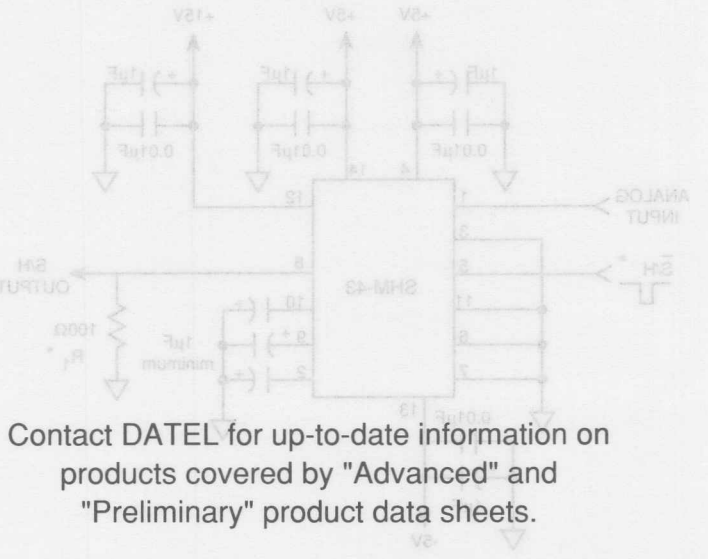
TEST METHOD



ORDERING GUIDE

MODEL NUMBER	TEMP. RANGE
SHM-43MC	0 to +70 °C
SHM-43MM	-55 to +125 °C

Contact DATEL for availability of MIL-STD-883 versions.



Contact DATEL for up-to-date information on products covered by "Advanced" and "Preliminary" product data sheets.

Dial
1-800-233-2765
for
Applications Assistance

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SHM-45

High-Speed Hybrid Precision Sample-hold

FEATURES

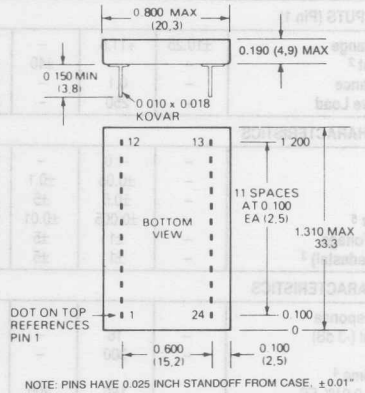
- **Ideally suited for DATEL's Ultra-fast ADC-500/505 A/D converters**
- **200 nSec Maximum acquisition time**
- **0.01% accuracy**
- **100 nSec Maximum sample-hold settling time**
- **74 dB Feedthrough attenuation**
- **±50 pSec Aperture uncertainty**
- **Operable at different gain settings**

GENERAL DESCRIPTION

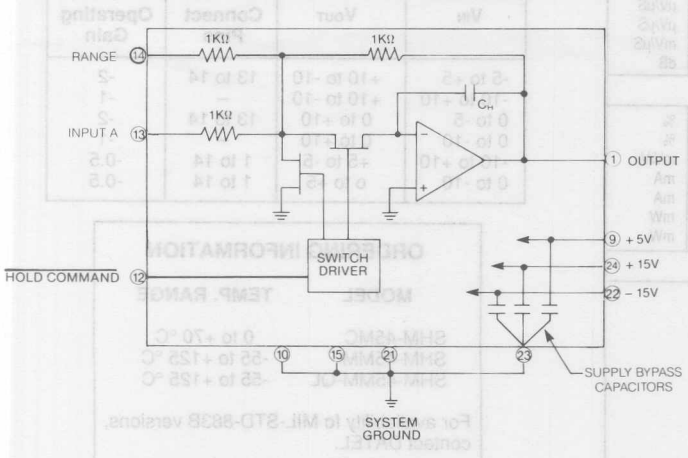
DATEL's SHM-45 is a high-speed, high accuracy sample-hold designed for precision, high-speed analog signal processing applications. Manufactured with modern, high quality hybrid technology, the SHM-45 features excellent dynamic specifications including a maximum acquisition time of only 200 nSec for a 10V step to 0.01%. Sample-to-hold settling time to 0.01% accuracy is 100 nSec maximum with an aperture uncertainty of ±50 pSec.

The SHM-45 is a complete sample-hold circuit, containing a precision MOS hold capacitor and a MOSFET switching configuration which results in faster switching and better feedthrough attenuation. Additionally, an FET input amplifier design allows faster acquisition and settling times while maintaining a considerably lower droop rate.

MECHANICAL DIMENSIONS
INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	OUTPUT	13	INPUT A
2	N/C	14	RANGE
3	N/C	15	GROUND
4	N/C	16	N/C
5	N/C	17	N/C
6	N/C	18	N/C
7	N/C	19	N/C
8	N/C	20	N/C
9	+5V SUPPLY	21	GROUND
10	GROUND	22	–15V SUPPLY
11	N/C	23	GROUND
12	HOLD COMMAND	24	+15V SUPPLY

ABSOLUTE MAXIMUM RATINGS

±15V Supply Voltage (Pins 24, 22)	±18V
+5V Supply Voltage (Pin 9)	−0.5V to +7V
Analog Input (Pin 13, 14)[1]	±18V
Digital Input (Pins 11, 12)	−0.5V to +5.5V
Output Current[2]	±65 mA

FUNCTIONAL SPECIFICATIONS

Specified at +25 °C, gains of -1, ±15V, and +5V power supplies unless otherwise specified.

ANALOG INPUTS (Pin 13, 14)	MIN.	TYP.	MAX.	UNITS
Input Volt. Range [1]	±10	–	–	V
Input Impedance	–	1	–	K ohm
LOGIC INPUTS (TTL)				
Logic 1 Voltage	+2.0	–	–	V
Logic 0 Voltage	–	–	+0.8	V
Logic 1 Current	–	–	40	µA
Logic 0 Current	–	–	-1.6	mA
ANALOG OUTPUTS (Pin 1)				
Output Volt. Range	±10.25	+11.5	–	V
Output Current [2]	–	–	±40	mA
Output Impedance	–	0.1	–	ohm
Max. Capacitive Load	–	250	–	pf
TRANSFER CHARACTERISTICS				
Gain	–	-1.0	–	V/V
Gain Error	–	±0.05	±0.1	%
Gain Tempco	–	±0.5	±5	ppm/ °C
Linearity Error [5]	–	±0.005	±0.01	%FS
Initial Offset Voltage	–	±1	±5	mV
Offset Step (pedestal) [3]	–	±1	±5	mV
DYNAMIC CHARACTERISTICS				
Frequency Response				
Small Signal (-3 dB)	–	16	–	MHz
Slew Rate	–	300	–	V/µS
Acquisition Time [4]				
10V step to 0.01% FS	–	160	200	nS
10V step to 0.1% FS	–	100	170	nS
Aperture Delay Time	–	6	–	nS
Aperture Uncertainty (Jitter)	–	±1	±5	pS
Settling Time				
10V to ±0.01% FS	–	60	100	nS
10V to ±0.1% FS	–	40	–	nS
Droop Rate				
at T = +25 °C	–	0.5	5	µV/µS
at T = +70 °C	–	15	–	µV/µS
at T = +125 °C	–	1.2	–	mV/µS
Feedthrough Rejection	–	-74	–	dB
POWER SUPPLY REQUIREMENTS				
Supply Voltage Range, ±15V	–	±3	–	%
+5V	–	±5	–	%
Power Supply Rej. Ratio	–	±0.5	–	mV/V
Current Drains, +15V	–	+21	+25	mA
-15V	–	-22	-25	mA
+5V	–	+17	+25	mW
Power Consumption	–	730	875	mW
PHYSICAL/ENVIRONMENTAL				
Operating Temperature Range				
SHM-45MC	0 to +70 °C (ambient)			
SHM-45MM/MM-QL	-55 to +125 °C (ambient)			
Storage Temperature Range	-65 to +150 °C			
Thermal Resistance				
Junction-to-Case	0.015 °C/mW			
Case-to-Ambient	0.035 °C/mW			
Package Type	24-pin ceramic			
Pins	Kovar (0.010 x 0.018)			

Footnotes

1. Input signal times gain should not exceed the output voltage range.
2. The SHM-45 output is current limited at approximately ±65 mA. The device can withstand a sustained short to ground. However, shorts to either supply will cause permanent damage.
3. Sample-to-Hold offset error (Pedestal) is constant regardless of input/output level.
4. FS is defined as 10 Volts.

TECHNICAL NOTES

1. All ground pins (10, 15, 21, 23) should be tied together and connected to system analog ground as close to the package as possible. It is recommended to use a ground plane under the device and solder all four ground pins directly to it. Care must be taken to insure that no ground potentials can exist between pin 10 and the other ground pins.
2. Although the power supply pins (9, 22, 24) are internally bypassed to ground with 0.01 µF ceramic capacitors, additional external 0.1 µF to 1 µF tantalum bypass capacitors may be required in critical applications.
3. A logic 1 on the $\overline{\text{HOLD COMMAND}}$ input, pin 12 will put the device in the sample mode. In this mode, the device acts as an inverting unity gain amplifier and its output will track its input. A logic 0 on pin 12 will put the device in the hold mode, and the output will be held constant at the last input level present when the hold command was given.
4. The maximum capacitive load to avoid oscillation is typically 250 pF. Recommended resistive load is 500Ω, although values as low as 250Ω may be used. Acquisition and sample-to-hold settling times are relatively unaffected by resistive loads down to 250Ω and capacitive loads up to 50 pF. However, higher capacitances will affect both acquisition and settling time.
5. The RANGE pin of the SHM-45 is usable to select different output voltage ranges. The output voltage ranges are selectable by hardware programming the SHM-45 to operate at different gains. Table 1 shows the range selection details.

Table 1. Jumper Selections for V_{OUT} Ranges

V_{IN}	V_{OUT}	Connect Pins	Operating Gain
-5 to +5	+10 to -10	13 to 14	-2
-10 to +10	+10 to -10	–	-1
0 to -5	0 to +10	13 to 14	-2
0 to -10	0 to +10	–	-1
-10 to +10	+5 to -5	1 to 14	-0.5
0 to -10	o to +5	1 to 14	-0.5

ORDERING INFORMATION

MODEL	TEMP. RANGE
SHM-45MC	0 to +70 °C
SHM-45MM	-55 to +125 °C
SHM-45MM-QL	-55 to +125 °C

For availability fo MIL-STD-883B versions, contact DATEL.

SHM-4860

High-Speed, 0.01% Hybrid Sample-Hold

FEATURES

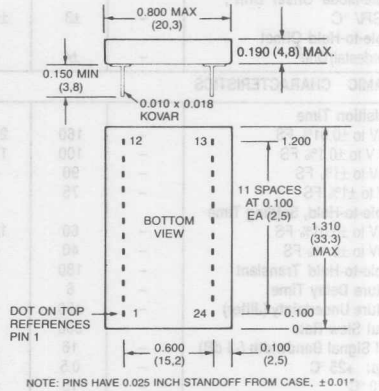
- **200 Nanoseconds maximum acquisition time**
- **0.01% Accuracy**
- **100 Nanoseconds maximum sample-hold settling time**
- **74 dB Feedthrough attenuation**
- **±50 Picoseconds aperture uncertainty**

GENERAL DESCRIPTION

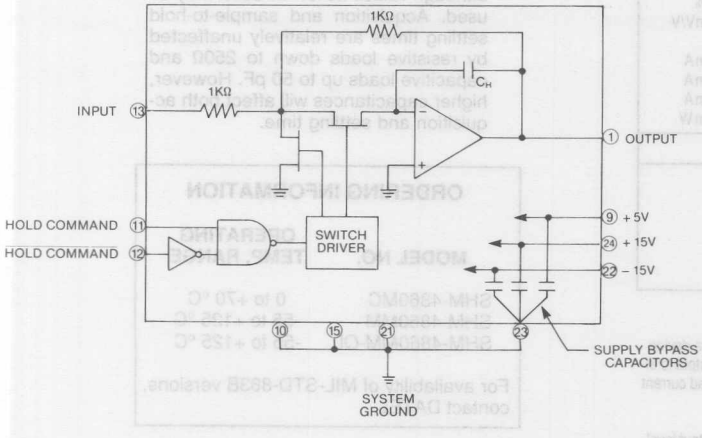
DATEL's SHM-4860 is a high-speed, highly accurate sample-hold designed for precision, high-speed analog signal processing applications. Manufactured using modern, high-quality hybrid technology, the SHM-4860 features excellent dynamic specifications including a maximum acquisition time of only 200 nanoseconds for a 10V step to 0.01%. Sample-to-hold settling time, to 0.01% accuracy, is 100 nanoseconds maximum with an aperture uncertainty of ±50 picoseconds.

The SHM-4860 is a complete sample-hold circuit, containing a precision MOS hold capacitor and a MOSFET switching configuration which results in faster switching and better feedthrough attenuation. Additionally, an FET input amplifier design allows faster acquisition and settling times while maintaining a considerably lower droop rate.

MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	OUTPUT	13	INPUT
2	N/C	14	N/C
3	N/C	15	GROUND
4	N/C	16	N/C
5	N/C	17	N/C
6	N/C	18	N/C
7	N/C	19	N/C
8	N/C	20	N/C
9	+5V SUPPLY	21	GROUND
10	GROUND	22	−15V SUPPLY
11	HOLD COMMAND	23	GROUND
12	HOLD COMMAND	24	+15V SUPPLY

FUNCTIONAL SPECIFICATIONS

Typcal at 25 °C, ±15V, and +5V supplies unless otherwise noted.

ANALOG INPUT/OUTPUT	MIN.	TYP.	MAX.	UNITS
Input/Output Voltage Range	±10.25	±11.5	–	V
Input Impedance	–	1	–	kΩ
Output Current[2]	–	–	±40	mA
Output Impedance	–	0.1	–	kΩ
Maximum Capacitive Load	–	250	–	pF
DIGITAL INPUT				
Input Logic Level				
Logic 1	+2.0	–	5.0	V
Logic 0	0	–	0.8	V
Loading				
Logic 1	–	–	40	mA
Logic 0	–	–	-1.6	mA
TRANSFER CHARACTERISTICS				
Gain	–	1.0	–	V/V
Gain Accuracy	–	±0.05	±0.1	%
Gain Linearity Error[3]	–	±0.005	±0.01	% FS
Sample-Mode Offset Voltage	–	±0.5	±5	mV
Sample-to-Hold Offset Error (Pedestal)[4]	–	±2.5	±20	mV
Gain Tempco (Drift)	–	±0.5	±5	ppm/ °C
Sample-Mode Offset Drift[3], FSR/ °C	–	±3	±15	ppm
Sample-to-Hold Offset (Pedestal) Drift[3]	–	±4	–	ppm
DYNAMIC CHARACTERISTICS				
Acquisition Time				
10V to ±0.01% FS	–	160	200	nS
10 V to ±0.1% FS	–	100	170	nS
10V to ±1% FS	–	90	–	nS
1V to ±1% FS	–	75	–	nS
Sample-to-Hold, Settling Time				
10V to ±0.01% FS	–	60	100	nS
10V to ±0.1% FS	–	40	–	nS
Sample-to-Hold Transient	–	180	–	mV P-P
Aperture Delay Time	–	6	–	nS
Aperture Uncertainty (Jitter)	–	±50	–	pS
Output Slew Rate	–	300	–	µV/µS
Small Signal Bandwidth (-3 dB)	–	16	–	MHz
Droop: +25 °C	–	0.5	5	µV/µS
+70 °C	–	15	–	µV/µS
+125 °C	–	1.2	–	mV/µS
Feedthrough	–	75	–	dB
POWER REQUIREMENTS				
Voltage Range: ±15V	–	±3	–	%
+5V	–	±5	–	%
Power Supply Rejection Ratio	–	±0.5	–	mV/V
Quiescent Current Drain				
+15V	–	+21	+25	mA
-15V	–	-22	-25	mA
+5V	–	+17	+25	mA
Power Consumption	–	730	875	mW
PHYSICAL/ENVIRONMENTAL				
Operating Temperature Ranges				
SHM-4860 MC		0 to +70 °C		
SHM-4860 MM/MM-QL		-55 to +125 °C		
Storage Temperature Range		-65 to +150 °C		
Package Type		24 Pin Ceramic		
Pins		Kovar (0.010 x 0.018)		

Footnotes

1. Input signal should not exceed the supply voltage.
2. The SHM-4860's output is current limited at approximately ±65 mA. The device can withstand a sustained short to ground. However, shorts from the output to either supply will cause permanent damage. For normal operation the load current should not exceed ±40 mA.
3. Fulll Scale (FS) = 10V. Full Scale Range (FSR) = 20V.
4. Sample-to-Hold offset error (Pedestal) is constant regardless of input/output level.

ABSOLUTE MAXIMUM RATINGS	
± 15V Supply Voltage (Pins 24, 22)	± 18V
+ 5V Supply Voltage (Pin 9)	− 0.5V to + 7V
Analog Input (Pin 13)[1]	± 18V
Digital Input (Pins 11, 12)	− 0.5V to + 5.5V
Output Current[2]	± 65 mA

TECHNICAL NOTES

1. All ground pins (10, 15, 21, 23) should be tied together and connected to system analog ground as close to the package as possible. It is recommended to use a ground plane under the device and solder all four ground pins directly to it. Care must be taken to insure that no ground potentials can exist between Pin 10 and the other ground pins.
2. Although the power supply pins (9, 22, 24) are internally bypassed to ground with 0.01 µF ceramic capacitors, additional external 0.1 µF to 1 µF tantalum bypass capacitors may be required in critical applications.
3. A logic "0" on the HOLD COMMAND INPUT, (Pin 11) (or a logic "1" on the HOLD COMMAND INPUT, Pin 12) will put the device in the sample mode. In this mode, the device acts as an inverting unity gain amplifier and its output will track its input. A logic "1" on Pin 11 (logic "0" on Pin 12) will put the device in the HOLD mode, and the output will be held constant at the last input level present when the hold command was given.

   If the HOLD COMMAND INPUT (Pin 11) is used to control the device, Pin 12 must be tied to digital ground. If HOLD COMMAND INPUT (Pin 12) is used to control the device, Pin 11 must be tied to + 5V.
4. The maximum capacitive load to avoid oscillation is typically 250 pF. Recommended resistive load is 500Ω, although values as low as 250Ω may be used. Acquisition and sample-to-hold settling times are relatively unaffected by resistive loads down to 250Ω and capacitive loads up to 50 pF. However, higher capacitances will affect both acquisition and settling time.

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
SHM-4860MC	0 to +70 °C
SHM-4860MM	-55 to +125 °C
SHM-4860MM-QL	-55 to +125 °C

For availability of MIL-STD-883B versions, contact DATEL.

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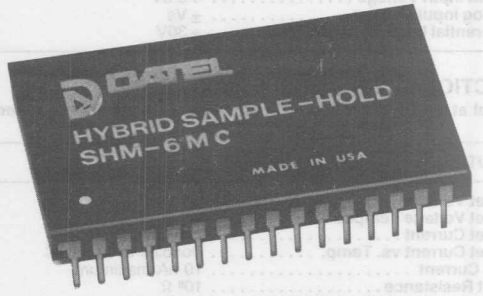
SHM-6

0.02%, 2.0 Microseconds Microelectronic Sample-hold

FEATURES

- **0.02% Accuracy**
- **2.0 Microseconds acquisition time**
- **2 Nanoseconds aperture uncertainty**
- **5 MHz Bandwidth, small signal**
- **25 mA Output current**
- **Gain-programmable from ±1 to ±10**

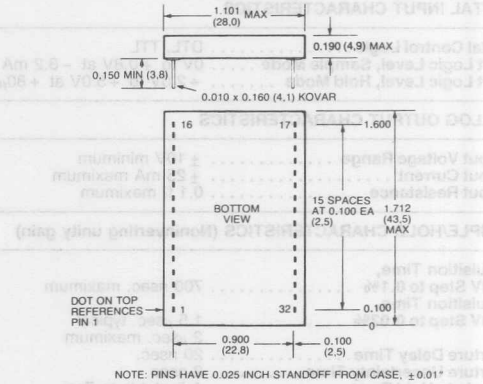


GENERAL DESCRIPTION

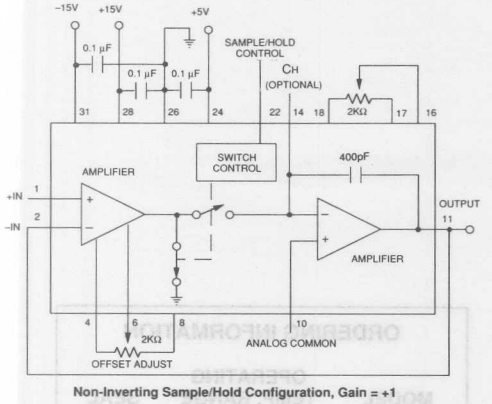
DATEL's SHM-6 is a high-speed, high accuracy sample-hold circuit manufactured with thin-film hybrid technology. This design offers the speed and performance of modular sample-holds with the compactness and integrity of advanced hybrid techniques. The unit's excellent high-speed characteristics include a guaranteed acquisition time of 700 nanoseconds to 0.1% accuracy and 2.0 microseconds to 0.02% for a 10 volt change.

The SHM-6 is a complete sample-hold containing a precision MOS holding capacitor. The input amplifier is an open loop transductance amplifier which can be externally connected for closed loop gains from ±1 to ±10. In addition to its speed, accuracy and selectable gain, the SHM-6 has an output capability of 25 mA. These features allow this unit to offer an unusual degree of adaptability.

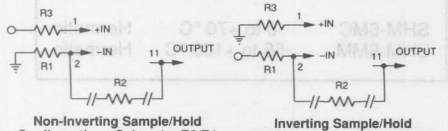
MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"



Non-Inverting Sample/Hold Configuration, Gain = +1



Non-Inverting Sample/Hold Configuration, Gain = 1 + R2/R1

Inverting Sample/Hold Configuration, Gain = –R2/R1

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	+ IN	17	S/H STEP ADJUST.
2	– IN	18	S/H STEP ADJUST.
3	NC	19	NC
4	OFFSET ADJUST	20	NC
5	NC	21	NC
6	OFFSET ADJ. (Wiper)	22	DIGITAL CONTROL
7	NC	23	NC
8	OFFSET ADJUST	24	+ V dc
9	NC	25	NC
10	ANALOG COMMON	26	POWER GROUND
11	OUTPU	27	NC
12	NC	28	+ 15V dc
13	NC	29	NC
14	C.H. (OPTIONAL)	30	NC
15	NC	31	– 15V dc
16	S/H ADJ. (Wiper)	32	NC

ABSOLUTE MAXIMUM RATINGS	
Positive Supply	+18V
Negative Supply	−18V
Logic Supply	+7.0V
Digital Input Voltage	+5.5V
Analog Input Voltage	±Vs
Differential Input Voltage	±30V

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V and +5V supplies unless otherwise noted.

INPUT AMPLIFIER SPECIFICATIONS	
Offset Voltage	±2 mV
Offset Voltage Tempco	±100 µV/°C
Offset Current	1 nA maximum
Offset Current vs. Temp.	Doubles every 10°C
Bias Current	10 nA maximum
Input Resistance	10^8 Ω
Common Mode Voltage Range	±10V minimum
Common Mode Rejection Ratio	74 dB minimum
Open Loop Gain	10^6V/V
Gain Bandwidth Product	5 MHz
Power Supply Rejection Ratio	0.004%/% Supply

DIGITAL INPUT CHARACTERISTICS	
Digital Control Logic	DTL, TTL
Input Logic Level, Sample Mode	0V to +0.8V at −3.2 mA
Input Logic Level, Hold Mode	+2.0V to +5.0V at +80µA

ANALOG OUTPUT CHARACTERISTICS	
Output Voltage Range	±10V minimum
Output Current	±25 mA maximum
Output Resistance	0.1 Ω maximum

SAMPLE/HOLD CHARACTERISTICS (Noninverting unity gain)	
Acquisition Time, 10V Step to 0.1%	700 nsec. maximum
Acquisition Time, 10V Step to 0.02%	1.5 µsec. typical 2 µsec. maximum
Aperture Delay Time	20 nsec.
Aperture Uncertainty Time	2 nsec.
Sample to Hold Error	Adjustable to Zero
Hold Mode Voltage Droop	10 µV/µsec. maximum
Hold Mode Feedthrough	0.02% maximum
Offset	Adjustable to Zero
Gain	±1 to ±10
Gain Error	0.01% maximum
Nonlinearity, V_{OUT} = ±10V	0.02% maximum
Full Power Bandwidth, V_{OUT} = ±10V	500 KHz
Slew Rate	40 V/µsec.

POWER REQUIREMENTS	
Positive Supply	+15V dc ±0.5V at 55 mA
Negative Supply	−15V dc ±0.5V at 60 mA
Logic Supply	+5V dc ±0.5V at 30 mA

PHYSICAL/ENVIRONMENTAL	
Operating Temperature Ranges	
SHM-6MC	0°C to +70°C
SHM-6MM	−55°C to +100°C
Storage Temperature Range	−65°C to +150°C
Package Type	32 Pin Ceramic
Pins	Kovar (0.010 x 0.018)
Weight	0.5 Ounce (14 grams)

TECHNICAL NOTES

1. It is essential that the +15V, -15V, and +5V supplies, pins 28, 31, and 24 respectively, each be bypassed to ground with a 0.1 µF ceramic capacitor connected as close to the pins as possible.

2. Digital Common, pin 26, and Analog Common, pin 10, are not connected together internally, therefore they must be connected externally as directly as possible.

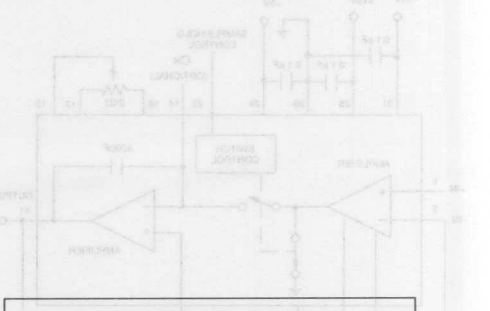
3. An external holding capacitor can be added to decrease hold mode voltage droop but with consequently long acquisition time.

4. In the inverting unity gain operating mode, the feedback and input resistors should be carefully matched or trimmed to yield the desired gain of one. In general, the operating parameters are the same as the noninverting unity gain configuration, except that the sampling bandwidth is reduced by a factor of two. For applications of the SHM-6 with gain greater than one, sampling bandwidth is inversely proportional to gain.

5. Capacitive loads on the output should be limited to 100 pF to maximize acquisition time. The SHM-6 has a ±25 mA current drive capability.

6. The adjustment procedures for the SHM-6 are as follows. Ground the input pin and connect the output to a D.V.M.; operate the offset adjustment potentiometer to yield an output of zero as read on the D.V.M. The sample-hold step adjustment is performed with the input pin grounded and the output connected to an oscilloscope set to 1 mV/cm sensitivity. The digital input pin is driven with a compatible square wave at approximately 250 KHz and the sample-hold step adjustment potentiometer is operated to produce a flat-line output on the oscilloscope.

7. Trim pots should be 100 ppm/ °C cermet type. Gain Resistors should be 100 ppm/ °C, or better, metal film type.



ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE	SEAL
SHM-6MC	0 to +70 °C	Hermetic
SHM-6MM	-55 to +100 °C	Hermetic

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FEATURES

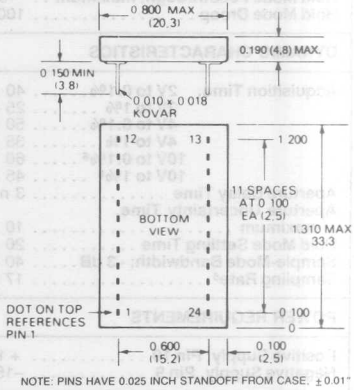
- **40 Nanoseconds acquisition time**
- **Dual outputs**
- **10 Picoseconds aperture uncertainty**
- **40 MHz Bandwidth**
- **30 mA Output current**

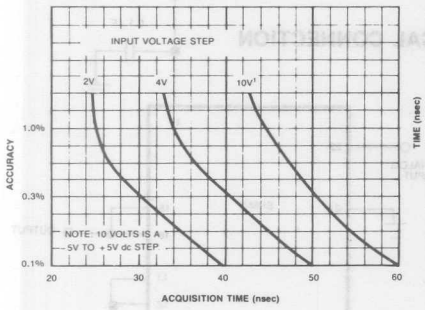
GENERAL DESCRIPTION

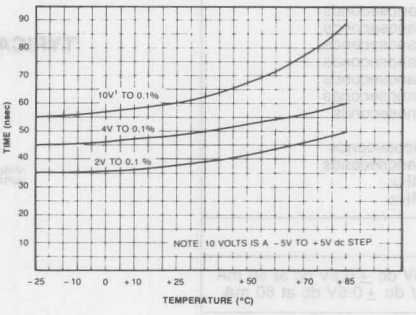
DATEL's SHM-7 is an ultra-fast sample and hold designed for high-speed analog signal processing applications. The SHM-7 acquires a 2V dc input change to 0.1% in only 40 nanoseconds and aperture uncertainty time is less than 10 picoseconds. Sample-mode bandwidth is 40 MHz.

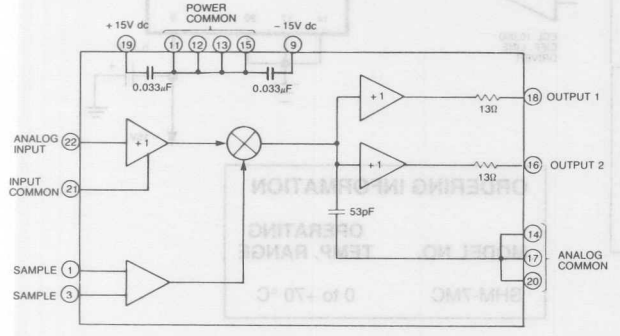
The SHM-7 is a complete sample-hold, containing an input buffer amplifier, a precision 53 pF MOS holding capacitor, and two output buffer amplifiers. The sampling switch is controlled by a series 10,000 complementary ECL input. An ECL differential line driver can be conveniently used for the sample control inputs.

MECHANICAL DIMENSIONS
INCHES (MM)









INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	SAMPLE	13	POWER COM.
2	N.C.	14	ANALOG COM.
3	SAMPLE	15	POWER COM.
4	N.C.	16	OUTPUT 2
5	N.C.	17	ANALOG COM.
6	N.C.	18	OUTPUT 1
7	N.C.	19	+15V dc
8	N.C.	20	ANALOG COM.
9	-15V dc	21	INPUT COM.
10	N.C.	22	ANALOG INPUT
11	POWER COM.	23	N.C.
12	POWER COM.	24	N.C.

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V dc Supplies Unless Otherwise Noted.

INPUTS	
Input Voltage Range[1], minimum	±2.5V dc
maximum	±5V dc
Input Bias Current	50 μA
Input Impedance, minimum	10 kΩ
Maximum Source Impedance[2]	50Ω
Sample Control Inputs[3]	Differential ECL 10,000 Positive Pulse on Pin 3 and Negative Pulse on Pin 1 gives Hold Mode.
OUTPUTS	
Output Voltage Range[1], minimum	±2.5V dc
maximum	±5V dc
Output Current[4]	±30 mA
Output Impedance[4]	13Ω
PERFORMANCE	
Linearity ±2.5V input volt. range	0.1%
±5V input volt. range	0.2%
Gain	+0.995
Gain Tempco, maximum	±33 ppm/°C
Sample-to-Hold Offset Error, maximum	40 mV
Sample-Mode Offset Voltage, maximum	±20 mV
Sample-to-Hold Offset Voltage Drift	75 μV/°C
Sample-Mode Offset Voltage Drift	±250 μV/°C
Hold Mode Feedthrough, maximum	−66 dB
Hold Mode Droop	100 μV/microseconds
DYNAMIC CHARACTERISTICS	
Acquisition Time, 2V to 0.1%	40 nanoseconds
2V to 1%	25 nanoseconds
4V to 0.1%	50 nanoseconds
4V to 1%	35 nanoseconds
10V to 0.1%[6]	60 nanoseconds
10V to 1%[6]	45 nanoseconds
Aperture Delay Time	3 nanoseconds
Aperture Uncertainty Time, maximum	10 picoseconds
Hold Mode Settling Time	20 nanoseconds
Sample-Mode Bandwidth; −3 dB	40 MHz
Sampling Rate[5]	17 MHz
POWER REQUIREMENTS	
Positive Supply, Pin 19	+15V dc ±0.5V dc at 60 mA
Negative Supply, Pin 9	−15V dc ±0.5V dc at 60 mA
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Ranges SHM-7MC	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Package Type	24 Pin, hermetically sealed, ceramic.
Pins	0.010 x 0.018 Inch Kovar

FOOTNOTES:

1. The SHM-7MC has a maximum input/output voltage range of ±5V.
2. Should be purely resistive. See technical note 3.
3. Input logic voltage levels are V_{in} "0" = −1.5V to −1.4V, and V_{in} "1" = −0.7V to −1.05V.
4. Specified for each output, both outputs may be tied together for decreased output impedance and increased output current.
5. For a ±2V input.
6. 10V is a step from −5V to +5V dc.

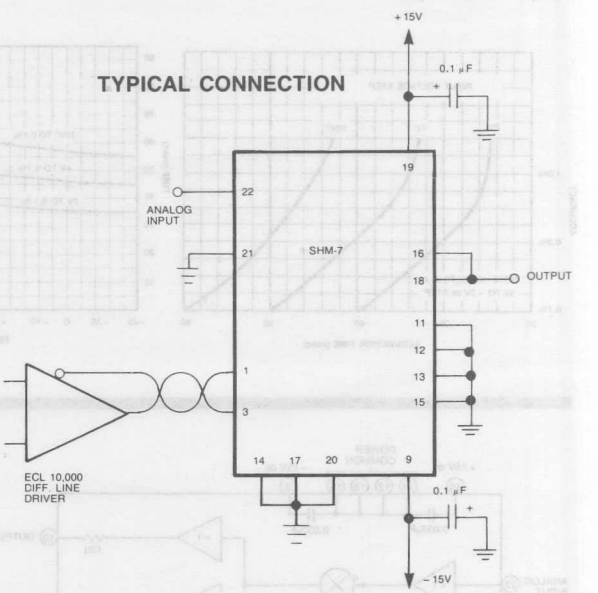
ABSOLUTE MAXIMUM RATINGS

Positive Supply	+18V dc
Negative Supply	−18V dc
Digital Input Voltage	±5V dc
Analog Input Voltage	±5V dc

TECHNICAL NOTES

1. The use of good high frequency circuit board layout techniques is required for rated performance. The power common, analog common, and input common pins are not connected internally and therefore must be connected externally as directly as possible thorugh a low inductance, low resistance path. The extensive use of a ground plane for all common connections is highly recommended.
2. Although they are internally bypassed with 0.033 μF capacitors the supply pins should be externally bypassed with 0.1 μF ceramic chip capacitors mounted as close to the supply pins as possible.
3. The SHM-7 inputs and outputs are sensitive to unusual loading or long lines. The analog input must be non-reactive so that leads should be short and purely resistive. Also, the complementary ECL driver should be as close as possible to pins 1 and 3 to minimize lead lengths to these pins.
4. The maximum, differential, digital input voltage is ±5V. For example, if pin 3 is at a potential of -5V, pin 1 may not exceed 0V.

TYPICAL CONNECTION



ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
SHM-7MC	0 to +70 °C

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SHM-91
Precision Dual Sample-and-Hold

FEATURES

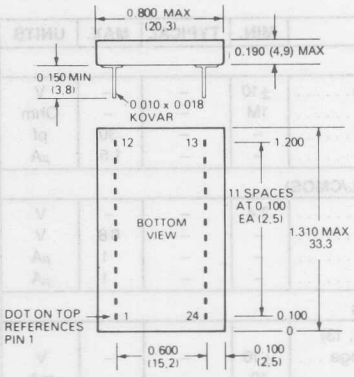
- **Contains two precision sample-hold amplifiers**
- **Designed for use with 12- or 14-bit A/D converters**
- **Fast acquisition time (2 μSec to ± 0.002%)**
- **No external components required**
- **Wide temperature range (-55 to +125°C available)**
- **24-pin dual in-line package**
- **Multiplexed inputs and outputs for application versatility**

GENERAL DESCRIPTION

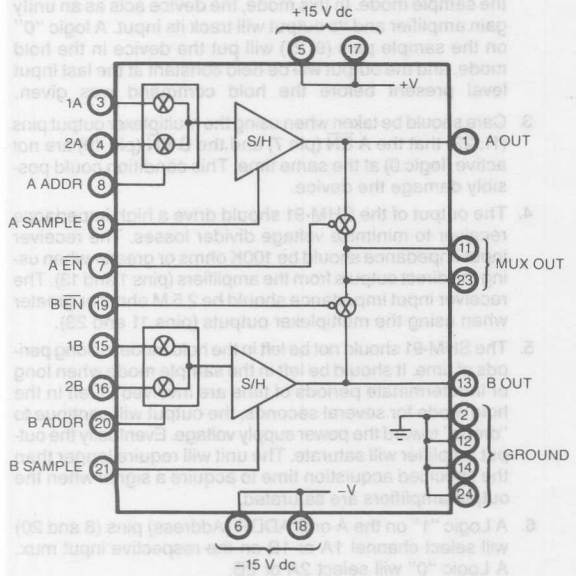
DATEL's SHM-91 is a high performance/high resolution dual sample-hold amplifier. This hybrid device is designed for multi-channel analog signal processing applications with 12- to 14-bit accuracy requirements. Typical applications for this device would demand high speed and high resolution. The SHM-91 offers both of these features at a low cost.

The SHM-91 consists of two separate sample-hold amplifiers, each independently controlled to allow flexibility when implementing a system design. Each half consists of a two-channel input multiplexer and a sample-hold amplifier. The output of each sample-hold is available directly or through a multipelxed output.

MECHANICAL DIMENSIONS
INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"



INPUT/OUTPUT CONNECTIONS

PIN	SIGNAL
1	A OUT
2	GROUND
3	1A
4	2A
5	+15V dc
6	−15V dc
7	A $\overline{EN}$
8	A ADDR
9	A SAMPLE
10	NO CONNECTION
11	MUX OUT
12	GROUND
13	B OUT
14	GROUND
15	1B
16	2B
17	+15V dc
18	−15V dc
19	B $\overline{EN}$
20	B ADDR
21	B SAMPLE
22	NO CONNECTION
23	MUX OUT
24	GROUND

ORDERING INFORMATION

MODEL	TEMP. RANGE
SHM-91MC	0 to +70 °C
SHM-91MM	-55 to +125 °C

ABSOLUTE MAXIMUM RATINGS

Positive Supply (Pins 5, 17)	−0.5V dc to +18V dc
Negative Supply (Pins 6, 18)	+0.5V dc to −18V dc
Digital Input Voltages	
Address, Sample (Pins 8, 9, 20, 21)	−0.5V dc to +7V dc
Mux. Enable (Pins 7, 19)	−18V dc to +18V dc
Analog Input Voltage	±15V dc

FUNCTIONAL SPECIFICATIONS

The following specifications apply over the full operating temperature range and power supply range unless otherwise specified. For test aspects, contact the factory.

DESCRIPTION	MIN.	TYPICAL	MAX.	UNITS
ANALOG INPUTS				
Input Voltage Range	±10	–	–	V
Input Impedance	1M	–	–	Ohm
Input Capacitance	–	–	30	pf
Input Bias Current	–	–	1.5	μA
LOGIC INPUTS (TTL/CMOS)				
Logic 1 voltage	2.4	–	–	V
Logic 0 voltage	–	–	0.8	V
Logic 1 current	–	–	1	μA
Logic 0 current	–	–	1	μA
ANALOG OUTPUTS				
Direct Output (pins 1, 13)				
Output Voltage Range	±10	–	–	V
Output Current	10	–	–	mA
Output Impedance	–	1	2	Ohm
Mux. Output (pins 11, 23)				
Output Voltage Range	±10	–	–	V
Output Current	10	–	–	mA
Output Impedance	–	50	150	Ohms
OFF Output Leakage	–	–	1	μA
OFF Output Capacitance	–	–	20	pf
Output Switch Delay	–	–	500	nS
PERFORMANCE				
Gain (1)	–	+1	–	–
Gain Error (1)	–	–	±0.02	%
Gain Tempco	–	1	10	ppm/°C
Linearity Error (1)	–	–	0.003	% FSR
Linearity Tempco.	–	–	±1	ppm/°C
Initial Offset Voltage (2)	–	–	±1	mV
Offset Tempco., Hold Mode	–	20	50	μV/°C
Crosstalk, channel-to-channel	-90	–	–	dB
Offset Tempco. Tracking (A vs. B)	–	±10	±20	μV/°C
Gain Tracking (A vs. B)	–	–	±50	ppm
Gain Tracking Tempco.	–	–	±0.5	ppm/°C
PHYSICAL/ENVIRONMENTAL				
Thermal Resistance				
Junction-to-Case	–	0.015	–	°C/mW
Case-to-Ambient	–	0.035	–	°C/mW
Operating Temp. Range				
SHM-91MC	0 to +70 °C (ambient)			
SHM-91MM	-55 to +125 °C (ambient)			
Storage Temperature Range	-55 to +125 °C			
Package Type	24-pin hermetically sealed ceramic DIP			

T/H SWITCHING	MIN.	TYP.	MAX.	UNITS
Aperture Delay Time	–	15	–	nS
Aperture Uncertainty (Jitter)	–	300	1,000	pS
Offset Step (2)	–	–	±1	mV
Settling Time to ±2 mV	–	–	600	nS
HOLD MODE DYNAMICS				
Droop Rate: +25 °C	–	–	5	μV/μS
+85 °C	–	–	10	μV/μS
+125 °C	–	–	100	μV/μS
Feedthrough Rejection	-90	–	–	dB
HOLD-TO-TRACK DYNAMICS				
Acquisition Time				
10V Step to ±0.2 mV	–	–	2	μS
10V Step to ±1 mV	–	–	1.5	μS
POWER SUPPLY REQUIREMENTS				
Supply Voltage Range ±V	±14.5	±15	±15.5	V dc
Power Supply Rej. Ratio	-60	–	–	dB
Current Drains: ±15V dc	–	–	30	mA
-15V	–	–	30	mA
Power Dissipation	–	700	900	mW
TRACK MODE DYNAMICS				
Frequency Response				
Small Signal (−3dB)	–	–	1	Mhz
Slew Rate	–	45	–	V/μS

1. Specified at +25 °C.
2. Tested at ±25 °C with input source impedance of 50 ohms.

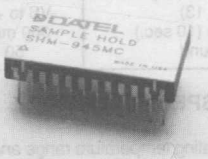
TECHNICAL NOTES

1. All ground pins (2, 12, 14, 24) should be tied together and connected to system analog ground as close to the package as possible. It is recommended to use a ground plane under the device and solder all four ground pins directly to it. The power supply pins (5, 6, 17, 18) should be bypassed to analog ground with .01 μF ceramic capacitors located as close to the pins as possible. In certain critical applications, additional bypass precautions using 0.1 or 1.0 μF tantalum capacitors are suggested.
2. A logic "1" on the sample pins (9, 21) will put this device in the sample mode. In this mode, the device acts as an unity gain amplifier and its output will track its input. A logic "0" on the sample pins (9, 21) will put the device in the hold mode, and the output will be held constant at the last input level present before the hold command was given.
3. Care should be taken when using the multiplexer output pins (11, 23) that the A $\overline{EN}$ (pin 7) and the B $\overline{EN}$ (pin 19) are not active (logic 0) at the same time. This condition could possibly damage the device.
4. The output of the SHM-91 should drive a high impedance receiver to minimize voltage divider losses. The receiver input impedance should be 100K ohms or greater when using the direct outputs from the amplifiers (pins 1 and 13). The receiver input impedance should be 2.5 M ohms or greater when using the multiplexer outputs (pins 11 and 23).
5. The SHM-91 should not be left in the hold mode for long periods of time. It should be left in the sample mode when long or indeterminate periods of time are involved. If left in the hold mode for several seconds, the output will continue to "droop" toward the power supply voltage. Eventually the output amplifier will saturate. The unit will require longer than the specified acquistion time to acquire a signal when the output amplifiers are saturated.
6. A Logic "1" on the A or B ADDR (Address) pins (8 and 20) will select channel 1A or 1B on the respective input mux. A Logic "0" will select 2A or 2B.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

SHM-945

High-Speed Hybrid Precision Sample-hold



FEATURES

- **500 nSec Maximum acquisition time to 0.00076%**
- **Differential input**
- **0.0004% Linearity**
- **16-Bit Performance over military temperature range**
- **Small 24-DDIP package**
- **Operates at different gain settings**

GENERAL DESCRIPTION

DATEL's SHM-945 is a precision, high-speed sample-and-hold featuring a maximum acquisition time of 500 nanoseconds to 0.00076% accuracy. Differential inputs are provided to reject common-mode signals found in applications requiring 16-bit accuracy. A range pin allows gain selections of -0.5, -1, and -2.

The SHM-945 contains an internal hold capacitor with internal compensation networks for pedestal error, feedthrough and dielectric absorption.

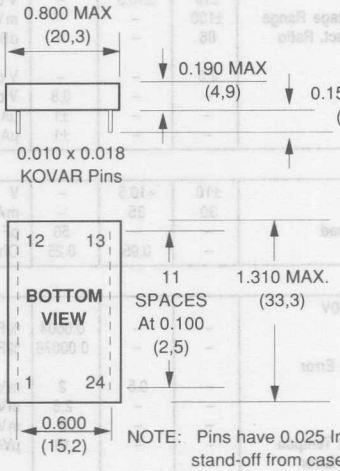
TECHNICAL NOTES

1. Bypass the ±15V and +5V supplies with a 1 µF, 25V tantalum electrolytic capacitor in parallel with a 0.01 ceramic capacitor, mounted as close to the pin as possible.

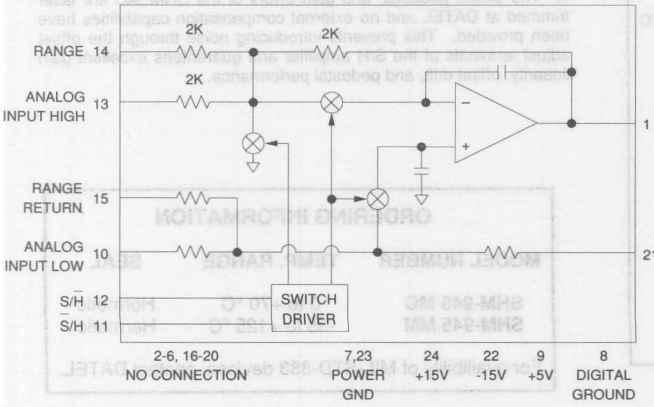
2. Tie all ground pins together at a single ground point beneath the device and use a short, low impedance run to the ground of the analog power supplies. The ground point should be a solid ground plane under the sample/hold and data converter.

3. Differential amplifier - high-resolution applications frequently require the ability to sense ground at a distant signal source. To avoid errors due to different ground potential, use the SHM-945's analog input low (pin 10) to sense the ground at the signal source. In noisy applications, using shielded twisted pair wire, with one end of the shield tied to ground at the sample/hold, is recommended. Analog Input Low and Range Return (when used) must be ≤ 100 mV maximum with respect to Analog Ground.

MECHANICAL DIMENSIONS
INCHES (mm)



NOTE: Pins have 0.025 Inch ±0.01 stand-off from case.



PIN	FUNCTION
1	ANALOG OUTPUT
2	NO CONNECTION
3	NO CONNECTION
4	NO CONNECTION
5	NO CONNECTION
6	NO CONNECTION
7	POWER GROUND
8	DIGITAL GROUND
9	+5V
10	ANALOG INPUT LOW
11	SAMPLE/HOLD
12	SAMPLE/HOLD
13	ANALOG INPUT HIGH
14	RANGE
15	RANGE RETURN
16	NO CONNECTION
17	NO CONNECTION
18	NO CONNECTION
19	NO CONNECTION
20	NO CONNECTION
21	ANALOG GROUND
22	-15V SUPPLY
23	POWER GROUND
24	+15V SUPPLY

PARAMETERS	LIMITS	UNITS
+15V Supply (pin 24)	-0.5 to +18	V dc
-15V Supply (pin 22)	+0.5 to -18	V dc
+5V Supply (pin 9)	-0.5 to +7	V dc
Digital Inputs (pins 11,12)	-0.5 to +7	V dc
Analog Inputs (pin 13)	-VS to +VS	V dc
Lead Temperature (10 sec.)	300 max.	°C
Short circuit to ground	50	mA

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and over the operating power supply range unless otherwise specified. Gain = -1.

INPUTS	MIN	TYP	MAX	UNITS
Voltage Ranges	±10	±10.5	–	V dc
Common Mode Voltage Range	±100	–	–	mV
Common Mode Reject. Ratio	86	–	–	dB
Digital Input				
Logic 1 Levels	2.0	–	–	V dc
Logic 0 Levels	–	–	0.8	V dc
Logic 1 Loading	–	–	±1	µA
Logic 0 Loading	–	–	±1	µA
OUTPUTS				
Voltage Ranges	±10	+10.5	–	V
Output Current	30	35	–	mA
Stable Capacitive Load	–	–	50	pF
Output Impedance	–	0.05	0.25	Ohms
PERFORMANCE				
Nonlinearity: DC ±10V				
+25 °C	–	–	0.0004	%FS
-55 to +125 °C	–	–	0.00076	%FS
Sample Mode Offset Error				
+25 °C	–	0.5	2	mV
0 to +70 °C	–	–	2.5	mV
-55 to +125 °C	–	–	3	mV
Sample Mode Offset Tempco	–	–	10	µV/ °C
S/H Offset (Pedestal) Error				
+25 °C	–	±2	±5	mV
0 to +70 °C	–	±5	±7.5	mV
-55 to +125 °C	–	±7	±10	mV
Pedestal Tempco	–	2	5	ppm/ °C
Pedestal Nonlinearity	–	–	0.00076	%FS
Gain	–	-1	–	V/V
Gain Error				
25 °C	–	–	±0.02	%FS
0 to +70 °C	–	–	±0.035	%FS
-55 to +125 °C	–	–	±0.05	%FS
Gain Tempco	–	3	5	ppm/ °C
Harmonic Distortion (below FS) ①	-96	–	–	dB
Acq. Time, ±0.003 %FS 10V Step				
+25 °C	–	275	350	nSec.
0 to +70 °C	–	–	350	nSec.
-55 to +125 °C	–	–	425	nSec.
Acq. Time, ±0.003 %FS 20V Step				
+25 °C	–	375	400	nSec.
0 to +70 °C	–	–	450	nSec.
-55 to +125 °C	–	–	500	nSec.
Acq. Time, ±0.00076 %FS 10V Step				
+25 °C	–	400	500	nSec.
0 to +70 °C	–	–	550	nSec.
-55 to +125 °C	–	–	600	nSec.
Acq. Time, ±0.00076 %FS 20V Step				
+25 °C	–	550	650	nSec.
0 to +70 °C	–	–	700	nSec.
-55 to +125 °C	–	–	750	nSec.
Aperture Delay, +25 °C	–	5	10	nSec.
-55 to +125 °C	–	–	13	nSec.
Aperture Uncertainty, +25 °C	–	10	15	pSec.
-55 to +125 °C	–	–	30	pSec.
Slew Rate	120	150	–	V/µSec.
Full Power BW (±FS)	1.6	1.9	–	MHz
Small Signal BW (-3 dB)	12	16	–	MHz
Hold Mode Settling, ±0.003 %FS				
+25 °C	–	130	150	nSec.
0 to +70 °C	–	–	150	nSec.
-55 to +125 °C	–	–	175	nSec.
Hold Mode Settling, ±0.00076 %FS				
+25 °C	–	200	250	nSec.
0 to +70 °C	–	–	250	nSec.
-55 to +125 °C	–	–	300	nSec.
Feedthrough Rejection 10V Step	92	100	–	dB
Droop Rate, +25 °C	–	0.5	1	µV/µS
0 to +70 °C	–	–	50	µV/µS
-55 to +125 °C	–	250	500	µV/µS
Output Noise, Hold Mode	–	60	80	µV RMS
POWER SUPPLY REQUIREMENTS				
Range, +15V	+14.25	+15.0	+15.75	V dc
-15V	-14.25	-15.0	-15.75	V dc
+5V	+4.75	+5.0	+5.25	V dc
Current, +15V	–	+10	+12	mA
-15V	–	-10	-12	mA
+5V	–	+0.5	+1.5	mA
Power Dissipation	–	305	385	mW
Power Supply Rejection	88	110	–	dB
ENVIRONMENTAL				
Operating Temp. Range				
-MC	0	–	+70	°C
-MM	-55	–	+125	°C
Storage Temp. Range	-65	–	+150	°C
Package Type	14-pin Hermetic DIP			
Weight	0.28 Oz. (8 grams) max.			

① (DC to 1 MHz, 10V pk-pk).

4. For a gain of -0.5, connect pin 14 (RANGE) to pin 1 (ANALOG OUTPUT) and tie pin 15 (RANGE RETURN) to ground.

5. For a gain of -2, connect pin 14 to pin 13 (ANALOG INPUT) and tie pin 15 to ground.

6. When using $\overline{\text{Sample}}$/Hold (pin 11) connect pin 12 to Digital Ground. If using the Sample/$\overline{\text{Hold}}$ polarity (pin 12) tie pin 11 to +5V.

7. The offset, pedestal, and gain errors of the SHM-945 are laser trimmed at DATEL and no external compensation capabilities have been provided. This prevents introducing noise through the offset adjust terminals of the S/H amplifier and guarantees excellent gain linearity, offset drift, and pedestal performance.

ORDERING INFORMATION

MODEL NUMBER	TEMP. RANGE	SEAL
SHM-945 MC	0 to +70 °C	Hermetic
SHM-945 MM	-55 to +125 °C	Hermetic

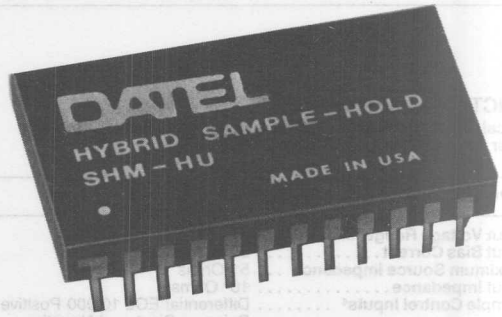
For availibility of MIL-STD-883 devices, contact DATEL.

SHM-HU

Ultra-Fast, 0.1% Micro-Electronic Sample-hold

FEATURES

- **25 Nanoseconds acquisition time**
- **50 MHz Bandwidth**
- **10 Picoseconds aperture uncertainty**
- **Up to 8-bit accuracy**
- **±2.5V Input range**



GENERAL DESCRIPTION

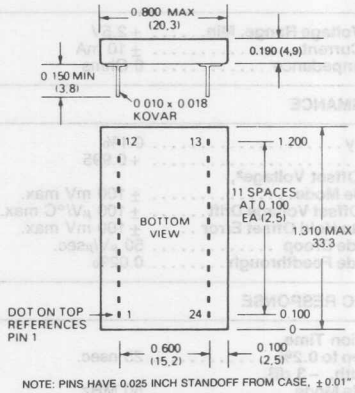
DATEL's SHM-HU is an ultra high-speed sample-hold capable of video speed signal processing. The SHM-HU acquires a full-scale 5V input change in just 25 nanoseconds and features a 10 picoseconds aperture uncertainty time. Bandwidth is 50 MHz and the slew rate is 200 V/microseconds.

Through the use of thin-film hybrid construction, this ultra high-speed circuit is contained in a miniature 24-pin ceramic package. A 53 picofarad MOS hold capacitor is incorporated inside the package and provision is made for externally added capacitance when necessary. The sample-hold requires four external resistors and an LH0033 fast buffer amplifier for completion. The circuit is zeroed by adjustment of the LH0033 amplifier.

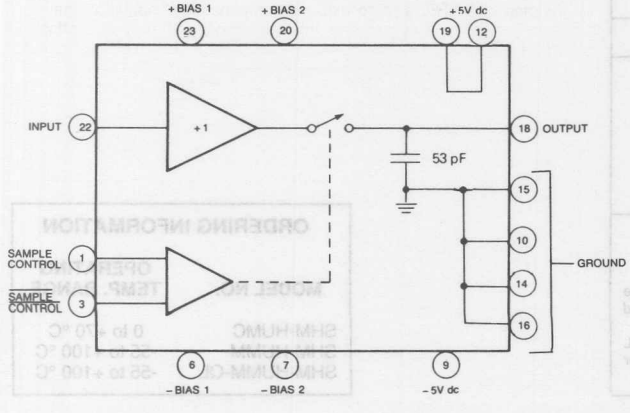
Other features of this unit include a ±2.5V input/output voltage range and a fixed gain of 0.0955. The sampling switch is controlled by a complementary series 10,000 ECL input. An ECL differential line driver can be conveniently used for the sample control inputs.

Power requirements are ±15V dc at 60 mA and ±5V dc at 70 mA. There are three basic models covering two operating temperature ranges, 0 to +70°C, and -55 to +100°C.

MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 INCH STANDOFF FROM CASE, ±0.01"



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	SAMPLE CONTROL
3	SAMPLE CONTROL
6	-BIAS 1
7	-BIAS 2
9	-5V POWER
10	GROUND
12	+5V POWER
14	GROUND
15	GROUND
16	GROUND
18	OUTPUT
19	+5V POWER
20	+BIAS 2
22	INPUT
23	+BIAS 1

NOTE: ALL OTHER PINS ARE NO CONNECTION

ABSOLUTE MAXIMUM RATINGS	
Power Supplies, Pins 9-19	±6V
Analog Input Voltage, Pin 22	±5V
Sample Inputs, Pins 1 & 3	±5V Differential
Current, Pins 6, 7, 20, 23,	50 mA

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V and ±5V supplies with external LH0033 Buffer Amplifier unless otherwise noted.

INPUTS	
Input Voltage Range, Min.	±2.5V
Input Bias Current	25 μA
Maximum Source Impedance	51 Ohms
Input Impedance	10^6 Ohms
Sample Control Inputs[4]	Differential ECL 10,000 Positive Pulse on Pin 1 and Negative Pulse on Pin 3 gives Sample Mode
OUTPUT[1]	
Output Voltage Range, Min.	±2.5V
Output Current	±10 mA
Output Impedance	6 Ohms
PERFORMANCE	
Accuracy	0.1%
Gain	+0.995
Output Offset Voltage[2], Sample Mode	±100 mV max.
Output Offset Voltage Drift	±100 μV/°C max.
Sample to Hold Offset Error	±100 mV max.
Hold Mode Droop	50 μV/μsec.
Hold Mode Feedthrough	0.02%
DYNAMIC RESPONSE	
Acquisition Time, 5V Step to 0.2%	25 nsec.
Bandwidth, −3 dB, Sample Mode	50 MHz
Slew Rate	200V/μsec.
Aperture Delay Time	6 nsec.
Aperture Uncertainty Time	10 psec.
POWER REQUIREMENTS[3]	
Power Supply Voltage	±15V dc ±0.75V at 60 mA ±5V dc ±0.25V at 70 mA
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Ranges	
SHM-HUMC	0 to +70°C
SHM-HUMM	−55 to +100°C
Storage Temperature Range	−65 to +150°C
Package Type	24 Pin Ceramic
Pins	0.010 x 0.018 inch Kovar
Weight	0.2 ounces (6 grams)

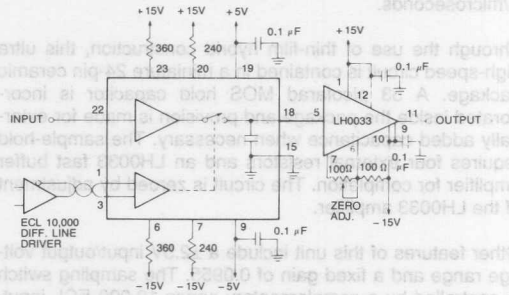
FOOTNOTES:

1. Output is from LH0033 amplifier and is not short circuit proof.
2. Output offset voltage adjustable to zero by LH0033 offset adjustment.
3. ±12V supplies can be used if the 360 ohm resistors at the Bias 1 pins are changed to 240 ohms and the 240 ohm resistors at the Bias 2 pins are changed to 160 ohms.
4. The SHM-HU can be driven by TTL logic input by biasing $\overline{\text{SAMPLE}}$ CONTROL input to +1.2V and driving the SAMPLE CONTROL with a positive pulse for sampling mode.

TECHNICAL NOTES

1. It is recommended that the ±5V supplies of the SHM-HU be bypassed with 0.1 μF ceramic capacitors as close as possible to pins 9 and 19. The ±15V supplies to the LH0033 should be bypassed with the same value capacitors.
2. It is essential that the output lead from pin 18 to pin 5 of the LH0033 be kept as short and direct as possible. Also, the complementary ECL driver should be as close as possible to pins 1 and 3 to minimize lead lengths to these pins.
3. With model SHM-HUMC the LH0033C should be used, and with model SHM-HUMM, model LH0033 should be used.
4. An external hold capacitor may be added from pin 18 to pin 15. This capacitor should be an MOS or polystyrene type. Hold mode Droop and sample-to-hold offset error will decrease proportionately with the size of this capacitor and acquisition time will increase proportionately.

CONNECTION DIAGRAM



ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
SHM-HUMC	0 to +70 °C
SHM-HUMM	-55 to +100 °C
SHM-HUMM-QL	-55 to +100 °C

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SHM-49

High Speed, 0.01% Hybrid Sample/Hold

PRELIMINARY PRODUCT DATA

FEATURES

- **16 MHz small signal bandwidth**
- **Small 8 pin DIP or LCC package**
- **200 nanoseconds maximum acquisition time to 0.01%**
- **100 nanoseconds maximum sample/hold settling time to 0.01%**
- **72 dB feedthrough attenuation**
- **±25 picoseconds aperture uncertainty**
- **413 mW maximum power dissipation**

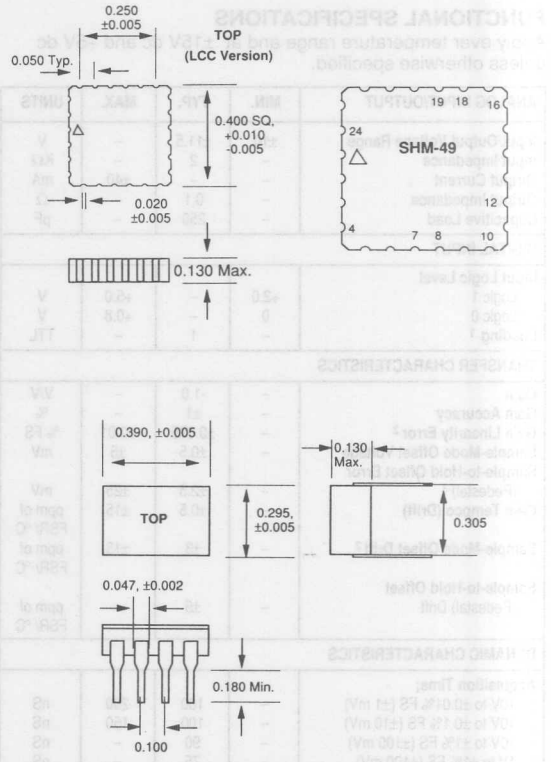
GENERAL DESCRIPTION

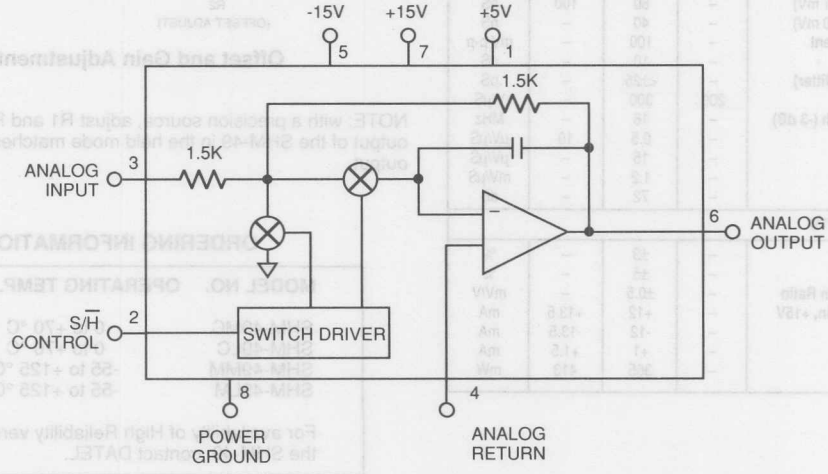
DATEL's SHM-49 is a high-speed, highly accurate sample/hold designed for precision, high-speed analog signal processing applications. Manufactured using modern, high-quality hybrid technology, the SHM-49 features excellent dynamic specifications including a maximum acquisition time of only 200 nanoseconds for a 10V step to 0.01%. Sample-to-hold settling time, to 0.01% accuracy, is 100 nanoseconds maximum with an aperture uncertainty of ±25 picoseconds.

The SHM-49 is a complete sample/hold circuit, containing a precision MOS hold capacitor and a MOSFET switching configuration which results in faster switching and better feedthrough attenuation. Additionally a FET input amplifier design allows faster acquisition and settling times while maintaining a considerably lower droop rate.

DIP	PINOUT	LCC
1	+5V	4
2	S/H	7
3	ANALOG IN	10
4	ANALOG RETURN	12
5	-15V	16
7	+15V	19
8	POWER GROUND	24

MECHANICAL DIMENSIONS





ABSOLUTE MAXIMUM RATINGS

±15V Supply Voltage	±18V
+5V Supply Voltage	-0.5V to +7V
Analog Input	±18V
Digital Input	-0.5V to +5.5V
Output Current	±65 mA

FUNCTIONAL SPECIFICATIONS

Apply ever temperature range and at ±15V dc and +5V dc unless otherwise specified.

ANALOG INPUT/OUTPUT	MIN.	TYP.	MAX.	UNITS
Input/Output Voltage Range	±10	±11.5	–	V
Input Impedance	–	2	–	KΩ
Output Current	–	–	±40	mA
Output Impedance	–	0.1	–	Ω
Capacitive Load	–	250	–	pF
DIGITAL INPUT				
Input Logic Level				
Logic 1	+2.0	–	+5.0	V
Logic 0	0	–	+0.8	V
Loading [1]	–	1	–	TTL
TRANSFER CHARACTERISTICS				
Gain	–	-1.0	–	V/V
Gain Accuracy	–	±1	–	%
Gain Linearity Error [2]	–	±0.005	±0.01	% FS
Sample-Mode Offset Voltage	–	±0.5	±5	mV
Sample-to-Hold Offset Error (Pedestal) [3]	–	±2.5	±25	mV
Gain Tempco (Drift)	–	±0.5	±15	ppm of FSR/ °C
Sample-Mode Offset Drift [2]	–	±3	±15	ppm of FSR/ °C
Sample-to-Hold Offset (Pedestal) Drift	–	±5	–	ppm of FSR/ °C
DYNAMIC CHARACTERISTICS				
Acquisition Time;				
10V to ±0.01% FS (±1 mV)	–	160	200	nS
10V to ±0.1% FS (±10 mV)	–	100	150	nS
10V to ±1% FS (±100 mV)	–	90	–	nS
1V to ±1% FS (±100 mV)	–	75	–	nS
Sample-to-Hold, Settling Time				
10V to ±0.01% FS (±1 mV)	–	60	100	nS
10V to ±0.1% FS (±10 mV)	–	40	–	nS
Sample-to-Hold Transient	–	100	–	mV p-p
Aperture Delay Time	–	10	–	nS
Aperture Uncertainty (Jitter)	–	<±25	–	pS
Output Slew Rate	200	300	–	V/µS
Small Signal Bandwidth (-3 dB)	–	16	–	MHz
Droop; +25 °C	–	0.5	10	µV/µS
+70 °C	–	15	–	µV/µS
+125 °C	–	1.2	–	mV/µS
Feedthrough	–	72	–	dB
POWER REQUIREMENTS				
Voltage Range, ±15V	–	±3	–	%
+5V	–	±5	–	%
Power Supply Rejection Ratio	–	±0.5	–	mV/V
Quiescent Current Drain, +15V	–	+12	+13.5	mA
-15V	–	-12	-13.5	mA
+5V	–	+1	+1.5	mA
Power Consumption	–	365	413	mW

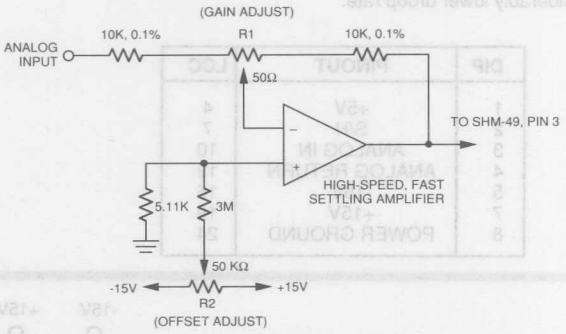
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	
SHM-49MC/LC	0 to +70 °C
SHM-49MM/LM	-55 to +125 °C
Storage Temperature Range	-65 to +150 °C
Package Type, DIP	8 pin ceramic
LCC	24 pin ceramic

Footnotes

1. One TTL load is defined as sinking 40 µA with a logic 1 input and sourcing 1.6mA with a logic 0 input.
2. Full Scale (FS) = 10V. Full Scale Range (FSR) = 20V.
3. Sample-to-Hold offset error (Pedestal) is constant regardless of input/output level.

TECHNICAL NOTES

1. All ground pins should be tied together and connected to system analog ground as close to the package as possible. It is recommended to use a ground plane under the device and solder ground pins directly to it. Care must be taken to insure that no ground potentials can exist between ground pins.
2. External 0.1 µF to 1 µF tantalum bypass capacitors are required in critical applications.
3. A logic 1 on S/$\overline{H}$ puts the unit in the track mode. A logic 0 puts the unit in hold mode.
4. The maximum capacitive load to avoid oscillation is typically 250 pF. Recommended resistive load is 500Ω, although values as low as 250Ω may be used. Acquisition and sample-to-hold settling times are relatively unaffected by resistive loads down to 250Ω and capacitive loads up to 50 pF. However, capacitances will affect both acquisition and settling time.



Offset and Gain Adjustments

NOTE: with a precision source, adjust R1 and R2 so that the output of the SHM-49 in the hold mode matches the source output.

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
SHM-49MC	0 to +70 °C
SHM-49LC	0 to +70 °C
SHM-49MM	-55 to +125 °C
SHM-49LM	-55 to +125 °C

For availability of High Reliability versions of the SHM-49, contact DATEL.

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MSH-840
Quad Simultaneous Sample Hold

ADVANCED PRODUCT DATA

FEATURES

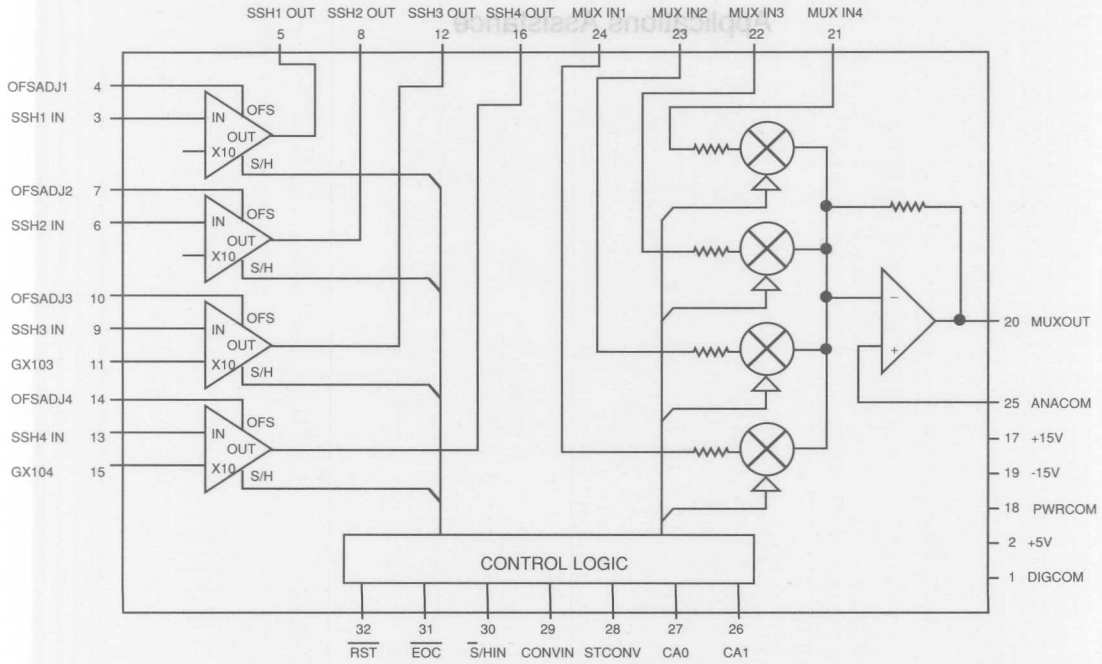
- **4 Simultaneous sample holds**
- **Internal 4-channel multiplexer**
- **750 nSec. Acquisition time, 10V step to 0.01%**
- **2 Channels with optional X10 gain**
- **Control logic for interfacing to A/D's**
- **Low power - 1.5 Watts**
- **Small 32-pin TDIP**
- **-55 °C to +125 °C Versions**

GENERAL DESCRIPTION

The MSH-840 is a quad simultaneous sample-hold featuring an acquisition time of 750 nSec. Control logic is provided for strobing the channels simultaneously and for interfacing to A/D's. A 4-channel multiplexer allows individual S/H outputs to be digitized.

The MSH-840 requires +/-15V and +5V power supplies and dissipates just 1.5 Watts. Packaged in a small 32-pin TDIP, both commercial 0 to +70 °C and military -55 to +125 °C operating temperature range models are offered.

PIN	FUNCTION	PIN	FUNCTION
1	DIGCOM	17	+15V
2	+5V	18	PWRCOM
3	SSH1 IN	19	-15V
4	OFSADJ1	20	MUX OUT
5	SSH1 OUT	21	MUX IN4
6	SSH2 IN	22	MUX IN3
7	OFSADJ2	23	MUX IN2
8	SSH2 OUT	24	MUX IN1
9	SSH3 IN	25	ANACOM
10	OFSADJ3	26	CA1
11	G X10 3	27	CAO
12	SSH3 OUT	28	START CONVERT
13	SSH4 IN	29	CONV IN
14	OFSADJ4	30	S/H IN
15	G X10 4	31	EOC
16	SSH4 OUT	32	RST



Contact DATEL for up-to-date information on products covered by "Advanced" and "Preliminary" product data sheets.

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HYBRID DATA ACQUISITION SYSTEMS

	Model	Resolution (Bits)	Throughput (KHz)	Linearity Error (Max)	Power (Watts Max)	Channels	Case	Page
	HDAS-16	12	50	±3/4 LSB	1.75	16 SE	62-Pin	5-1
	HDAS-8	12	50	±3/4 LSB	1.75	8 DE	62-Pin	5-1
	HDAS-75	12	75	±3/4 LSB	0.7	8 SE	40-Pin DIP	5-15
	HDAS-76	12	75	±3/4 LSB	0.7	4 DE	40-Pin DIP	5-15
	HDAS-534	12	250	±3/4 LSB	3.0	4 DE	40-Pin DIP	5-11
	HDAS-538	12	250	±3/4 LSB	3.0	8 SE	40-PIN DIP	5-11
	HDAS-524	12	400	±3/4 LSB	3.0	4 DE	40-Pin DIP	5-7
	HDAS-528	12	400	±3/4 LSB	3.0	8 SE	40-Pin DIP	5-7
Preliminary	**HDAS-950**	16	100	±1/2 LSB @ 14 BITS	1.4	8 SE	40-Pin DIP	5-19
Preliminary	**HDAS-951**	16	100	±1/2 LSB @ 14 BITS	1.4	4 DE	40-Pin DIP	5-19

Contact DATEL for your
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HDAS-16, HDAS-8

12-Bit Microelectronic Data Acquisition Systems

FEATURES

- **Miniature 63-pin hermetic package**
- **12-Bit resolution, 50 KHz**
- **Full-scale gain range of 50 mV to 10V**
- **Three-state outputs**
- **16 Channels single-ended or 8 channels differential**
- **Auto-sequencing channel addressing**
- **MIL-STD-883 versions**
- **No missing codes**

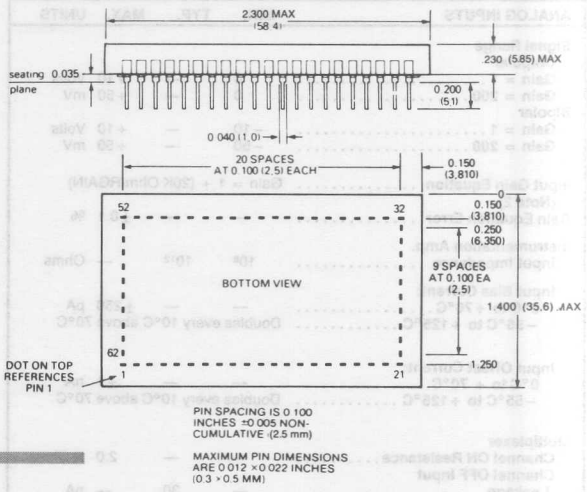
GENERAL DESCRIPTION

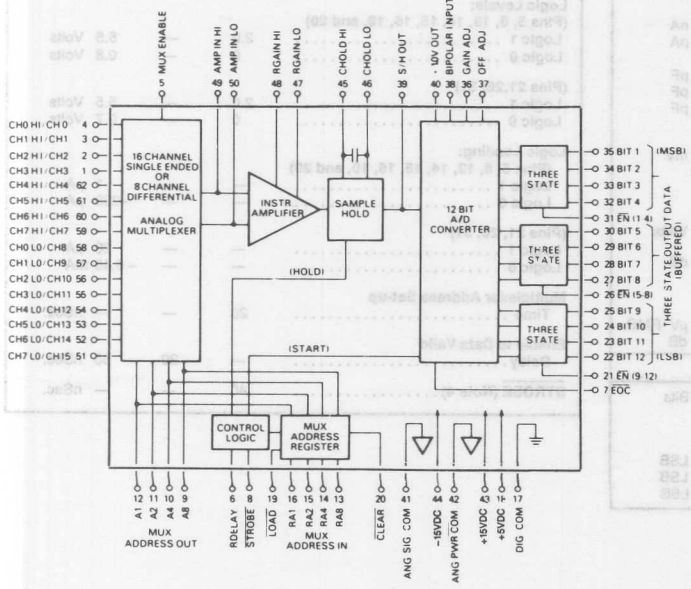
Using thin-and thick-film hybrid technology, DATEL offers complete low-cost data acquisition systems with superior performance and reliability.

The HDAS-8 (with 8 differential input channels), and the HDAS-16 (with 16 single-ended input channels), are complete high performance 12-bit data acquisition systems in 62-pin packages. Each HDAS may expand to 32 single-ended or 16 or more differential channels by adding external multiplexers.

Internal channel address sequencing is automatic after each conversion, or the user may supply external channel addresses.

MECHANICAL DIMENSIONS — INCHES (MM)





Internal HDAS circuitry includes:

- **Analog signal multiplexer**
- **Resistor programmable gain instrumentation amplifier**
- **A sample-and-hold-circuit, complete with MOS hold capacitor**
- **A 10 volt buffered reference**
- **A 12-bit A/D converter with three-state outputs and control logic**

ABSOLUTE MAXIMUM RATINGS			
Parameters	**Min.**	**Max.**	**Units**
+15V Supply (Pin 43)	−0.5	+18	Volts dc
−15V Supply (Pin 44)	+0.5	−18	Volts dc
+5V Supply (Pin 18)	−0.5	+7	Volts dc
Analog Inputs (Note 1)	−35	+35	Volts
Digital Inputs	−0.5	+7	Volts
Thermal Resistance			
Junction-Case		13	°C/Watt
Case-Ambient		17	°C/Watt
Junction-Ambient		30	°C/Watt
Power Dissipation		1.75	Watts
Lead Temp. (10 Sec.)		300	°C

FUNCTIONAL SPECIFICATIONS

The following specifications apply over the operating temperature range and power supply range unless otherwise indicated.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Signal Range				
Unipolar				
Gain = 1	0	—	+10	Volts
Gain = 200	0	—	+50	mV
Bipolar				
Gain = 1	−10	—	+10	Volts
Gain = 200	−50	—	+50	mV
Input Gain Equation (Note 2)	Gain = 1 + (20K Ohm/RGAIN)			
Gain Equation Error	—	—	±0.1	%
Instrumentation Amp.				
Input Impedance	10^8	10^{12}	—	Ohms
Input Bias Current:				
0°C to +70°C	—	—	±250	pA
−55°C to +125°C	Doubles every 10°C above 70°C			
Input Offset Current:				
0°C to +70°C	—	—	±1	nA
−55°C to +125°C	Doubles every 10°C above 70°C			
Multiplexer				
Channel ON Resistance	—	—	2.0	K Ohms
Channel OFF Input Leakage	—	30	—	pA
Channel OFF Output Leakage	—	1.0	—	nA
Channel ON Leakage	—	100	—	pA
Input Capacitance				
HDAS-16, Channel On	—	100	—	pF
HDAS-8, Channel On	—	50	—	pF
+25°C, Channel Off	—	5	—	pF
Input Offset Voltage				
Gain = 1 to 200, +25°C	—	—	±2	mV
−55°C to +125°C	± (30ppm/°C × Gain) ppm/°C (max)		±20	
Common Mode Range	±11	—	—	Volts
CMRR, Gain = 1, at 60 Hz	−70	−82	—	dB
Input Voltage Noise (Referred to Input)				
Gain = 1	—	150	200	µV RMS
Channel Crosstalk	−80	—	—	dB

PERFORMANCE				
Resolution	12	—	—	Bits
Integral Nonlinearity:				
+25°C	—	—	±¾	LSB
0°C to 70°C	—	—	±1	LSB
−55°C to +125°C	—	—	±1	LSB

PERFORMANCE (cont.)	MIN.	TYP.	MAX.	UNITS
Differential Nonlinearity:				
+25°C	—	—	±¾	LSB
0°C to 70°C	—	—	±1	LSB
−55°C to +125°C	—	—	±1	LSB
Differential Nonlinearity Tempco	—	—	±2	ppm/°C
Unipolar Zero Error				
+25°C (Note 3)	—	—	±0.1	%FSR
−55°C to +125°C	—	—	±0.3	%FSR
Unipolar Zero Tempco	—	—	±20	ppm/°C
Bipolar Zero Error				
±25°C (Note 3)	—	—	+0.1	%FSR
−55°C to +125°C	—	—	±0.3	%FSR
Bipolar Zero Tempco	—	—	±35	ppm/°C
Bipolar Offset Error				
+25°C (Note 3)	—	—	0.1	%FSR
−55°C to +125°C	—	—	0.3	%FSR
Bipolar Offset Tempco	—	—	±35	ppm/°C
Gain Error				
+25°C (Note 3)	—	—	±0.2	%FSR
−55°C to +125°C	—	—	±0.3	%FSR
Gain Error Tempco	—	—	±30	ppm/°C
No Missing Codes	Over the operating temperature range			

DYNAMIC CHARACTERISTICS				
Acquisition Time,				
At Gain = 1, +25°C	—	9	10	µSec.
−55°C to +125°C	—	—	15	µSec.
At Gain = 10, +25°C	—	9	—	µSec.
At Gain = 50, +25°C	—	16	—	µSec.
At Gain = 200, +25°C	—	60	—	µSec.
Aperture Delay Time	—	100	500	nSec.
Aperture Uncertainty	—	—	1	nSec.
S/H Droop Rate	—	—	800	mV/Sec.
Feedthrough Accuracy	—	—	±0.01	%
A/D Conversion Time:				
+25°C	—	9	10	µSec.
−55°C to +125°C	—	—	15	µSec.
Throughput Rate				
+25°C	50	55	—	KHz
−55°C to +125°C	33	—	—	KHz

DIGITAL INPUTS				
Logic Levels:				
(Pins 5, 8, 13, 14, 15, 16, 19, and 20)				
Logic 1	2.0	—	5.5	Volts
Logic 0	0	—	0.8	Volts
(Pins 21,26, 31)				
Logic 1	2.0	—	5.5	Volts
Logic 0	0	—	0.7	Volts
Logic Loading:				
(Pins 5, 8, 13, 14, 15, 16, 19, and 20)				
Logic 1	—	—	1	µA
Logic 0	—	—	−280	µA
(Pins 21, 26, 31)				
Logic 1	—	—	20	µA
Logic 0	—	—	−0.40	mA
Multiplexer Address Set-up Time	20	—	—	nSec.
Enable to Data Valid Delay	—	20	30	nSec.
STROBE (Note 4)	40	—	—	nSec.

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OUTPUTS	MIN.	TYP.	MAX.	UNITS
Logic Levels: (Pin 7 & Output Data)				
Logic 1	2.4	—	—	Volts
Logic 0	—	—	0.4	Volts
(Pins 9, 10, 11, and 12)				
Logic 1	4.4	—	—	Volts
Logic 0	—	—	0.1	Volts
Logic Loading:				
Logic 1	—	—	400	μA
Logic 0	—	—	4	mA
Internal Reference:				
Voltage, +25°C	+9.99	+10.00	+10.01	Volts dc
Drift	—	—	±20	ppm/°C
External current	—	—	1	mA
Data Output Coding	Straight binary (unipolar) or offset binary (bipolar)			
POWER REQUIREMENTS				
Power Supply Range:				
+15V dc Supply	+14.5	+15.0	+15.5	Volts dc
−15V dc Supply	−14.5	−15.0	−15.5	Volts dc
+5 dc Supply	+4.75	+5.0	+5.25	Volts dc
Supply Current:				
+15V Supply	—	—	+40	mA
−15V Supply	—	—	−45	mA
+5V Supply	—	—	+95	mA
Power Dissipation	—	1.45	1.75	Watts
PHYSICAL — ENVIRONMENTAL				
Operating Temperature Range:				
MC Models	0	—	+70	deg. C
MM/883B Models	−55	—	+125	deg. C
Storage Temperature Range:	−65	—	+150	deg. C
Weight		1.4(39.7)		oz. (gram)
Package Type	62-pin hermetically sealed Ceramic DIP			
Pin Type	0.010 x 0.018 in. Kovar			

SPECIFICATION NOTES

1. Analog inputs will withstand ±35 volts with power on. If the power is off, the maximum safe input (no damage) is ±20 volts.
2. The gain equation error is guaranteed before external trimming and applies at gains under 50. This error increases at gains over 50.
3. Adjustable to zero.
4. $\overline{\text{STROBE}}$ pulse width must be smaller than $\overline{\text{EOC}}$ period to achieve maximum throughput rate.

TECHNICAL NOTES

1. Input channels are protected to 20 volts beyond the power supplies. All digital output pins have one second short circuit protection; CHOLD has a ten second short circuit protection.
2. To retain high system throughput rate while digitizing low level signals, apply external high-gain amplifiers for each channel. Datel's AM-551 is suggested for such amplifier-per-channel applications.
3. The HDAS devices have self-starting circuits for free-running sequential operation. If, however, in a power-up condition the supply voltage slew rate is less than 3V per microsecond, the free running state might not be initialized. Apply a negative pulse to the $\overline{\text{STROBE}}$, to eliminate this condition.
4. For unipolar operation, connect BIPOLAR INPUT (pin 38) to S/H OUT (pin 39). For bipolar operation, connect BIPOLAR INPUT (pin 38) to +10V REFERENCE OUT (pin 40).
5. RDELAY may be a standard value 5% carbon composition or film type resistor.
6. RGAIN must be very accurate with low temperature coefficients. If necessary, fabricate the gain resistor from a precision metal film type in series with a low value trim resistor or potentiometer. The total resistor temperature coefficient must be no greater than ± 10 ppm/°C.

PIN CONNECTIONS

PIN NO.	HDAS-16	HDAS-8
1	CH3 IN	CH3 HIGH IN
2	CH2 IN	CH2 HIGH IN
3	CH1 IN	CH1 HIGH IN
4	CH0 IN	CH0 HIGH IN
5	MUX ENABLE	*
6	R DELAY	*
7	$\overline{\text{EOC}}$	*
8	STROBE	*
9	A8 (MULTIPLEXER ADDRESS OUT)	*
10	A4	*
11	A2	*
12	A1	*
13	RA8 (MULTIPLEXER ADDRESS IN)	*
14	RA4	*
15	RA2	*
16	RA1	*
17	DIGITAL COMMON	*
18	+5V dc	*
19	$\overline{\text{LOAD ENABLE}}$	*
20	$\overline{\text{CLEAR ENABLE}}$	*
21	$\overline{\text{ENABLE}}$ (Bits 9–12)	*
22	BIT 12 OUT (LSB)	*
23	BIT 11 OUT	*
24	BIT 10 OUT	*
25	BIT 9 OUT	*
26	$\overline{\text{ENABLE}}$ (Bits 5–8)	*
27	BIT 8 OUT	*
28	BIT 7 OUT	*
29	BIT 6 OUT	*
30	BIT 5 OUT	*
31	$\overline{\text{ENABLE}}$ (Bits 1–4)	*
32	BIT 4 OUT	*
33	BIT 3 OUT	*
34	BIT 2 OUT	*
35	BIT 1 OUT (MSB)	*
36	GAIN ADJUST	*
37	OFFSET ADJUST	*
38	BIPOLAR INPUT	*
39	SAMPLE/HOLD OUT	*
40	+10V OUT	*
41	ANALOG SIGNAL COMMON	*
42	ANALOG POWER COMMON	*
43	+15V dc	*
44	−15V dc	*
45	C HOLD HIGH	*
46	C HOLD LOW	*
47	R GAIN LOW	*
48	R GAIN HIGH	*
49	AMP. IN HIGH[1]	*
50	AMP. IN LOW[1]	*
51	CH15 IN	CH7 LOW IN
52	CH14 IN	CH6 LOW IN
53	CH13 IN	CH5 LOW IN
54	CH12 IN	CH4 LOW IN
55	CH11 IN	CH3 LOW IN
56	CH10 IN	CH2 LOW IN
57	CH9 IN	CH1 LOW IN
58	CH8 IN	CH0 LOW IN
59	CH7 IN	CH7 HIGH IN
60	CH6 IN	CH6 HIGH IN
61	CH5 IN	CH5 HIGH IN
62	CH4 IN	CH4 HIGH IN

* Same as HDAS-16

1. Caution: pins 49 and 50 do not have overvoltage protection; therefore, protected multiplexers, such as DATEL's MX-1606 an MX-808 are recommended. See the General Operation description.

Table 1. Description of Pin Functions

FUNCTION	LOGIC STATE	DESCRIPTION
DIGITAL INPUTS		
STROBE	1 to 0	Initiates acquisition and conversion of analog signal
LOAD	0	Random Address Mode Initiated on falling edge of STROBE
	1	Sequential Address Mode
CLEAR	0	Allows next STROBE pulse to reset MULTIPLEXER ADDRESS to CH0 overriding LOAD COMMAND
MULTIPLEXER ENABLE	0	Disables internal MULTIPLEXER
	1	Enables internal MULTIPLEXER
MULTIPLEXER ADDRESS IN		Selects channel for Random Address Mode 8, 4, 2, and 1 natural binary coding
DIGITAL OUTPUTS		
EOC		End of Conversion (STATUS)
	0	Conversion complete
	1	Conversion in process
ENABLE (1–4)	0	Enables three-state outputs bits 1–4
	1	Disables three-state outputs bits 1–4
ENABLE (5–8)	0	Enables three-state outputs bits 5–8
	1	Disables three-state outputs bits 5–8
ENABLE (9–12)	0	Enables three-state outputs bits 9–12
	1	Disables three-state outputs bits 9–12
MULTIPLEXER ADDRESS OUT		Output of MULTIPLEXER Address Register 8, 4, 2, 1 natural binary coding
ANALOG INPUTS		
Channel Inputs		Limit voltage to ±20V beyond power supplies.
Bipolar Input		For unipolar operation, connect to pin 39 (S/H OUT) For biploar operation, connect to pin 40 (+10V OUT)
AMP. IN HIGH AMP. IN LOW		These pins are direct inputs to the instrumentation amplifier for external channel expansion beyond 16SE or 8D channels.
ANALOG OUTPUTS		
S/H OUT		Sample/Hold Output
+10V OUT		Buffered +10V reference output
ADJUSTMENT PINS		
ANALOG SIGNAL COMMON		Low level analog signal return
GAIN ADJUSTMENT		External gain adjustment, see calibration instructions.
OFFSET ADJUSTMENT		External offset adjustment. See calibration instructions.
R GAIN		Optional gain selection point. Factory adjusted for G = 1 when left open.
C HOLD		Optional hold capacitor connection.
R DELAY		Optional acquisition time adjustment when connected to +5V, factory adjusted for 9 μSec. Must be connected to +5V either directly or through a resistor.

7. ANALOG SIGNAL COMMON, POWER COMMON, and DIGITAL COMMON are connected internally. Avoid ground-related problems by connecting the commons to one point . . . the ground plane beneath the converer when the above special grounding considerations do not apply.

8. For HDAS-16, tie pin 50 to a "signal source common" if possible. Otherwise tie pin 50 to pin 41 (ANA SIGN COM).

Table 2. Calibration Table

UNIPOLAR RANGE	ADJUST	INPUT VOLTAGE
0 TO +5V	ZERO	+0.6 mV
	GAIN	+4.9982V
0 TO +10V	ZERO	+1.2 mV
	GAIN	+9.9963V
BIPOLAR RANGE		
±2.5V	OFFSET	−2.4994V
	GAIN	+2.4982V
±5V	OFFSET	−4.9988V
	GAIN	+4.9963V
±10V	OFFSET	−9.9976V
	GAIN	+9.9927V

CALIBRATION PROCEDURES

1. Offset and gain adjustments are made by connecting two 20K trim potentiometers as shown in Figure 1.
2. Connect a precision voltage source to pin 4 (CH0 IN). If the HDAS-8 is used, connect pin 58 (CH0 LOW IN) to analog ground. Ground pin 20 (CLEAR) and momentarily short pin 8 (STROBE). Trigger the A/D by connecting pin 7 (EOC) to pin 8 (STROBE). Select proper value for RGAIN and RDELAY by referring to Table 3.
3. Adjust the precision voltage source to the value shown in Table 2 for the unipolar zero adjustment (ZERO + ½ LSB) or the bipolar offset adjustment (−FS + ½ LSB). Adjust the offset trim potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001.
4. Change the output of the precision voltage source to the value shown in Table 2 for the unipolar or bipolar gain adjustment (+FS − 1½ LSB). Adjust the gain trim potentiometer so that the output flickers equally between 1111 1111 1110 and 1111 1111 1111.

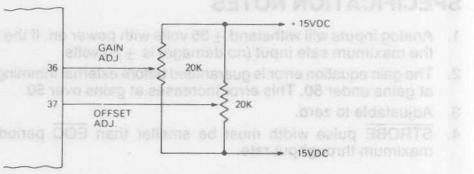


Figure 1. External Adjustment

GENERAL OPERATION

The HDAS devices accept either 16 single-ended or 8 differential input signals. For single-ended circuits, the AMP IN LOW (pin 50) input to the instrumentation amplifier must terminate at ANALOG SIGNAL COMMON (pin 41). For differential circuits, both the HIGH and LOW signal inputs must terminate externally for each channel. Tie unused channels to the ANALOG SIGNAL COMMON (pin 41). To obtain additional channels, connect external multiplexers to the AMP IN HIGH (pin 49) and AMP IN LOW (pin 50). Using this scheme, the HDAS-16 can provide 32 single-ended expansion channels while the HDAS-8 can provide up to 16 differential expansion channels. DATEL multiplexer MX-1606 is recommended.

The acquisition time is the amount of time the multiplexer, instrumentation amplifier, and Sample/Hold require to settle within a specified range of accuracy after STROBE (pin 8) goes low. The acquisition time period can be observed by measuring how long EOC is low after the falling edge of STROBE (see

Table 3. Input Range Parameters (Typical)

INPUT RANGE	GAIN	RGAIN (Ω)	ACQUISITION AND SETTLING DELAY	RDELAY (Ω)	THROUGHPUT	SYSTEM ACCURACY (%of FSR)
±10V	1	OPEN	9 μSec.	0 (SHORT)	55.5 KHz	0.009%
±5V	2	20.0K	9 μSec.	0 (SHORT)	55.5 KHz	0.009%
±2.5V	4	6.667K	9 μSec.	0 (SHORT)	55.5 KHz	0.009%
±1V	10	2.222K	9 μSec.	0 (SHORT)	55.5 KHz	0.009%
±200 mV	50	408.2	16 μSec.	7K	40.0 KHz	0.010%
±100 mV	100	202.0	30 μSec.	21K	25.6 KHz	0.011%
±50 mV	200	100.5	60 μSec.	51K	14.5 KHz	0.016%

NOTES

$$RGAIN\ (\Omega) = \frac{20{,}000}{(GAIN-1)} \qquad RDELAY\ (\Omega) = \frac{(Delay\ \mu sec. \times 1000)}{} - 9000$$

1. For gains between 1 and 10, RDELAY (pin 6) must be shorted to +5V (pin 18).
2. Throughput period equals Acquisition and Settling Delay, plus A/D conversion period (10 microseconds maximum).
3. The analog input range to the A/D converter is 0 to +10V for unipolar signals, and −10.0V to +10.0V for bipolar signals.
4. Full-scale can be accommodated for analog signal ranges of ±50mv to ±10V.

Figure 2). For higher gains increase the acquisition time. Do this by connecting a resistor from RDELAY (pin 6) to +5V (pin 18). An external resistor RGAIN, can be added to increase the gain value. The gain is equal to 1 without an RGAIN resistor. Table 3 refers to the appropriate RDELAY and RGAIN resistors required for various gains.

The HDAS devices enter the hold mode and are ready for conversion as soon as the one-shot (controlling acquisition time) times out. An internal clock is gated ON, and start-convert pulse is sent to the 12-bit A/D converter, driving the EOC output high.

The HDAS devices can be configured for either bipolar or unipolar operation (see Table 2). The conversion is complete within a maximum of 10 microseconds. The $\overline{EOC}$ now returns low, the data is valid and sent to the three-state output buffers. The sample/hold amplifier is now ready to acquire new data. The next falling edge of the STROBE pulse repeats the process for the next conversion.

Table 4. Output Coding

	UNIPOLAR		STRAIGHT BINARY
	0 to +10V	0 to +5V	
+FS − 1 LSB	+9.9976	+4.9988	1111 1111 1111
+½FS	+5.0000	+2.5000	1000 0000 0000
+1 LSB	+0.0024	+0.0012	0000 0000 0001
ZERO	0.0000	0.0000	0000 0000 0000

	BIPOLAR		OFFSET BINARY*
	±10 V	±5V	
+FS − 1 LSB	+9.9951	+4.9976	1111 1111 1111
+½FS	+5.0000	+2.5000	1100 0000 0000
+1 LSB	+0.0049	+0.0024	1000 0000 0001
ZERO	0.0000	0.0000	1000 0000 0000
−FS + 1 LSB	−9.9951	−4.9976	0000 0000 0001
−FS	−10.000	−5.0000	0000 0000 0000

*For 2's complement — add inverter to MSB line.

MULTIPLEXER ADDRESSING

The HDAS devices can be configured in either random or sequential addressing modes. Refer to Table 5 and the subsequent descriptions. The number of channels sequentially addressed can be truncated using the MUX ADDRESS OUT (pins 9, 10, 11 and 12) and appropriate decoding circuitry for the highest channel desired. The decoding circuit can drive the $\overline{CLEAR}$ (pin 20) function low to reset the addressing to channel 0.

RANDOM ADDRESS

Set pin 19 ($\overline{LOAD}$) to logic 0. The next falling edge of $\overline{STROBE}$ will load the MUX CHANNEL ADDRESS present on pin 13 to pin 16. Digital address inputs must be stable 20 nanoseconds before and after falling edge of $\overline{STROBE}$ pulse.

FREE RUNNING SEQUENTIAL ADDRESS

Set pin 19 ($\overline{LOAD}$) and pin 20 ($\overline{CLEAR}$) to logic 1 or leave open. Connect pin 7 ($\overline{EOC}$) to pin 8 ($\overline{STROBE}$). The falling edge of $\overline{EOC}$ will increment channel address. This means that when the $\overline{EOC}$ is low, the digital output data is valid for the previous channel (CHn −1) than the channel indicated on MUX ADDRESS OUTPUT. The HDAS will continually scan all channels.

Example:

CH4 has been addressed and a conversion takes place. The $\overline{EOC}$ goes low. That channel's data becomes valid, but MUX ADDRESS CODE is now CH5.

TRIGGERED SEQUENTIAL ADDRESS

Set pin 19 ($\overline{LOAD}$) and pin 20 ($\overline{CLEAR}$) to logic 1 or leave open. Apply a falling edge trigger pulse to pin 8 ($\overline{STROBE}$). This negative transition causes the contents of the address counter to be incremented by one, followed by an A/D conversion in 9 microseconds.

Table 5. Mux Channel Addressing

← MUX ADDRESS →						
PIN						
9	10	11	12	5		
RA8	RA4	RA2	RA1	MUX ENAB.	ON CHANNEL	
X	X	X	X	0	NONE	
0	0	0	0	1	0	
0	0	0	1	1	1	
0	0	1	0	1	2	
0	0	1	1	1	3	
0	1	0	0	1	4	
0	1	0	1	1	5	
0	1	1	0	1	6	HDAS-8 (3-BIT ADDRESS)
0	1	1	1	1	7	
1	0	0	0	1	8	
1	0	0	1	1	9	
1	0	1	0	1	10	
1	0	1	1	1	11	
1	1	0	0	1	12	
1	1	0	1	1	13	
1	1	1	0	1	14	HDAS-16 (4-BIT ADDRESS)
1	1	1	1	1	15	

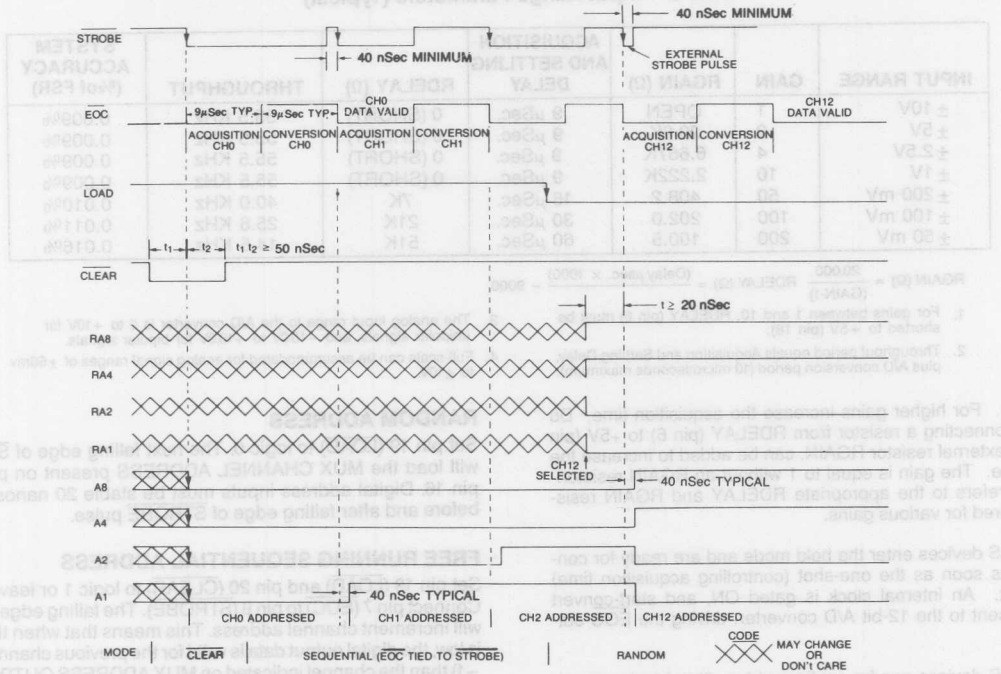


Figure 2. HDAS Timing Diagram

INPUT VOLTAGE PROTECTION

As shown in Figure 3, the multiplexer has reversed biased diodes which protect the input channels from being damaged by over-voltage signals. The HDAS input channels are protected up to 20V beyond the supplies and can be increased by adding series resistors (Ri) to each channel. The input resistor must limit the current flowing through the protection diodes to 10 mA.

The value of Ri for a specific voltage protection range (Vp) can be calculated by the following formula:

$$Vp = (R\ signal + Ri + Ron)\ (10\ mA)$$

where $R_{ON} = 2K$

NOTE: Increased input series resistance will increase multiplexer settling time significantly.

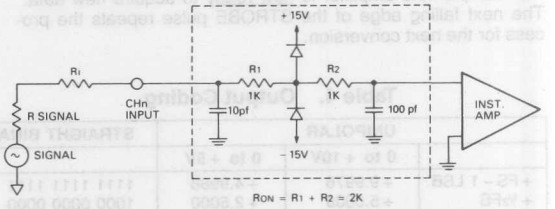


Figure 3. Multiplexer Equivalent Circuit

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE
HDAS-16MC	0°C to + 70°C
HDAS-16MM	−55°C to + 125°C
HDAS-16/883B	−55°C to + 125°C
HDAS-8MC	0°C to + 70°C
HDAS-8MM	−55°C to + 125°C
HDAS-8/883B	−55°C to + 125°C

Receptacle for PC board mounting can be ordered through AMP Incorporated, #3-331272-4 (component lead spring socket) 62 required.

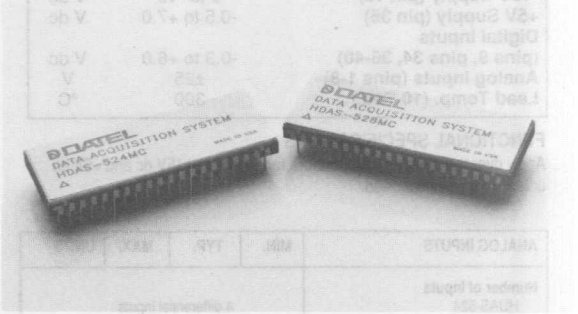
/883B Models are fully compliant to MIL-STD-883.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

HDAS-524,-528
12-Bit, 400 KHz
Data Acquisition Systems

FEATURES

- **12-bit resolution, 400 KHz**
- **8 channels single-ended or 4 channels differential**
- **Miniature 40-pin DDIP**
- **Full scale gain range from 100 mV to 10V**
- **Three-state outputs**
- **No missing codes**



GENERAL DESCRIPTION

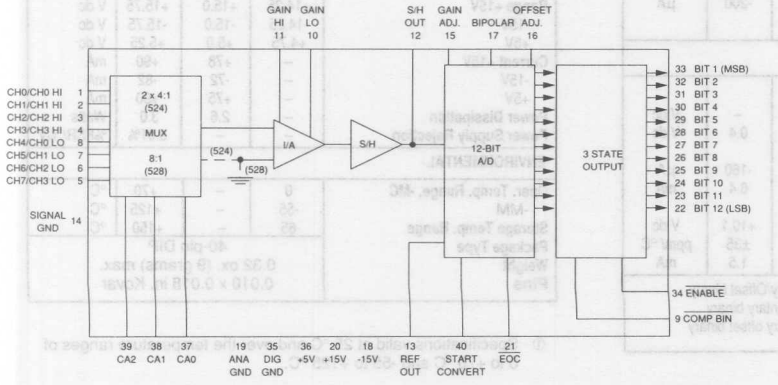
The HDAS-524,-528 are complete data acquisition systems containing an internal multiplexer, instrumentation amplifier, sample-hold, analog-to-digital converter and three-state outputs. Packaged in a miniature 40-pin double-dip package, the HDAS-524/528 has a low power dissipation of 2.6 watts.

The HDAS-524 provides 4 differential inputs and the HDAS-528 provides 8 single-ended inputs. An internal instrumentation amplifier is characterized for gains of 1,2,4,8,10 and 100. The gain range is selectable through an external resistor.

TECHNICAL NOTES

1. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the analog, signal and digital grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies. This prevents contamination of the analog ground by noisy digital ground currents.

2. Double-level multiplexing allows expanding the multiplexer channel capacity of the HDAS-528 from 8 single-ended channels to 128 single-ended channels or the HDAS-524 from 4 differential channels to 32 single-ended channels.



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	CH 0/CH 0 HI	40	START CNVRT
2	CH 1/CH 1 HI	39	CA2
3	CH 2/CH 2 HI	38	CA1
4	CH 3/CH 3 HI	37	CA0
5	CH 7/CH 3 LO	36	+5V
6	CH 6/CH 2 LO	35	DIGITAL GND
7	CH 5/CH 1 LO	34	ENABLE
8	CH 4/CH 0 LO	33	BIT 1 (MSB)
9	COMP BIN	32	BIT 2
10	RGAIN LO	31	BIT 3
11	RGAIN HI	30	BIT 4
12	S/H OUT	29	BIT 5
13	+10V REF OUT	28	BIT 6
14	SIGNAL GND	27	BIT 7
15	GAIN ADJ	26	BIT 8
16	OFFSET ADJUST	25	BIT 9
17	BIPOLAR	24	BIT 10
18	-15V	23	BIT 11
19	ANALOG GND	22	BIT 12
20	+15V	21	EOC

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (pin 20)	0 to +18	V dc
-15V Supply (pin 18)	0 to -18	V dc
+5V Supply (pin 36)	-0.5 to +7.0	V dc
Digital Inputs (pins 9, pins 34, 36-40)	-0.3 to +6.0	V dc
Analog Inputs (pins 1-8)	±25	V
Lead Temp. (10 Sec.)	300	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and +5V dc unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Number of Inputs				
HDAS-524	4 differential inputs			
HDAS-528	8 single-ended inputs			
Input Voltage Ranges				
Gain = 1	0 to +10V , ±10V			
Gain = 100	0 to 100 mV , ±100 mV			
I.A. Gain Ranges	1, 2, 4, 8, 10, 100			
Input Impedance				
CH ON, CH OFF	10^{11}	10^{12}	–	Ohms
Input Capacitance				
(-528) CH ON, CH OFF	–	–	25	pF
(-524) CH ON,CH OFF	–	–	12	pF
Input Bias Current	–	–	200	pA
Input Offset Current	–	–	50	pA
Input Offset Voltage	–	–	±10	mV
Common Mode Volt. Range	±11	–	–	V
CMMR, G=1,@10Hz,				
Vcm=1V p-p	-75	-80	–	dB
Voltage Noise (RMS)				
Gain = 1	–	–	200	µV
Gain = 8	–	–	50	µV
MUX Crosstalk @ 125 KHz	-72	–	–	dB
MUX ON Resistance	–	450	500	Ohms
Bias Current Tempco	Doubles (max.) every 10 °C above 70 °C			
Offset Current Tempco	Doubles (max.) every 10 °C above 70 °C			
Offset Voltage Tempco	(±30 ppm/ °C x gain) ±20 ppm/ °C (max.)			
Input Gain Equation	Rg = 1/[(gain -1)/2K]			
DIGITAL INPUTS				
Logic Levels				
Logic 1	2.0	–	–	V dc
Logic 0	–	–	0.8	V dc
Logic Loading				
Logic 1	–	–	5	µA
Logic 0	–	–	-200	µA
OUTPUTS				
Logic Levels				
Logic 1	2.4	–	–	V dc
Logic 0	–	–	0.4	V dc
Logic Loading				
Logic 1	–	–	-160	µA
Logic 0	–	–	6.4	mA
Internal Reference				
Voltage, +25 °C	+9.9	+10.0	+10.1	V dc
Drift	–	±5	±35	ppm/ °C
External Current	–	–	1.5	mA
Output Coding	Straight binary/Offset binary Complementary binary Complementary offset binary			

PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Resolution	12	–	–	Bits
Integral Nonlinearity,25 °C	–	–	±3/4	LSB
0 to +70 °C	–	–	±3/4	LSB
-55 to +125 °C	–	–	±1.5	LSB
Differential Nonlinearity				
+25 °C	–	–	±3/4	LSB
0 to +70 °C	–	–	±3/4	LSB
-55 to +125 °C	–	–	±1	LSB
F.S. Abs. Accuracy +25 °C	–	±0.13	±0.30	%FSR
0 to +70 °C	–	±0.15	±0.5	%FSR
-55 to +125 °C	–	±0.25	±0.78	%FSR
Unipolar Zero Error,+25 °C	–	±0.074	±0.15	%FSR
Unipolar Zero Tempco	–	±15	±30	ppm/ °C
Bipolar Zero Error, +25 °C	–	±0.074	±0.15	%FSR
Bipolar Zero Tempco	–	±5	±10	ppm/ °C
Bipolar Offset Error,+25 °C	–	±0.1	±0.25	%FSR
Bipolar Offset Tempco	–	±20	±40	ppm/ °C
Gain Error, +25 °C	–	±0.1	±0.25	%FSR
Gain Tempco	–	±20	±40	ppm/ °C
Harmonic Distortion (- FS)				
(DC to 50 KHz,10V pk-pk) ①	-65	-73	–	dB
No Missing Codes	Over operating temperature range			
SIGNAL TIMING				
Enable to Data Val. Delay	–	–	10	nS
MUX Address Set-up Time	400	–	–	nS
Start Convert Pulse Width	50	100	–	nS
Data Valid After				
EOC Signal Goes Low	–	–	20	nS
Conversion Time, +25 °C	–	–	800	nS
0 to +70 °C	–	–	850	nS
-55 to +125 °C	–	–	880	nS
Throughput Rates				
Gain= 1, ①	400	–	–	KHz
Gain = 2, ①	325	–	–	KHz
Gain = 4, ①	275	–	–	KHz
Gain = 8, ①	225	–	–	KHz
Gain = 10, ①	175	–	–	KHz
Gain = 100, ①	40	–	–	KHz
S/H PERFORMANCE				
Acquistion Time				
Full Scale Step to 0.01%	–	500	900	nS
Full Scale Step to 0.1%	–	400	750	nS
Aperture Delay	-50	-20	0	nS
Aperture Uncertainty	–	±100	±150	nS
Slew Rate	70	90	–	V/µS
Hold Mode Settling Time,				
10V to ±0.01%FS	–	100	200	nS
10V to ±0.1%FS	–	75	150	nS
Feedthrough Rejection	-80	-88	–	dB
Droop Rate, ①	–	0.1	100	µV/µS
POWER SUPPLY				
Range +15V	+14.25	+15.0	+15.75	V dc
-15V	-14.25	-15.0	-15.75	V dc
+5V	+4.75	+5.0	+5.25	V dc
Current +15V	–	+78	+90	mA
-15V	–	-72	-82	mA
+5V	–	+75	+90	mA
Power Dissipation	–	2.6	3.0	Watts
Power Supply Rejection	–	–	0.01%	%FSR/ %V
ENVIRONMENTAL				
Oper. Temp. Range, -MC	0	–	+70	°C
-MM	-55	–	+125	°C
Storage Temp. Range	-65	–	+150	°C
Package Type	40-pin DIP			
Weight	0.32 ox. (9 grams) max.			
Pins	0.010 x 0.018 in. Kovar			

① Specifications valid at 25 °C and over the temperature ranges of 0 to +70 °C and -55 to +125 °C.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

TECHNICAL NOTES (CONT.)

3. Obtain straight binary/offset binary output coding by tying $\overline{\text{COMP BIN}}$ (pin 9) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie the $\overline{\text{COMP BIN}}$ pin to ground. The $\overline{\text{COMP BIN}}$ signal is compatible to CMOS/TTL logic levels for those users desiring logic control of this function.

4. To enable the three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 10) to a logic "0" (low). To disable, connect $\overline{\text{ENABLE}}$ (pin 10) to a logic "1" (high).

HDAS-524/528 OPERATION

The HDAS devices accept either 8 single-ended or 4 differential input signals. Tie unused channels to SIGNAL GROUND, pin 14.

Channel selection is accomplished using the multiplexer address pins shown in Table 1. Obtain additional channels by connecting external multiplexers.

The acquisition time is the amount of time the multiplexer, instrumentation amplifier and sample-hold require to settle within a specified range of accuracy. The acquisition time can be measured by how long $\overline{\text{EOC}}$ is low before the rising edge of the START CONVERT pulse for continuous operation. Higher gains require the use of the RGAIN resistor to increase the acquisition time. The gain is equal to 1 without an RGAIN resistor. Table 2 refers to the appropriate RGAIN resistors for various throughputs.

The HDAS devices enter the hold mode and are ready for conversion upon the start convert going high. The conversion is complete within a maximum of 800 nsec (+25°C). $\overline{\text{EOC}}$ returns low, the data is valid and sent to the three-state output buffers. The sample/hold is now ready to acquire new data.

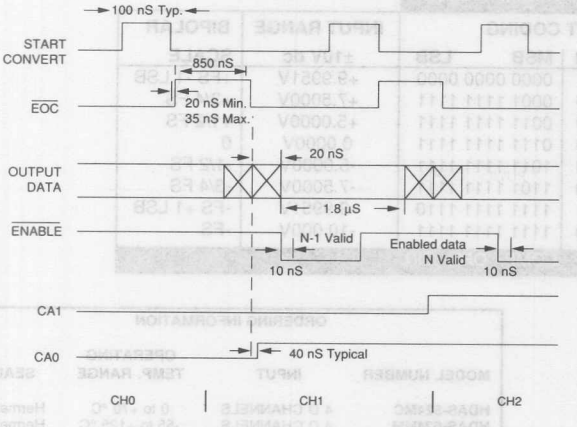


Figure 1. HDAS-524/528 Timing Diagram

NOTES:

1. A START CONVERT pulse greater than 150 nS will slow the throughput.
2. Retriggering START CONVERT before EOC goes low will not start a new conversion.
3. Times shown apply over the full operating temperature range.

Table 1. MUX Channel Addressing

MUX ADDRESS PINS 39 CA2	38 CA1	37 CA0	CHANNEL	
0	0	0	0	
0	0	1	1	HDAS-524
0	1	0	2	(2-BIT ADDRESS)
0	1	1	3	
1	0	0	4	
1	0	1	5	HDAS-528
1	1	0	6	(3-BIT ADDRESS)
1	1	1	7	

Table 2. Input Range Parameters

INPUT RANGE	GAIN	RGAIN ( )	THROUGHPUT
0 to +10V	1	OPEN	400 KHz
0 to +5V	2	2K	325 KHz
0 to +2.5V	4	665 Ω	275 KHz
0 to +1.25V	8	287 Ω	225 KHz
0 to +1.0V	10	221 Ω	175 KHz
0 to +100mV	100	20 Ω	40 KHz
±10V	1	OPEN	400 KHz
±5V	2	2K	325 KHz
±2.5V	4	665 Ω	275 KHz
±1.25V	8	287 Ω	225 KHz
±1.0V	10	221 Ω	175 KHz
±100mV	100	20 Ω	40 KHz

Note 1. $\text{Rgain} = \dfrac{\left[\dfrac{1}{(\text{gain} - 1)}\right]}{2\text{K}}$

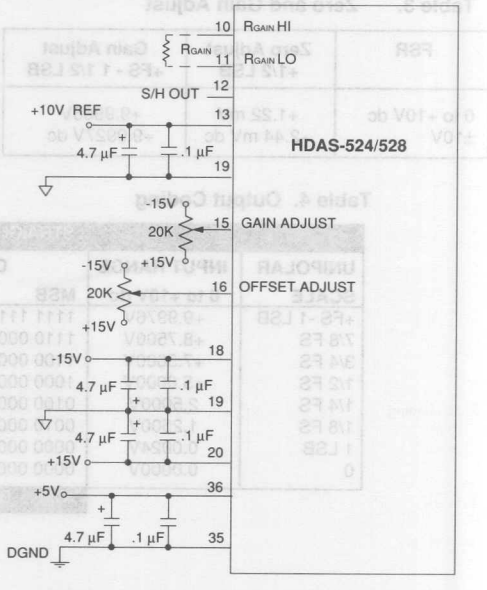
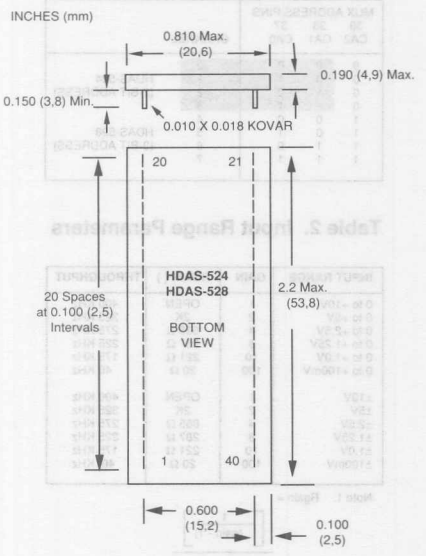


Figure 2. Typical Connection Diagram

NOTES:

1. For unipolar operation, connect pin 12 to pin 17.
2. For bipolar operation, connect pin 13 to pin 17.
3. Position RGAIN as close as possible to pins 10 and 11. Use RN55C, 1% resistors.
4. If gain and offset adjusts are not used connect pin 15 to ground and leave pin 16 open.

MECHANICAL DIMENSIONS



CALIBRATION PROCEDURE

1. Connect the converter per Figure 2 and Tables 2 and 3 for the appropriate full-scale range (FSR). Apply a pulse of 100 nanoseconds (typical) to the START CONVERT input (pin 40) at a rate of 100 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments

Apply a precision voltage reference source between the analog input and signal ground (pin 14). Adjust the output of the reference source per Table 3. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with the COMP BIN (pin 9) tied high (straight binary) or between 1111 1111 1111 and 1111 1111 1110 with the COMP BIN (pin 9) tied low (complementary binary).

For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with COMP BIN (pin 9) tied high (offset binary) or between 0111 1111 1111 and 0111 1111 1110 with COMP BIN (pin 9) tied low (complementary offset binary).

3. Full-Scale Adjustment

Set the output of the voltage reference used in step 2 to the value shown in Table 3. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 or 0000 0000 0001 and 0000 0000 0000 for complementary coding.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 4.

Table 3. Zero and Gain Adjust

FSR	Zero Adjust +1/2 LSB	Gain Adjust +FS - 1 1/2 LSB
0 to +10V dc ±10V	+1.22 mV +2.44 mV dc	+9.9963V +9.9927V dc

Table 4. Output Coding

		STRAIGHT BIN. COMP. BINARY			
UNIPOLAR SCALE	INPUT RANGE 0 to +10V dc	OUTPUT CODING MSB LSB	MSB LSB	INPUT RANGE ±10V dc	BIPOLAR SCALE
+FS -1 LSB	+9.9976V	1111 1111 1111	0000 0000 0000	+9.9951V	+FS -1 LSB
7/8 FS	+8.7500V	1110 0000 0000	0001 1111 1111	+7.5000V	+3/4 FS
3/4 FS	+7.5000V	1100 0000 0000	0011 1111 1111	+5.0000V	+1/2 FS
1/2 FS	+5.0000V	1000 0000 0000	0111 1111 1111	0.0000V	0
1/4 FS	2.5000V	0100 0000 0000	1011 1111 1111	-5.0000V	-1/2 FS
1/8 FS	1.2500V	0010 0000 0000	1101 1111 1111	-7.5000V	-3/4 FS
1 LSB	0.0024V	0000 0000 0001	1111 1111 1110	-9.9951V	-FS +1 LSB
0	0.0000V	0000 0000 0000	1111 1111 1111	-10.000V	-FS
		OFF. BINARY	COMP. OFF. BIN.		

ORDERING INFORMATION

MODEL NUMBER	INPUT	OPERATING TEMP. RANGE	SEAL
HDAS-524MC	4 D CHANNELS	0 to +70 °C	Hermetic
HDAS-524MM	4 D CHANNELS	-55 to +125 °C	Hermetic
HDAS-528MC	8 SE CHANNELS	0 to +70 °C	Hermetic
HDAS-528MM	8 SE CHANNELS	-55 to +125 °C	Hermetic

Receptacle for PC board mounting can be ordered through AMP Inc.,Part # 3-331272-8 (Component Lead Socket), 40 required.

For availability of MIL-STD-883B versions of the HDAS-524 & HDAS-528, contact DATEL.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

HDAS-534,-538
12-Bit, 250 KHz Data Acquisition Systems

FEATURES

- **12-bit resolution, 250 KHz**
- **8 channels single-ended or 4 channels differential**
- **Miniature 40-pin DDIP**
- **Full scale gain range from 100 mV to 10V**
- **Three-state outputs**
- **No missing codes**

GENERAL DESCRIPTION

The HDAS-534/538 are complete data acquisition systems containing an internal multiplexer, instrumentation amplifier, sample-hold, analog-to-digital converter and three-state outputs. Packaged in a miniature 40-pin double-dip package, the HDAS-534/538 provides 250 KHz throughput with a low power dissipation of 2.6 Watts.

The HDAS-534 provides 4 differential inputs and the HDAS-538 provides 8 single-ended inputs. An internal instrumentation amplifier is characterized for gains of 1,2,4,8,10 and 100. The gain range is selectable through an external resistor.

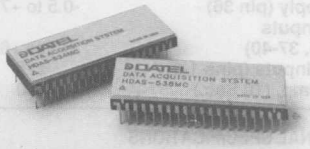
TECHNICAL NOTES

1. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the analog, signal and digital grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

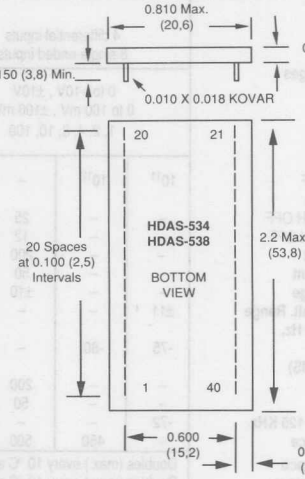
2. Double-level multiplexing allows expanding the multiplexer channel capacity of the HDAS-538 from 8 single-ended channels to 128 single-ended channels or the HDAS-534 from 4 differential channels to 32 single-ended channels.

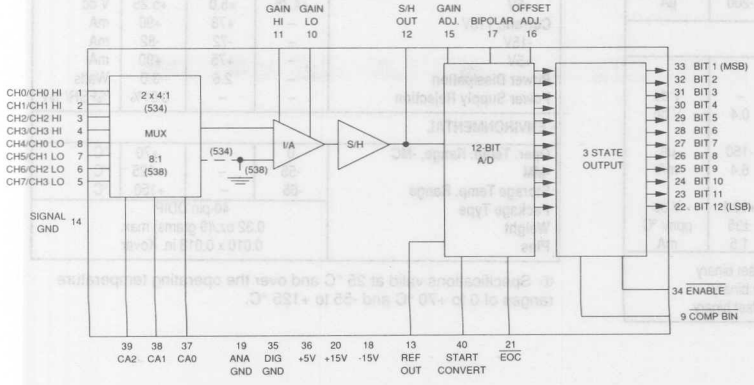
3. Obtain straight binary/offset binary output coding by tying COMP BIN (pin 9) to +5V dc or leaving it open. The device has an internal pull-up resistor on this pin. To obtain complementary binary or complementary offset binary output coding, tie pin 9 to ground. Pin 9 signal is compatible to CMOS/TTL logic levels for logic control of this function.

4. To enable the three-state outputs, connect $\overline{\text{ENABLE}}$ (pin 10) to a logic "0" (low). To disable, connect pin 10 to a logic "1" (high).



MECHANICAL DIMENSIONS INCHES (mm)





INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	CH 0/CH 0 HI	40	START CNVRT
2	CH 1/CH 1 HI	39	CA2
3	CH 2/CH 2 HI	38	CA1
4	CH 3/CH 3 HI	37	CA0
5	CH 7/CH 3 LO	36	+5V
6	CH 6/CH 2 LO	35	DIGITAL GND
7	CH 5/CH 1 LO	34	$\overline{\text{ENABLE}}$
8	CH 4/CH 0 LO	33	BIT 1 (MSB)
9	COMP BIN	32	BIT 2
10	RGAIN LO	31	BIT 3
11	RGAIN HI	30	BIT 4
12	S/H OUT	29	BIT 5
13	+10V REF OUT	28	BIT 6
14	SIGNAL GND	27	BIT 7
15	GAIN ADJ	26	BIT 8
16	OFFSET ADJUST	25	BIT 9
17	BIPOLAR	24	BIT 10
18	-15V	23	BIT 11
19	ANALOG GND	22	BIT 12 (LSB)
20	+15V	21	$\overline{\text{EOC}}$

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (pin 20)	0 to +18	V dc
-15V Supply (pin 18)	0 to -18	V dc
+5V Supply (pin 36)	-0.5 to +7.0	V dc
Digital Inputs (pins 34, 37-40)	-0.3 to +6.0	V dc
Analog Inputs (pins 1-8)	±25	V
Lead Temp. (10 Sec.)	300	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and +5V dc unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Number of Inputs				
HDAS-534	4 differential inputs			
HDAS-538	8 single-ended inputs			
Input Voltage Ranges				
Gain = 1	0 to +10V , ±10V			
Gain = 100	0 to 100 mV , ±100 mV			
I.A. Gain Ranges	1, 2, 4, 8, 10, 100			
Input Impedance				
CH ON, CH OFF	10^{11}	10^{12}	–	Ohms
Input Capacitance				
(534) CH ON, CH OFF	–	–	25	pF
(538) CH ON,CH OFF	–	–	12	pF
Input Bias Current	–	–	200	pA
Input Offset Current	–	–	50	pA
Input Offset Voltage	–	–	±10	mV
Common Mode Volt. Range	±11	–	–	V
CMMR, G=1 ,@ 10 Hz, Vcm=1V p-p	-75	-80	–	dB
Voltage Noise (RMS)				
Gain = 1	–	–	200	µV
Gain = 8	–	–	50	µV
MUX Crosstalk @ 125 KHz	-72	–	–	dB
MUX ON Resistance	–	450	500	Ohms
Bias Current Tempco	Doubles (max.) every 10 °C above 70 °C			
Offset Current Tempco	Doubles (max.) every 10 °C above 70 °C			
Offset Voltage Tempco	(±30 ppm/ °C x gain) ±20 ppm/ °C (max.)			
Input Gain Equation	Rg = 1/[(gain -1)/2K]			
DIGITAL INPUTS				
Logic Levels				
Logic 1	2.0	–	–	V dc
Logic 0	–	–	0.8	V dc
Logic Loading				
Logic 1	–	–	5	µA
Logic 0	–	–	-200	µA
OUTPUTS				
Logic Levels				
Logic 1	2.4	–	–	V dc
Logic 0	–	–	0.4	V dc
Logic Loading				
Logic 1	–	–	-160	µA
Logic 0	–	–	6.4	mA
Internal Reference				
Voltage, +25 °C	+9.9	+10.0	+10.1	V dc
Drift	–	±5	±35	ppm/ °C
External Current	–	–	1.5	mA
Output Coding	Straight binary/Offset binary Complementary binary Complementary offset binary			

PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Resolution	12	–	–	Bits
Integral Nonlinearity,25 °C	–	–	±3/4	LSB
0 to +70 °C	–	–	±3/4	LSB
-55 to +125 °C	–	–	±1.5	LSB
Differential Nonlinearity, +25 °C	–	–	±3/4	LSB
0 to +70 °C	–	–	±3/4	LSB
-55 to +125 °C	–	–	±1	LSB
F.S. Abs. Accuracy +25 °C	–	±0.13	±0.30	%FSR
0 to +70 °C	–	±0.15	±0.5	%FSR
-55 to +125 °C	–	±0.25	±0.78	%FSR
Unipolar Zero Error,+25 °C	–	±0.074	±0.15	%FSR
Unipolar Zero Tempco	–	±15	±30	ppm/ °C
Bipolar Zero Error, +25 °C	–	±0.074	±0.15	%FSR
Bipolar Zero Tempco	–	±5	±10	ppm/ °C
Bipolar Offset Error,+25 °C	–	±0.1	±0.25	%FSR
Bipolar Offset Tempco	–	±20	±40	ppm/ °C
Gain Error, +25 °C	–	±0.1	±0.25	%FSR
Gain Tempco	–	±20	±40	ppm/ °C
Harmonic Distortion (- FS) (DC to 50 KHz, 10V pk-pk)①	-65	-73	–	dB
No Missing Codes	Over operating temperature range			
SIGNAL TIMING				
Enable to Data Val. Delay	–	–	10	nS
MUX Address Set-up Time	400	–	–	nS
Start Convert Pulse Width	125	150	175	nS
Data Valid Before $\overline{EOC}$ Signal Goes Low	–	–	20	nS
Conversion Time, +25 °C	–	–	1000	nS
0 to +70 °C, -55 to +125 °C	–	–	1100	nS
Throughput Rates				
Gain= 1, ①	250	–	–	KHz
Gain = 2, ①	150	–	–	KHz
Gain = 4, ①	125	–	–	KHz
Gain = 8, ①	100	–	–	KHz
Gain = 10, ①	90	–	–	KHz
Gain = 100, ①	30	–	–	KHz
S/H PERFORMANCE				
Acquistion Time				
Full Scale Step to 0.01%	–	500	900	nS
Full Scale Step to 0.1%	–	400	750	nS
Aperture Delay	-50	-20	0	nS
Aperture Uncertainty	–	±100	±150	pS
Slew Rate	70	90	–	V/µS
Hold Mode Settling Time,				
10V to ±0.01%FS	–	100	200	nS
10V to ±0.1%FS	–	75	150	nS
Feedthrough Rejection	-80	-88	–	dB
Droop Rate, ①	–	0.1	100	µV/µS
POWER SUPPLY				
Range, +15V	+14.25	+15.0	+15.75	V dc
-15V	-14.25	-15.0	-15.75	V dc
+5V	+4.75	+5.0	+5.25	V dc
Current, +15V	–	+78	+90	mA
-15V	–	-72	-82	mA
+5V	–	+75	+90	mA
Power Dissipation	–	2.6	3.0	Watts
Power Supply Rejection	–	–	0.01%	%FSR/ %V
ENVIRONMENTAL				
Oper. Temp. Range, -MC	0	–	+70	°C
-MM	-55	–	+125	°C
Storage Temp. Range	-65	–	+150	°C
Package Type	40-pin DDIP			
Weight	0.32 oz./(9 grams) max.			
Pins	0.010 x 0.018 in. Kovar			

① Specifications valid at 25 °C and over the operating temperature ranges of 0 to +70 °C and -55 to +125 °C.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

HDAS-534/538 OPERATION

The HDAS devices accept either 8 single-ended or 4 differential input signals. Tie unused channels to SIGNAL GROUND, pin 14.

Channel selection is accomplished using the multiplexer address pins shown in Table 1. Obtain additional channels by connecting external multiplexers.

The acquisition time is the amount of time the multiplexer, instrumentation amplifier and sample-hold require to settle within a specified range of accuracy.

The acquisition time can be measured by how long $\overline{EOC}$ is low before the rising edge of the START CONVERT pulse for continuous operation. Higher gains require the use of the RGAIN resistor to increase the acquisition time. The gain is equal to 1 without an RGAIN resistor. Table 2 refers to the appropriate RGAIN resistors for various throughputs.

The HDAS devices enter the hold mode and are ready for conversion upon the start convert going high. The conversion is complete within a maximum of 1 µsec (+25°C). $\overline{EOC}$ returns low, the data is valid and sent to the three-state output buffers. The sample/hold is now ready to acquire new data.

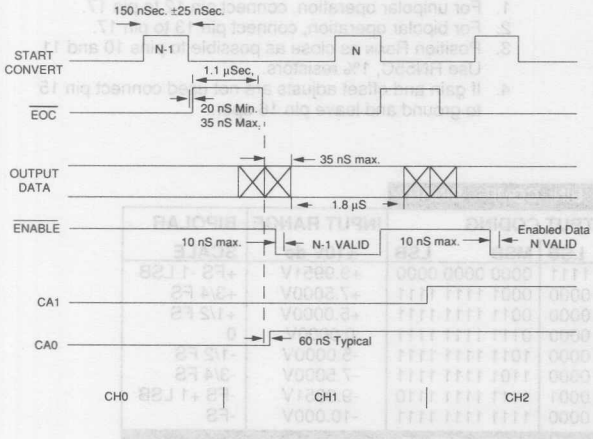


Figure 1. HDAS-534/538 Timing Diagram

Table 1. MUX Channel Addressing

MUX ADDRESS PINS 39 CA2	38 CA1	37 CA0	CHANNEL	
0	0	0	0	
0	0	1	1	HDAS-534
0	1	0	2	(2-BIT ADDRESS)
0	1	1	3	
1	0	0	4	
1	0	1	5	HDAS-538
1	1	0	6	(3-BIT ADDRESS)
1	1	1	7	

Table 2. Input Range Parameters

INPUT RANGE	GAIN	RGAIN ( )	THROUGHPUT
0 to +10V	1	OPEN	250 KHz
0 to +5V	2	2K	150 KHz
0 to +2.5V	4	665 Ω	125 KHz
0 to +1.25V	8	287 Ω	100 KHz
0 to +1.0V	10	221 Ω	90 KHz
0 to +100mV	100	20 Ω	30 KHz
±10V	1	OPEN	250 KHz
±5V	2	2K	150 KHz
±2.5V	4	665 Ω	125 KHz
±1.25V	8	287 Ω	100 KHz
±1.0V	10	221 Ω	90 KHz
±100mV	100	20 Ω	30 KHz

$$\left[\frac{1}{\frac{(\text{gain} - 1)}{2K}}\right]$$

Notes

1. A START CONVERT pulse greater than 175 nanoseconds will slow the throughput.
2. Retriggering START CONVERT before EOC goes low will not start a new conversion.
3. Times shown apply over the full operating temperature range.

Table 3. Zero and Gain Adjust

FSR	Zero Adjust +1/2 LSB	Gain Adjust +FS - 1 1/2 LSB
0 to +10V dc	+1.22mV	+9.9963V dc
±10V dc	+2.44 mV dc	+9.9927V dc

CALIBRATION PROCEDURE

1. Connect the converter per Figure 2 and Table 2 for the appropriate full-scale range (FSR). Apply a pulse of 150 nSec (typical) to the START CONVERT input (pin 40) at a rate of 75 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments

Apply a precision voltage reference source between the analog input and signal ground (pin 14). Adjust the output of the reference source per Table 3. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 with $\overline{\text{COMP BIN}}$ (pin 9) tied high (straight binary) or between 1111 1111 1111 and 1111 1111 1110 with pin 9 tied low (complementary binary).

For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001 with pin 9 tied high (offset binary) or between 0111 1111 1111 and 0111 1111 1110 with pin 9 tied low (complementary offset binary).

3. Full-Scale Adjustment

Set the output of the voltage reference used in step 2 to the value shown in Table 3. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 for pin 9 tied high and 0000 0000 0001 and 0000 0000 0000 for pin 9 tied low.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 4.

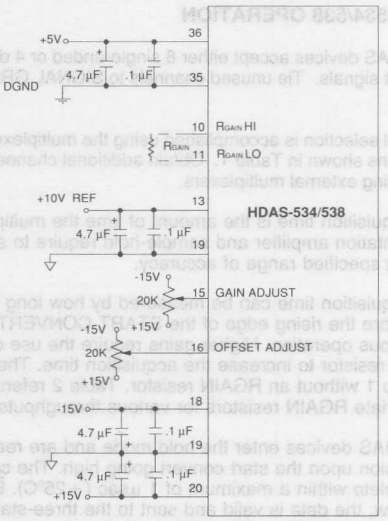


Figure 2. Typical Connection Diagram

NOTES:

1. For unipolar operation, connect pin 12 to pin 17.
2. For bipolar operation, connect pin 13 to pin 17.
3. Position RGAIN as close as possible to pins 10 and 11. Use RN55C, 1% resistors.
4. If gain and offset adjusts are not used connect pin 15 to ground and leave pin 16 open.

Table 4. Output Coding

		STRAIGHT BIN. COMP. BINARY			
UNIPOLAR	INPUT RANGES, V dc	OUTPUT CODING		INPUT RANGE	BIPOLAR
SCALE	0 to +10V	MSB LSB	MSB LSB	±10V dc	SCALE
+FS -1 LSB	+9.9976V	1111 1111 1111	0000 0000 0000	+9.9951V	+FS -1 LSB
7/8 FS	+8.7500V	1110 0000 0000	0001 1111 1111	+7.5000V	+3/4 FS
3/4 FS	+7.5000V	1100 0000 0000	0011 1111 1111	+5.0000V	+1/2 FS
1/2 FS	+5.0000V	1000 0000 0000	0111 1111 1111	0.0000V	0
1/4 FS	+2.5000V	0100 0000 0000	1011 1111 1111	-5.0000V	-1/2 FS
1/8 FS	+1.2500V	0010 0000 0000	1101 1111 1111	-7.5000V	-3/4 FS
1 LSB	+0.0024V	0000 0000 0001	1111 1111 1110	-9.9951V	-FS +1 LSB
0	0.0000V	0000 0000 0000	1111 1111 1111	-10.000V	-FS
		OFF. BINARY	COMP. OFF. BIN.		

ORDERING INFORMATION

MODEL NO.	INPUT	OPER. TEMP. RANGE	SEAL
HDAS-534MC	4 D Channels	0 to +70 °C	Hermetic
HDAS-534MM	4 D Channels	-55 to +125°C	Hermetic
HDAS-538MC	8 SE Channels	0 to +70° C	Hermetic
HDAS-538MM	8 SE Channels	-55 to +125 °C	Hermetic

Receptacle for PC board mounting can be ordered through AMP Inc.,Part # 3-331272-8 (Component Lead Socket), 40 required.

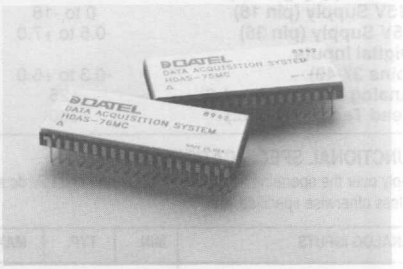
For availability of MIL-STD-883B versions, contact DATEL.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

HDAS-75,-76
12-Bit, 75 KHz
Data Acquisition Systems

FEATURES

- **12-Bit resolution, 75 KHz**
- **8 Channels single-ended or 4 channels differential**
- **Miniature 40-pin DDIP**
- **Full-scale gain range from 100 mV to 10V**
- **High impedance output state**
- **No missing codes**



GENERAL DESCRIPTION

The HDAS-75,-76 are complete data acquisition systems containing an internal multiplexer, instrumentation amplifier, sample-hold, analog-to-digital converter and three-state outputs. Packaged in a miniature 40-pin double-dip package, the HDAS-75/76 has a low power dissipation of 500 milliwatts.

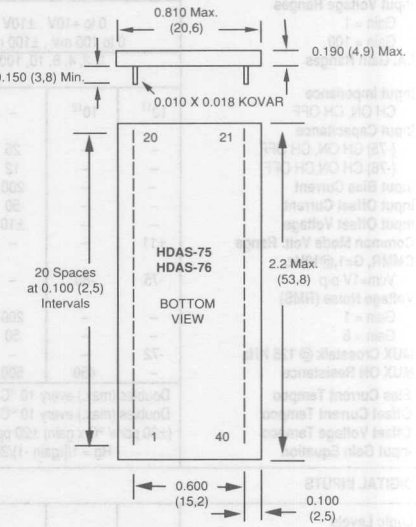
The HDAS-76 provides 4 differential inputs and the HDAS-75 provides 8 single-ended inputs. An internal instrumentation amplifier is characterized for gains of 1,2,4,8,10 and 100. The gain range is selectable through an external resistor.

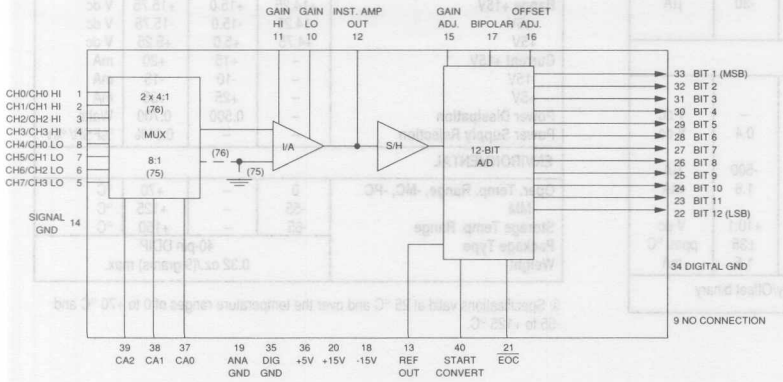
TECHNICAL NOTES

1. Rated performance requires using good high-frequency circuit board layout techniques. The analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the analog, signal and digital grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

2. Double-level multiplexing allows expanding the multiplexer channel capacity of the HDAS-75 from 8 single-ended channels to 128 single-ended channels or the HDAS-76 from 4 differential channels to 32 single-ended channels.

MECHANICAL DIMENSIONS
INCHES (MM)





INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	CH 0/CH 0 HI	40	START CNVRT
2	CH 1/CH 1 HI	39	CA2
3	CH 2/CH 2 HI	38	CA1
4	CH 3/CH 3 HI	37	CA0
5	CH 7/CH 3 LO	36	+5V
6	CH 6/CH 2 LO	35	DIGITAL GND
7	CH 5/CH 1 LO	34	DIGITAL GND
8	CH 4/CH 0 LO	33	BIT 1 (MSB)
9	NO CONNECTION	32	BIT 2
10	RGAIN LO	31	BIT 3
11	RGAIN HI	30	BIT 4
12	INST. AMP OUT	29	BIT 5
13	+10V REF OUT	28	BIT 6
14	SIGNAL GND	27	BIT 7
15	GAIN ADJ	26	BIT 8
16	OFFSET ADJUST	25	BIT 9
17	BIPOLAR	24	BIT 10
18	-15V	23	BIT 11
19	ANALOG GND	22	BIT 12 (LSB)
20	+15V	21	EOC

+15V Supply (pin 20)	0 to +18	V dc
-15V Supply (pin 18)	0 to -18	V dc
+5V Supply (pin 36)	-0.5 to +7.0	V dc
Digital Inputs (pins 37-40)	-0.3 to +6.0	V dc
Analog Inputs (pins 1-8)	±25	V
Lead Temp. (10 Sec.)	300	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and +5V dc unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Number of Inputs				
HDAS-76	4 differential inputs			
HDAS--75	8 single-ended inputs			
Input Voltage Ranges				
Gain = 1	0 to +10V , ±10V			
Gain = 100	0 to 100 mV , ±100 mV			
I.A. Gain Ranges	1, 2, 4, 8, 10, 100			
Input Impedance				
CH ON, CH OFF	10^{11}	10^{12}	–	Ohms
Input Capacitance				
(-75) CH ON, CH OFF	–	–	25	pF
(-76) CH ON,CH OFF	–	–	12	pF
Input Bias Current	–	–	200	pA
Input Offset Current	–	–	50	pA
Input Offset Voltage	–	–	±10	mV
Common Mode Volt. Range	±11	–	–	V
CMMR, G=1,@10Hz, Vcm=1V p-p	-75	-80	–	dB
Voltage Noise (RMS)				
Gain = 1	–	–	200	µV
Gain = 8	–	–	50	µV
MUX Crosstalk @ 125 KHz	-72	–	–	dB
MUX ON Resistance	–	450	500	Ohms
Bias Current Tempco	Doubles (max.) every 10 °C above 70 °C			
Offset Current Tempco	Doubles (max.) every 10 °C above 70 °C			
Offset Voltage Tempco	(±30 ppm/ °C x gain) ±20 ppm/ °C (max.)			
Input Gain Equation	Rg = 1/[(gain -1)/2K]			
DIGITAL INPUTS				
Logic Levels				
Logic 1	2.4	–	–	V dc
Logic 0	–	–	0.8	V dc
Logic Loading				
Logic 1	–	–	+30	µA
Logic 0	–	–	-30	µA
OUTPUTS				
Logic Levels				
Logic 1	2.4	–	–	V dc
Logic 0	–	–	0.4	V dc
Logic Loading				
Logic 1	–	–	-500	µA
Logic 0	–	–	1.6	mA
Internal Reference				
Voltage, +25 °C	+9.9	+10.0	+10.1	V dc
Drift	–	±5	±35	ppm/ °C
External Current	–	–	1.5	mA
Output Coding	Straight binary/Offset binary			

0 to +70 °C	–	–	±3/4	LSB
-55 to +125 °C	–	–	±1.5	LSB
Differential Nonlinearity				
+25 °C	–	–	±3/4	LSB
0 to +70 °C	–	–	±3/4	LSB
-55 to +125 °C	–	–	±1	LSB
F.S. Abs. Accuracy +25 °C	–	±0.13	±0.30	%FSR
0 to +70 °C	–	±0.15	±0.5	%FSR
-55 to +125 °C	–	±0.25	±0.78	%FSR
Unipolar Zero Error,+25 °C	–	±0.074	±0.15	%FSR
Unipolar Zero Tempco	–	±15	±30	ppm/ °C
Bipolar Zero Error, +25 °C	–	±0.074	±0.15	%FSR
Bipolar Zero Tempco	–	±5	±10	ppm/ °C
Bipolar Offset Error,+25 °C	–	±0.1	±0.25	%FSR
Bipolar Offset Tempco	–	±20	±40	ppm/ °C
Gain Error, +25 °C	–	±0.1	±0.25	%FSR
Gain Tempco	–	±20	±40	ppm/ °C
Harmonic Distortion (- FS) (DC to 5KHz,10V pk-pk) ①	-65	-73	–	dB
No Missing Codes	Over operating temperature range			
SIGNAL TIMING				
MUX Address Set-up Time	400	–	–	nS
Start Convert Pulse Width	0.050	1	–	µS
Data Valid Before $\overline{EOC}$ Signal Goes Low	300	–	–	nS
Conversion Time, +25 °C	–	–	12	µS
0 to +70 °C	–	–	13	µS
-55 to +125 °C	–	–	13	µS
Throughput Rates				
Gain= 1, ①	75	80	–	KHz
Gain = 2, ①	60	70	–	KHz
Gain = 4, ①	50	60	–	KHz
Gain = 8, ①	45	50	–	KHz
Gain = 10, ①	40	45	–	KHz
Gain = 100, ①	10	20	–	KHz
S/H PERFORMANCE				
Acquistion Time				
Full Scale Step to 0.01%	–	1.4	1.8	µS
Full Scale Step to 0.1%	–	0.8	1.4	µS
Aperture Delay	-50	-20	0	nS
Aperture Uncertainty	–	–	±200	pS
Slew Rate	70	90	–	V/µS
Hold Mode Settling Time, 10V to ±0.01%FS	–	200	400	nS
10V to ±0.1%FS	–	150	300	nS
Feedthrough Rejection	-80	-88	–	dB
Droop Rate, ①	–	–	100	µV/µS
POWER SUPPLY				
Range +15V	+14.25	+15.0	+15.75	V dc
-15V	-14.25	-15.0	-15.75	V dc
+5V	+4.75	+5.0	+5.25	V dc
Current +15V	–	+15	+20	mA
-15V	–	-10	-15	mA
+5V	–	+25	+35	mA
Power Dissipation	–	0.500	0.700	Watts
Power Supply Rejection	–	–	0.01%	%FSR/ %V
ENVIRONMENTAL				
Oper. Temp. Range, -MC, -PC	0	–	+70	°C
-MM	-55	–	+125	°C
Storage Temp. Range	-65	–	+150	°C
Package Type	40-pin DDIP			
Weight	0.32 oz./(9 grams) max.			

① Specifications valid at 25 °C and over the temperature ranges of 0 to +70 °C and -55 to +125 °C.

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HDAS-75/76 OPERATION

The HDAS devices accept either 8 single-ended or 4 differential input signals. Tie unused channels to SIGNAL GROUND, pin 14.

Channel selection is accomplished using the multiplexer address pins shown in Table 1. Obtain additional channels by connecting external multiplexers.

The acquisition time is the amount of time the multiplexer, instrumentation amplifier and sample-hold require to settle within a specified range of accuracy after the start convert goes high. The acquisition time can be measured by how long EOC is low before the rising edge of the START CONVERT pulse for continuous operation. Higher gains require the use of the RGAIN resistor to increase the acquisition time. The gain is equal to 1 without an RGAIN resistor. Table 2 refers to the appropriate RGAIN resistors for various throughputs.

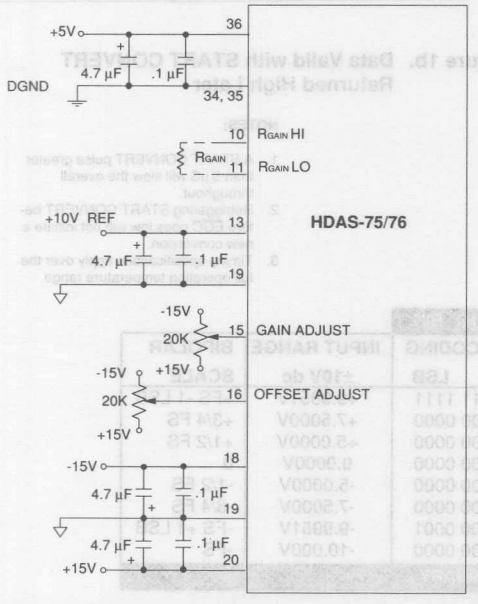

Figure 2. Typical Connection Diagram

NOTES:

1. For unipolar operation, connect pin 12 to pin 17.
2. For bipolar operation, connect pin 13 to pin 17.
3. Ground pin 15 if Gain Adjust is not used.
4. Leave pin 16 open if offset adjust is not used.
5. Position RGAIN as close as possible to pins 10 and 11. Use RN55C, 1% resistors.

CALIBRATION PROCEDURE

1. Connect the converter per Figure 2 and Tables 2 and 3 for the appropriate full-scale range (FSR). Apply a pulse of 1.0 µsec (typical) to the START CONVERT input (pin 40) at a rate of 75 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

Table 2. Input Range Parameters

INPUT RANGE	GAIN	RGAIN	THROUGHPUT
0 to +10V	1	OPEN	75 KHz
0 to +5V	2	2K Ω	60 KHz
0 to +2.5V	4	665 Ω	50 KHz
0 to +1.25V	8	287 Ω	45 KHz
0 to +1.0V	10	221 Ω	40 KHz
0 to +100mV	100	20 Ω	10 KHz
±10V	1	OPEN	75 KHz
±5V	2	2K Ω	60 KHz
±2.5V	4	665 Ω	50 KHz
±1.25V	8	287 Ω	45 KHz
±1.0V	10	221 Ω	40 KHz
±100mV	100	20 Ω	10 KHz

$$\text{Rgain} = \frac{1}{\left[\frac{(\text{gain} - 1)}{2\text{K}}\right]}$$

Table 1. MUX Channel Addressing

MUX ADDRESS PINS 39 CA2	38 CA1	37 CA0	CHANNEL	
0	0	0	0	
0	0	1	1	HDAS-76
0	1	0	2	(2-BIT ADDRESS)
0	1	1	3	
1	0	0	4	
1	0	1	5	HDAS-75
1	1	0	6	(3-BIT ADDRESS)
1	1	1	7	

2. Zero Adjustments

Apply a precision voltage reference source between the analog input and signal ground (pin 14). Adjust the output of the reference source per Table 3. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001.

For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 and 1000 0000 0001.

3. Full-Scale Adjustment

Set the output of the voltage reference used in step 2 to the value shown in Table 3. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111.

4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Table 4.

Table 3. Zero and Gain Adjust

FSR	Zero Adjust +1/2 LSB	Gain Adjust +FS - 1 1/2 LSB
0 to +10V dc	+1.22mV	+9.9963V dc
±10V dc	+2.44 mV dc	+9.9927V dc

TIMING

The $\overline{EOC}$ output signal, when high, indicates that a conversion is in process. During a conversion the digital output buffers are in a high impedance state, preventing data from being read. A START CONVERT input received during a conversion has no effect on the existing conversion. As shown in Figure1a, data can be read while START CONVERT is high and $\overline{EOC}$ is low.

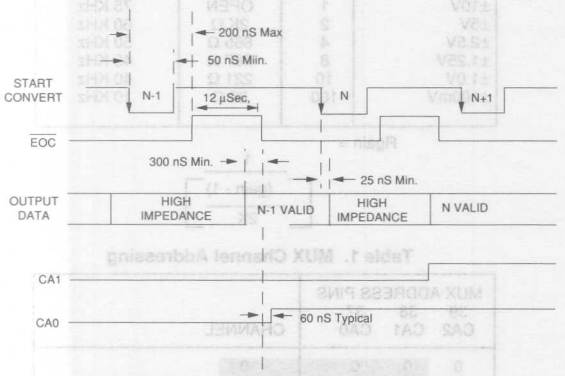

Figure 1a. Data Valid with START CONVERT Immediately Returned High

The A/D conversion begins on the falling edge of a start convert command. If START CONVERT stays low after $\overline{EOC}$ becomes low, the output buffers stay in a high impedance state. Valid data can be read 150 nanseconds maximum after START CONVERT goes high. Figure 1b shows how to use the START CONVERT pulse to control when the output data becomes valid.

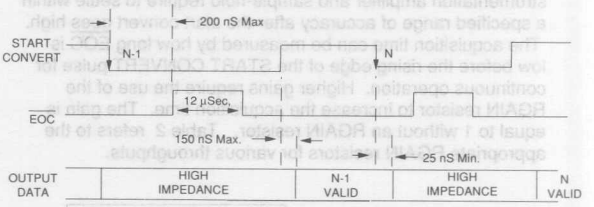

Figure 1b. Data Valid with START CONVERT Returned High Later

NOTES:

1. A START CONVERT pulse greater than 5 µS will slow the overall throughput.
2. Retriggering START CONVERT before $\overline{EOC}$ goes low will not initiate a new conversion.
3. Timing specifications apply over the full operating temperature range.

Table 4. Output Coding

		STRAIGHT BIN.		
UNIPOLAR SCALE	INPUT RANGES, V dc 0 to +10V	OUTPUT CODING MSB LSB	INPUT RANGE ±10V dc	BIPOLAR SCALE
+FS -1 LSB	+9.9976V	1111 1111 1111	+9.9951V	+FS -1 LSB
7/8 FS	+8.7500V	1110 0000 0000	+7.5000V	+3/4 FS
3/4 FS	+7.5000V	1100 0000 0000	+5.0000V	+1/2 FS
1/2 FS	+5.0000V	1000 0000 0000	0.0000V	0
1/4 FS	+2.5000V	0100 0000 0000	-5.0000V	-1/2 FS
1/8 FS	+1.2500V	0010 0000 0000	-7.5000V	-3/4 FS
1 LSB	+0.0024V	0000 0000 0001	-9.9951V	-FS +1 LSB
0	0.0000V	0000 0000 0000	-10.000V	-FS
		OFF. BINARY		

ORDERING INFORMATION

MODEL NO.	INPUT	OPERATING TEMP. RANGE	SEAL
HDAS-76PC	4 D Channels	0 to +70 °C	Plastic
HDAS-76MC	4 D Channels	0 to +70 °C	Hermetic
HDAS-76MM	4 D Channels	-55 to +125 °C	Hermetic
HDAS-76/883	4D Channels	-55 to +125 °C	Hermetic
HDAS-75PC	8 SE Channels	0 to +70 °C	Plastic
HDAS-75MC	8 SE Channels	0 to +70 °C	Hermetic
HDAS-75MM	8 SE Channels	-55 to +125 °C	Hermetic
HDAS-75/883	8 SE Channels	-55 to +125 °C	Hermetic

Receptacle for PC board mounting can be ordered through AMP Inc.,Part # 3-331272-8 (Component Lead Socket), 40 required.

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HDAS-950/-951
16-Bit, 100 KHz Data Acquisition Systems

PRELIMINARY PRODUCT DATA

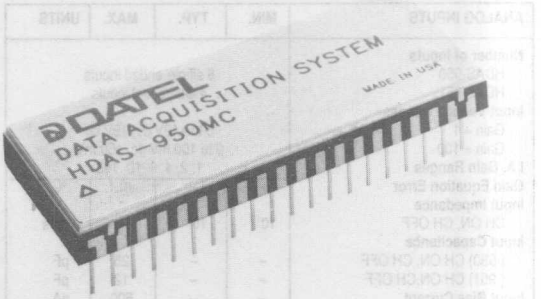
FEATURES

- **16-Bit resolution, 100 KHz**
- **8 Channels single-ended or 4 channels differential**
- **Miniature 40-pin DDIP**
- **Full-scale gain range from 100 mV to 10V**
- **High-impedance output state**

GENERAL DESCRIPTION

The HDAS-950/-951 are complete data acquisition systems containing an internal multiplexer, instrumentation amplifier, sample-hold, analog-to-digital converter and three-state outputs. Packaged in a miniature 40-pin double-dip package, the HDAS-950/-951 have a low power dissipation of 2.4 watts.

The HDAS-951 provides 4 differential inputs and the HDAS-950 provides 8 single-ended inputs. An internal instrumentation amplifier is characterized for gains of 1, 2, 4, 8, 10 and 100. the gain range is selectable using an external resistor.



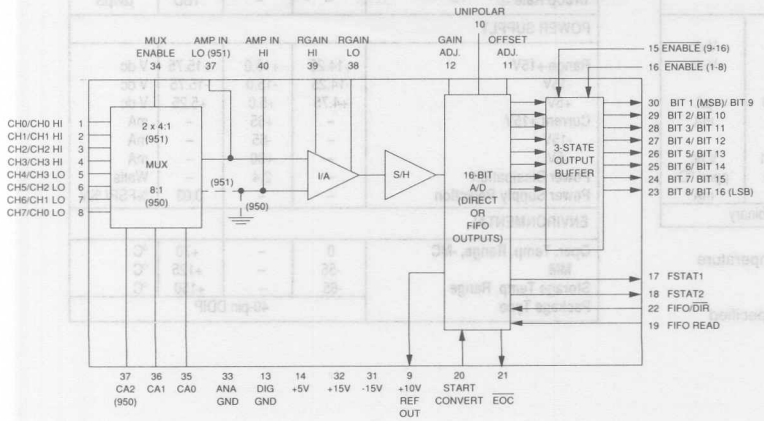
TECHNICAL NOTES

1. Use external potentiometers to remove system errors or the small initial errors to zero. Use a 20K trimming potentiometer for gain adjustment with the wiper tied to pin 12 (ground pin 12 for operation without adjustments). Use a 20K trimming potentiometer with the wiper tied to pin 11 for zero/offset adjustment (leave pin 11 open for operation without adjustment).

2. Bypass the analog and digital supplies and the +10V reference (pin 9) to ground with a 4.7 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor. Bypass the +10V reference (pin 9) to analog ground (pin 33).

3. Rated performance requires using good high-frequency circuit board layout techniques. the analog and digital grounds are not connected internally. Avoid ground-related problems by connecting the analog and digital grounds to one point, the ground plane beneath the converter. Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies.

4. Double-level multiplexing allows expanding the multiplexer channel capacity of the HDAS-950 from 8 single-ended channels to 128 single-ended channels or the HDAS-951 from 4 differential channels to 32 single-ended channels.



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	CH 0/CH 0 HI	40	AMP IN HI
2	CH 1/CH 1 HI	39	RGAIN HI
3	CH 2/CH 2 HI	38	RGAIN LO
4	CH 3/CH 3 HI	37	CA2/AMP IN LO
5	CH 4/CH 3 LO	36	CA1
6	CH 5/CH 2 LO	35	CA0
7	CH 6/CH 1 LO	34	MUX ENABLE
8	CH 7/CH 0 LO	33	ANALOG GROUND
9	+10V REF. OUT	32	+15V POWER
10	UNIPOLAR	31	-15V POWER
11	OFFSET ADJUST	30	BIT 1(MSB)/ BIT 9
12	GAIN ADJUST	29	BIT 2/ BIT 10
13	DIGITAL GROUND	28	BIT 3/ BIT 11
14	+5V POWER	27	BIT 4/ BIT 12
15	ENABLE (9-16)	26	BIT 5/ BIT 13
16	ENABLE (1-8)	25	BIT 6/ BIT 14
17	FSTAT1	24	BIT 7/ BIT 15
18	FSTAT2	23	BIT 8/ BIT 16 (LSB)
19	FIFO READ	22	FIFO/DIR
20	START CONVERT	21	EOC

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (pin 32)	0 to +18	V dc
-15V Supply (pin 31)	0 to -18	V dc
+5V Supply (pin 14)	-0.5 to +7.0	V dc
Digital Inputs (pins 15-20, 22, 34-37)	-0.3 to V_{DD} +0.3	V dc
Analog Inputs (pins 1-8)	±14	V
Lead Temp. (10 Sec.)	300	°C

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V dc and +5V dc unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Number of Inputs				
HDAS-950	8 single-ended inputs			
HDAS-951	4 differential inputs			
Input Voltage Ranges				
Gain = 1	0 to +10V dc, ±5V dc			
Gain = 100	0 to 100 mV dc, ±50 mV			
I.A. Gain Ranges	1, 2, 4, 8, 10, 100			
Gain Equation Error	–	–	±0.1	%
Input Impedance				
CH ON, CH OFF	10^{13}	10^{14}	–	Ohms
Input Capacitance				
(-950) CH ON, CH OFF	–	–	25	pF
(-951) CH ON,CH OFF	–	–	12	pF
Input Bias Current	–	–	500	nA
Input Offset Current	–	–	20	nA
Input Offset Voltage	–	±2	–	mV
Common Mode Volt. Range	±10	–	–	V
CMMR, G=1, @ 10Hz,				
Vcm=1V p-p	–	-110	–	dB
Voltage Noise (RMS)				
Gain = 1	–	–	TBD	µV
Gain = 8	–	–	TBD	µV
MUX Crosstalk @ 100 KHz	–	-72	–	dB
Bias Current Tempco	Doubles (max.) every 10 °C above 70 °C			
Offset Current Tempco	Doubles (max.) every 10 °C above 70 °C			
Offset Voltage Tempco	(±30 ppm/ °C x gain) ±20 ppm/ °C (max.)			
Input Gain Equation	Rg = 2K/(gain -1)			
DIGITAL INPUTS				
Logic Levels				
Logic 1	2.25	–	–	V dc
Logic 0	–	–	0.8	V dc
Logic Loading				
Logic 1	–	–	+5	µA
Logic 0	–	–	-200	µA
OUTPUTS				
Logic Levels				
Logic 1	2.4	–	–	V dc
Logic 0	–	–	0.4	V dc
Logic Loading				
Logic 1	–	–	-160	µA
Logic 0	–	–	6.4	mA
Internal Reference				
Voltage, +25 °C	+9.9	+10.0	+10.1	V dc
Drift	–	±15	±40	ppm/ °C
External Current	–	–	5	mA
Output Coding	Straight binary/Offset binary			

NOTES:
① Specifications valid at 25 °C and over the operating temperature ranges of 0 to +70 °C and -55 to +125 °C.

② Pulse widths greater than 5 µSec. will decrease the specified throughput rate.

PERFORMANCE	MIN.	TYP.	MAX.	UNITS
Resolution	16	–	–	Bits
Integral Nonlinearity,25 °C	–	–	±0.006	%FSR
0 to +70 °C	–	–	±0.012	%FSR
-55 to +125 °C	–	–	TBD	%FSR
Differential Nonlinearity, +25 °C	–	–	±0.006	%FSR
0 to +70 °C	–	–	±0.012	%FSR
-55 to +125 °C	–	–	TBD	%FSR
F.S. Abs. Accuracy +25 °C	–	–	±0.15	%FSR
0 to +70 °C	–	–	TBD	%FSR
-55 to +125 °C	–	–	TBD	%FSR
Unipolar Zero Error,+25 °C	–	–	±0.05	%FSR
Unipolar Zero Tempco	–	–	TBD	ppm/ °C
Bipolar Zero Error, +25 °C	–	–	±0.05	%FSR
Bipolar Zero Tempco	–	–	TBD	ppm/ °C
Bipolar Offset Error,+25 °C	–	–	±0.1	%FSR
Bipolar Offset Tempco	–	–	TBD	ppm/ °C
Gain Error, +25 °C	–	–	±0.1	%FSR
Gain Tempco	–	–	TBD	ppm/ °C
Harmonic Distortion (- FS) (DC to 5KHz,10V pk-pk)				
+25 °C	–	-78	–	dB
-55 to +125 °C	–	TBD	–	dB
No Missing Codes	Over operating temperature range			
SIGNAL TIMING				
Enable to Data Val. Delay	–	–	10	nS
MUX Address Set-up Time	400	–	–	nS
Start Convert Pulse Width, ②	0.800	–	5.0	µS
Data Valid After				
EOC Signal Goes Low	35	–	–	nS
Conversion Time, ①	–	–	4	µS
Throughput Rates				
Gain= 1,				
+25 °C	100	–	–	KHZ
0 to +70 °C	TBD	–	–	KHz
-55 to +125 °C	TBD	–	–	KHz
Gain = 2, ①	–	75	–	KHz
Gain = 4, ①	–	75	–	KHz
Gain = 8, ①	–	75	–	KHz
Gain = 10, ①	–	75	–	KHz
Gain = 100, ①	–	50	–	KHz
S/H PERFORMANCE				
Acquistion Time				
Full Scale Step to 0.01%	–	5.2	–	µS
Full Scale Step to 0.1%	–	4.2	–	µS
Aperture Delay	–	-20	0	nS
Aperture Uncertanty	–	±100	–	pS
Slew Rate	–	90	–	V/µS
Hold Mode Settling Time,				
10V to ±0.003% FS	–	800	–	nS
10V to ±0.1%FS	–	400	–	nS
Feedthrough Rejection	–	TBD	–	dB
Droop Rate ①	–	–	TBD	µV/µS
POWER SUPPLY				
Range +15V	+14.25	+15.0	+15.75	V dc
-15V	-14.25	-15.0	-15.75	V dc
+5V	+4.75	+5.0	+5.25	V dc
Current +15V	–	+65	–	mA
-15V	–	-65	–	mA
+5V	–	+80	–	mA
Power Dissipation	–	2.4	–	Watts
Power Supply Rejection	–	–	0.03	%FSR/ %V
ENVIRONMENTAL				
Oper. Temp. Range, -MC	0	–	+70	°C
MM	-55	–	+125	°C
Storage Temp. Range	-65	–	+150	°C
Package Type	40-pin DDIP			

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HDAS-950/951 OPERATION

The HDAS devices accept either 8 single-ended or 4 differential input signals. Tie unused channels to ANALOG GROUND, pin 33.

Channel selection is accomplished using the multiplexer address pins shown in Table 1. Obtain additional channels by connecting external multiplexers.

The acquisition time is the amount of time the multiplexer, instrumentation amplifier and sample-hold require to settle within a specified range of accuracy prior to $\overline{EOC}$ going low. The acquisition time can be measured by how long $\overline{EOC}$ is low before the rising edge of the START CONVERT pulse for continuous operation. Higher gains require the use of the RGAIN resistor to increase the acquisition time. The gain is equal to 1 without an RGAIN resistor. Table 2 refers to the appropriate RGAIN resistors for various throughputs.

Table 2. Input Range Parameters

INPUT RANGE	GAIN	RGAIN	THROUGHPUT
0 to +10V	1	OPEN	100 KHz
0 to +5V	2	2K Ω	75 KHz
0 to +2.5V	4	665 Ω	75 KHz
0 to +1.25V	8	287 Ω	75 KHz
0 to +1.0V	10	221 Ω	75 KHz
0 to +100mV	100	20 Ω	50 KHz
±5V	1	OPEN	100 KHz
±2.5V	2	2K Ω	75 KHz
±1.25V	4	665 Ω	75 KHz
±0.625V	8	287 Ω	75 KHz
±0.5V	10	221 Ω	75 KHz
±50mV	100	20 Ω	50 KHz

Note Rgain = 2K/(gain -1)

The HDAS devices enter the hold mode and are ready for conversion upon the start convert going high; the falling edge forces $\overline{EOC}$ high. the conversion is complete within a maximum of 4 µsec (+25 °C). $\overline{EOC}$ returns low, the data is valid and sent to the output. The sample/hold is now ready to acquire new data. The next start convert pulse repeats the process for the next conversion.

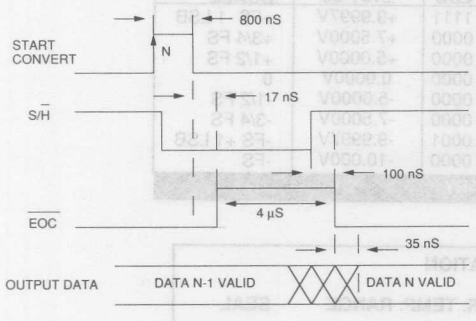

Figure 1. HDAS-950/-951 Timing

The specifications listed in Figure 1 apply over the full operating temperature range unless otherwise specified.

	FSTAT1	FSTAT2
Empty	0	1
Half-full	1	0
Full	1	1

Table 5. FIFO Status

FIFO OPERATION

FIFO/$\overline{DIR}$ — When HIGH, the FIFO is enabled. When LOW, the data is brought directly to the output bits.

FIFO READ — A rising pulse edge brings the oldest (First In) word stored in the memory to the output bits.

FSTAT1, FSTAT2 — These outputs show the status of the FIFO. See Table 5.

Table 1. MUX Channel Addressing

MUX ADDRESS PINS 37 CA2	36 CA1	35 CA0	CHANNEL	
0	0	0	0	
0	0	1	1	HDAS-951
0	1	0	2	(2-BIT ADDRESS)
0	1	1	3	
1	0	0	4	
1	0	1	5	HDAS-950
1	1	0	6	(3-BIT ADDRESS)
1	1	1	7	

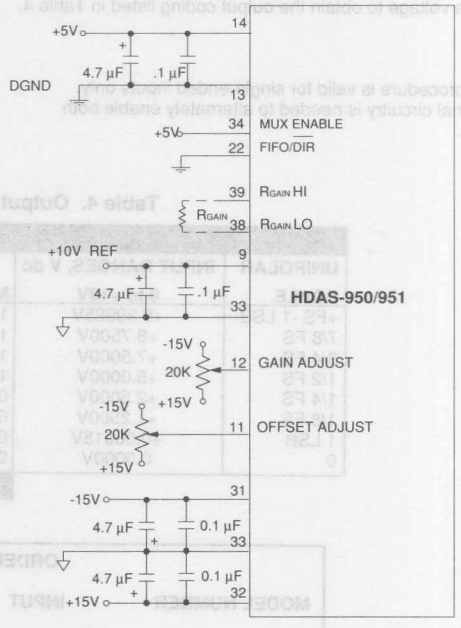

Figure 2. Typical Connection Diagram

NOTES:

1. For unipolar operation, connect pin 9 to pin 10.
2. For bipolar operation, leave pin 10 floating.
3. Position Rgain as close as possible to pins. Use RN55C, 1% resistors.

propriate full-scale range (FSR). Apply a pulse of 1.0 µsec (typical) to the START CONVERT input (pin 20) at a rate of 50 KHz. This rate is chosen to reduce flicker if LED's are used on the outputs for calibration purposes.

2. Zero Adjustments

Apply a precision voltage reference source between the analog input and analog ground (pin 33). Adjust the output of the reference source per Table 3 for the unipolar zero or the bipolar zero adjustment. For unipolar, adjust the zero trimming potentiometer so that the output code flickers equally between 0000 0000 0000 0000 and 0000 0000 0000 0001.

For bipolar operation, adjust the potentiometer such that the code flickers equally between 1000 0000 0000 0000 and 1000 0000 0000 0001.

3. Full-Scale Adjustment

Set the output of the voltage reference used in step 2 to the value shown in Table 3 or for the unipolar or bipolar gain adjustment. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1111 1110 and 1111 1111 1111 1111.

4. To confirm proper operation of the device, vary the precision reference voltage to obtain the output coding listed in Table 4.

NOTES

1. This procedure is valid for single-ended inputs only.
2. External circuitry is needed to alternately enable both bytes.

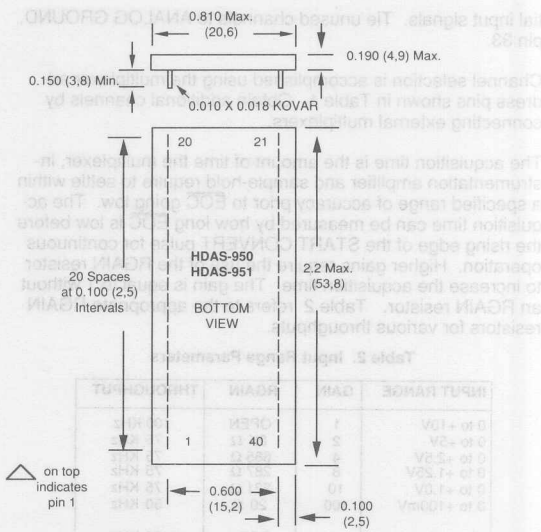

Table 3. Zero and Gain Adjust

FSR	Zero Adjust +1/2 LSB	Gain Adjust +FS - 1 1/2 LSB
0 to +10V dc	+76 µV	+9.99977V dc
±10V dc	+153 µV dc	+9.99954V dc

Table 4. Output Coding

		STRAIGHT BIN.		
UNIPOLAR	INPUT RANGES, V dc	OUTPUT CODING	INPUT RANGE	BIPOLAR
SCALE	0 to +10V	MSB LSB	±10V dc	SCALE
+FS -1 LSB	+9.99985V	1111 1111 1111 1111	+9.9997V	+FS -1 LSB
7/8 FS	+8.7500V	1110 0000 0000 0000	+7.5000V	+3/4 FS
3/4 FS	+7.5000V	1100 0000 0000 0000	+5.0000V	+1/2 FS
1/2 FS	+5.0000V	1000 0000 0000 0000	0.0000V	0
1/4 FS	+2.5000V	0100 0000 0000 0000	-5.0000V	-1/2 FS
1/8 FS	+1.2500V	0010 0000 0000 0000	-7.5000V	-3/4 FS
1 LSB	+0.00015V	0000 0000 0000 0001	-9.9997V	-FS +1 LSB
0	0.0000V	0000 0000 0000 0000	-10.000V	-FS
		OFFSET BINARY		

ORDERING INFORMATION

MODEL NUMBER	INPUT	OPER. TEMP. RANGE	SEAL
HDAS-951MC	4 D CHANNELS	0 to +70 °C	Hermetic
HDAS-951MM	4 D CHANNELS	-55° to +125°C	Hermetic
HDAS-950MC	8 SE CHANNELS	0 to +70° C	Hermetic
HDAS-950MM	8 SE CHANNELS	-55 to +125 °C	Hermetic

Receptacle for PC board mounting can be ordered through AMP Inc.,Part # 3-331272-8 (Component Lead Socket), 40 required.

For high reliability versions of the HDAS-950 & HDAS-951, contact DATEL.

MULTIPLEXERS

	Model	Channels	Settling Time 20V to 0.01%	Access Time	Input Range	Power (Watts)	Case	Page
	MXD-409	4 D	3 µs	500 ns	±15V	0.105	16-Pin DIP	6-5
	MX-808	8 SE	3 µs	500 ns	±15V	0.105	16-Pin DIP	6-5
	MXD-807	8 D	3 µs	500 ns	±15V	0.105	28-Pin DIP	6-5
	MX-1606	16 SE	3 µs	500 ns	±15V	0.105	28-Pin DIP	6-5
	MVD-409	4 D	2.8 µs	350 ns	±15V	0.055	16-Pin DIP	6-1
	MV-808	8 SE	2.8 µs	350 ns	±15V	0.055	16-Pin DIP	6-1
	MVD-807	8 D	2.4 µs	300 ns	±15V	0.105	28-Pin DIP	6-1
	MV-1606	16 SE	2.4 µs	300 ns	±15V	0.105	28-Pin DIP	6-1
	MX-818C	8 SE/4D	800 ns	125 ns	±15V	0.540	18-Pin DIP	6-9
	MX-1616C	16 SE/8 D	800 ns	150 ns	±15V	0.900	28-Pin DIP	6-9
New	**MX-826**	8 SE	200 ns	70 ns	±10.5V	0.395	24-Pin DIP	6-13
New	**MX-850**	4 SE	50 ns	20 ns	±10V	0.250	14-Pin DIP	6-15

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MV Series
Low ON-Resistance CMOS Analog Multiplexers

FEATURES

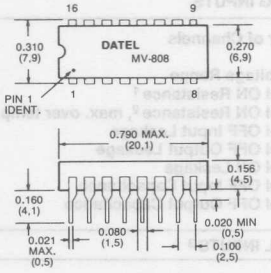
- 0.01% Accuracy
- Low "ON" resistance
- Break-before-make switching
- Dielectrically isolated CMOS
- Single-ended or differential
- Fast settling time
- DTL/TTL/CMOS-compatible
- 350 KHz Sampling rate

GENERAL DESCRIPTION

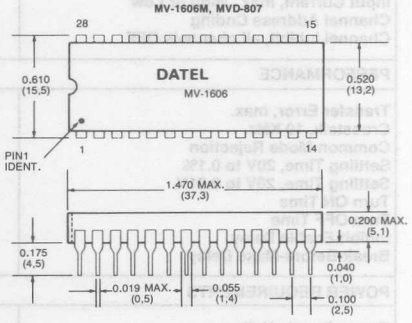
The MV Series analog multiplexers are 4-, 8-, and 16-channel monolithic devices featuring a low ON resistance of 270 ohms. These units are manufactured with CMOS technology using a dielectric isolation process. There are 8- and 16-channel single-ended models and 4- and 8-channel differential models in this series. Channel addressing is done by a 2-, 3-, or 4-bit binary code; an inhibit input enables or disables the entire device to permit expansion of the number of channels by using several devices together. Another important feature is break-before-make switching, which insures that no two channels are ever momentarily shorted together. With a high impedance load, transfer accuracies of 0.01% can be achieved at channel sampling rates up to 350 KHz.

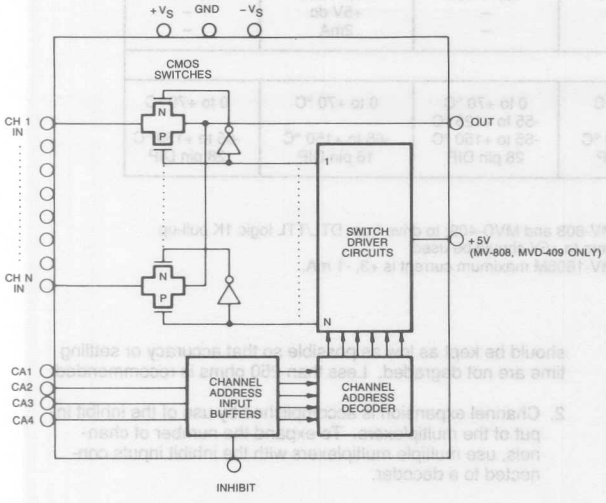
MECHANICAL DIMENSIONS INCHES (MM)

MV-808, MVD-409

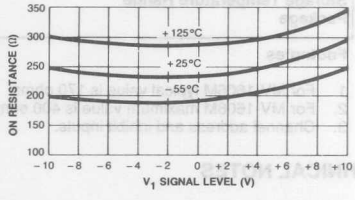


MV-1606M, MVD-807





ON RESISTANCE VS. TEMPERATURE



Power Supply, analog	±20V	±20V	±20V	±20V
Power Supply, digital	+30V	–	+30V	–
Analog Input Voltage	±|Vs +2V|	±|Vs +2V|	±|Vs +2V|	±|Vs +2V|
Digital Input Voltage	±Vs	±|Vs +4V|	±Vs	±|Vs +4V|
Package Dissipation, max.	780 mW	1200 mW	780 mW	1200 mW

FUNCTIONAL SPECIFICATIONS

Typical at +15V supplies (and +5V supply for MV-808 & MVD-409), unless otherwise noted.

ANALOG INPUTS	MV-808	MV-1606/1606M	MVD-409	MVD-807
Number of Channels	8	16	4	8
Type	Single-ended	Single-ended	Differential	Differential
Input Voltage Range	±15V	±15V	±15V	±15V
Channel ON Resistance [1]	250Ω	270Ω	250Ω	270Ω
Channel ON Resistance [2], max. over temp.	500Ω	500Ω	500Ω	500Ω
Channel OFF Input Leakage	20 pA	30 pA	20 pA	30 pA
Channel OFF Output Leakage	100 pA	1.0 nA	50 pA	1.0 nA
Channel ON Leakage	100 pA	1.0 nA	50 pA	1.0 nA
Channel OFF Input Capacitance	4 pF	4 pF	4 pF	4 pF
Channel OFF Output Capacitance	20 pF	44 pF	10 pF	22 pF
DIGITAL INPUTS [3]				
Logic 0 Threshold, max.	+0.4V	+0.8V	+0.4V	+0.8V
Logic 1 Threshold [4], min.	+4.0V	+2.4V	+4.0V	+2.4V
Input Current, max., High or Low	1 µA	5 µA	1 µA	5 µA
Channel Address Coding	3 Bits	4 Bits	2 Bits	3 Bits
Channel Inhibit, all channels OFF	Logic 1	Logic 0	Logic 1	Logic 0
PERFORMANCE				
Transfer Error, max.	0.01%	0.01%	0.01%	0.01%
Crosstalk, 10 KHz	-86 dB	-86 dB	-86 dB	-86 dB
Common Mode Rejection	–	–	120 dB	120 dB
Settling Time, 20V to 0.1%	1.1 µS	1.2 µS	1.1 µS	1.2 µS
Settling Time, 20V to 0.01%	2.8 µS	2.4 µS	2.8 µS	2.4 µS
Turn ON Time	350 nS	300 nS	350 nS	300 nS
Turn OFF Time	250 nS	220 nS	250 nS	220 nS
Inhibit/Enable Delay	300 nS	300 nS	300 nS	300 nS
Break-Before-Make Delay	100 nS	80 nS	100 nS	80 nS
POWER REQUIREMENTS				
Power Supply Voltage	±15V dc	±15V dc	±15V dc	±15V dc
Power Supply Current [5], max.	+1, -2 mA	+3, -1 mA	+1, -1 mA	+3, -1 mA
Digital Supply Voltage	+5V dc	–	+5V dc	–
Digital Supply Current, max.	2 mA	–	2mA	–
PHYSICAL/ENVIRONMENTAL				
Operating Temperature Range	0 to +70 °C	0 to +70 °C	0 to +70 °C	0 to +70 °C
MV-1606M Oper. Temp. Range		-55 to +125 °C		
Storage Temperature Range	-65 to +150 °C	-65 to +150 °C	-65 to +150 °C	-65 to +150 °C
Package	16 pin DIP	28 pin DIP	16 pin DIP	28 pin DIP

Footnotes

1. For MV-1606M typical value is 170 ohms.
2. For MV-1606M maximum value is 400 ohms.
3. Channel address and inhibit inputs.
4. For MV-808 and MVD-409; to drive from DTL/TTL logic 1K pull-up resistors to +5V should be used.
5. For MV-1606M maximum current is +3, -1 mA.

TECHNICAL NOTES

1. The transfer accuracy of the MV series multiplexers depends on both the source resistance and load resistance. For example, with zero source resistance and assuming 500 ohms maximum channel ON resistance, the load impedance must be at least 5 megohms to achieve 0.01% accuracy. In practice it is recommended that a load impedance of 10^8 ohms or more be used. Source resistance should be kept as low as possible so that accuracy or settling time are not degraded. Less than 250 ohms is recommended.

2. Channel expansion is accomplished by use of the inhibit input of the multiplexers. To expand the number of channels, use multiple multiplexers with the inhibit inputs connected to a decoder.

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CONNECTION AND APPLICATION

CHANNEL ADDRESSING

MV-1606

8	4	2	1	INHIB.	ON CHANNEL
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

MV-808, MVD-807

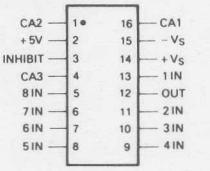
4	2	1	MVD-807 INHIB.	MV-808 INHIB.	ON CHANNEL
X	X	X	0	1	NONE
0	0	0	1	0	1
0	0	1	1	0	2
0	1	0	1	0	3
0	1	1	1	0	4
1	0	0	1	0	5
1	0	1	1	0	6
1	1	0	1	0	7
1	1	1	1	0	8

MVD-409

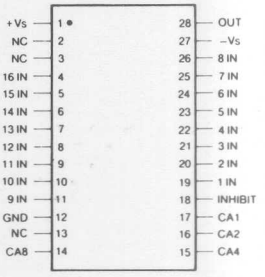
2	1	INHIB.	ON CHANNEL
X	X	1	NONE
0	0	0	1
0	1	0	2
1	0	0	3
1	1	0	4

PIN CONNECTIONS

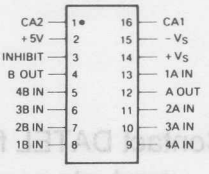
MV-808



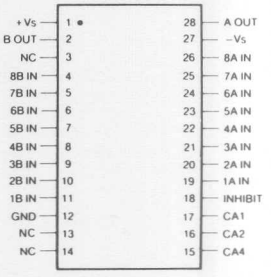
MV-1606



MVD-409



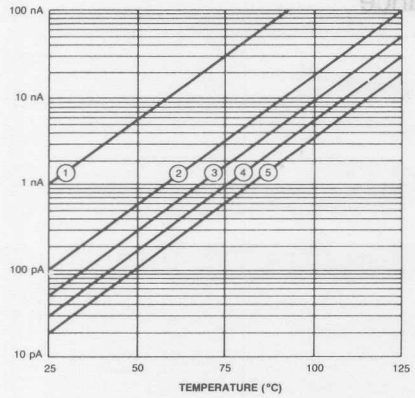
MVD-807



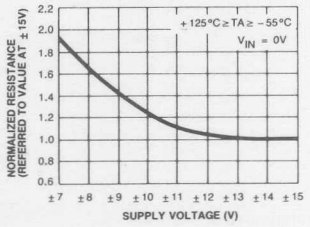
NOTES:
CA = CHANNEL ADDRESS
VS = SUPPLY VOLTAGE
NC = NO CONNECTIONS

TOP VIEW SHOWN

LEAKAGE CURRENT VS. TEMPERATURE

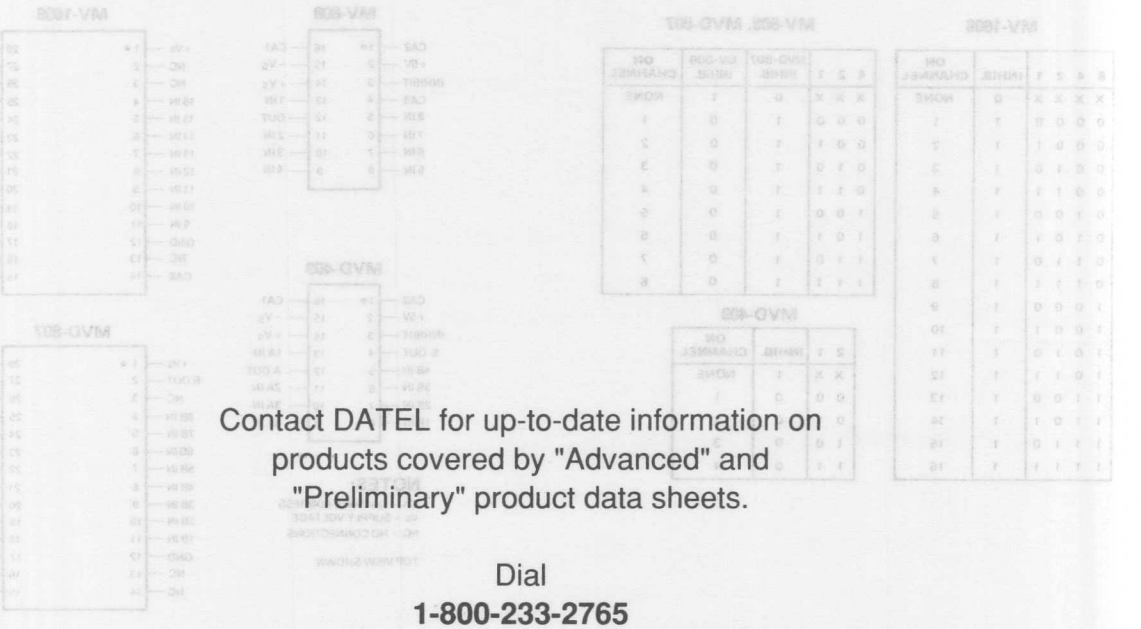


1. MV-1606, MVD-807 CHANNEL OFF OUTPUT LEAKAGE
2. MV-808 CHANNEL OFF OUTPUT LEAKAGE
3. MVD-409 CHANNEL OFF OUTPUT LEAKAGE
4. MV-1606, MVD-807 CHANNEL OFF INPUT LEAKAGE
5. MV-808, MVD-409 CHANNEL OFF INPUT LEAKAGE



ORDERING INFORMATION

MODEL NO.	CHANNELS	OPERATING TEMP. RANGE
MV-808	8 S.E.	0 to 70°C
MV-1606	16 S.E.	0 to 70°C
MV-1606M	16 S.E.	−55 to +125°C
MVD-409	4 Diff.	0 to 70°C
MVD-807	8 Diff.	0 to 70°C



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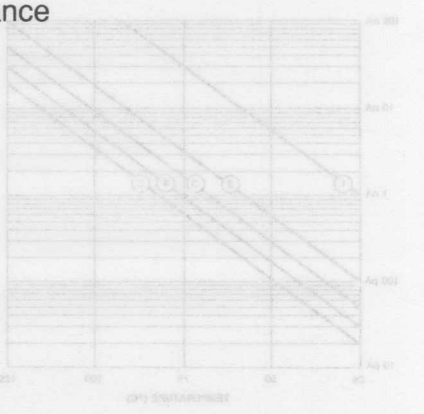

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MX Series
4-, 8-, and 16-Channel CMOS Multiplexers

FEATURES

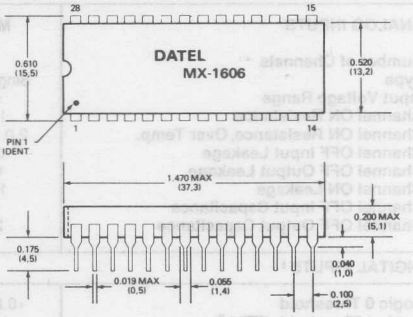
- 200 KHz Sampling rates
- 0.01% Accuracy
- Dielectrically isolated CMOS
- Break-before-make switching
- Single-ended and differential
- Overvoltage protection
- DTL/TTL/CMOS-compatible
- 7.5 mW Standby power

GENERAL DESCRIPTION

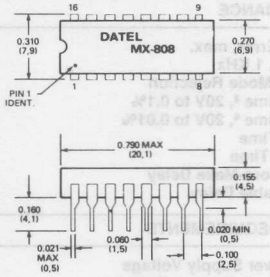
The MX Series analog multiplexers are 4-, 8-, and 16-channel monolithic devices manufactured with a dielectrically isolated complementary MOS process. The circuits incorporate analog and digital input protection which protects the units from both overvoltage and loss of power. The digital inputs are DTL/TTL/CMOS compatible and address the proper channel by means of a 2-, 3-, or 4-bit binary code. An inhibit input enables or disables the entire device and this permits expansion of the number of channels by using several devices together. Another important feature of these multiplexers is the use of break-before-make switching to in-sure that no two channels are ever momentarily shorted together. Transfer accuracies of 0.01% can be achieved at channel sampling rates up to 200 KHz and over ±10V signal ranges.

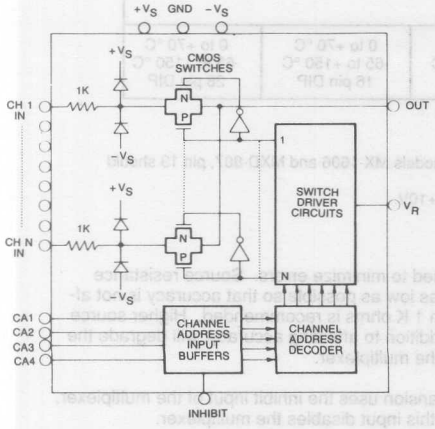
MECHANICAL DIMENSIONS — INCHES (MM)

MX-1606, MXD-807

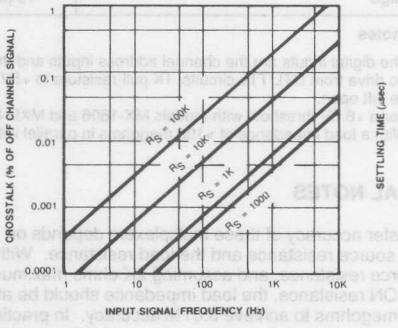


MX-808, MXD-409





CROSSTALK VS. FREQUENCY OF INPUT SIGNAL



	MX-808	MX-1606	MXD-409	MXD-807
Voltage Between Supply Pins	40V	40V	40V	40V
VREF to Ground, V + to Ground	+20V	+20V	+20V	+20V
Digital Input Overvoltage	±|Vs +4V|	±|Vs +4V|	±|Vs +4V|	±|Vs +4V|
Analog Input Overvoltage	±|Vs +20V|	±|Vs +20V|	±|Vs +20V|	±|Vs +20V|
Package Dissipation, max.	725 mW	1200 mW	725 mW	1200 mW

FUNCTIONAL SPECIFICATIONS

Typical at 25 °C +15V supplies R source <1K, unless otherwise noted.

ANALOG INPUTS	**MX-808**	**MX-1606**	**MXD-409**	**MXD-807**
Number of Channels	8	16	4	8
Type	Single-ended	Single-ended	Differential	Differential
Input Voltage Range	±15V	±15V	±15V	±15V
Channel ON Resistance	1.5 KΩ	1.5 KΩ	1.5 KΩ	1.5 KΩ
Channel ON Resistance, Over Temp.	2.0 KΩ max.	2.0 KΩ max.	2.0 KΩ max.	2.0 KΩ max.
Channel OFF Input Leakage	30 pA	30 pA	30 pA	30 pA
Channel OFF Output Leakage	1.0 nA	1.0 nA	1.0 nA	1.0 nA
Channel ON Leakage	100 pA	100 pA	100 pA	100 pA
Channel OFF Input Capacitance	5 pF	5 pF	5 pF	5 pF
Channel OFF Output Capacitance	25 pF	50 pF	12 pF	25 pF
DIGITAL INPUTS [1]				
Logic 0 Threshold	+0.8V, max.	+0.8V, max.	+0.8V, max.	+0.8V, max.
Logic 1 Threshold, (TTL) [2]	+4.0V min.	+4.0V min.	+4.0V min.	+4.0V min.
Logic 1 Threshold, (CMOS) [3]	+6.0V min.	+6.0V min.	–	–
Input Current, High or Low	5 µA max.	5 µA max.	5 µA max.	5 µA max.
Channel Address Coding	3 Bits	4 Bits	2 Bits	3 Bits
Channel Inhibit, all channels OFF	Logic 0	Logic 0	Logic 0	Logic 0
PERFORMANCE				
Transfer Error, max.	0.01%	0.01%	0.01%	0.01%
Crosstalk, 1 KHz	0.005%	0.005%	0.005%	0.005%
Common Mode Rejection	–	–	120 dB	120 dB
Settling Time [4], 20V to 0.1%	2 µS	2 µS	2 µS	2 µS
Settling Time [4], 20V to 0.01%	3 µS	3 µS	3 µS	3 µS
Turn ON Time	500 nS	500 nS	500 nS	500 nS
Turn OFF Time	300 nS	300 nS	300 nS	300 nS
Break-Before-Make Delay	80 nS	80 nS	80 nS	80 nS
Inhibit/Enable Delay	300 nS	300 nS	300 nS	300 nS
POWER REQUIREMENTS				
Rated Power Supply Voltage	±15V dc	±15V dc	±15V dc	±15V dc
Power Supply Voltage Range	±5V to ±20V	±5V to ±20V	±5V to ±20V	±5V to ±20V
Quiescent Current, max.	+2, -1 mA	+2, -1 mA	+2, -1 mA	+2, -1 mA
Power Consumption, 10 KHz Sampling	7.5 mW	7.5 mW	7.5 mW	7.5 mW
PHYSICAL/ENVIRONMENTAL				
Operating Temperature Range	0 to +70 °C	0 to +70 °C	0 to +70 °C	0 to +70 °C
Storage Temperature Range	-65 to +150 °C	-65 to +150 °C	-65 to +150 °C	-65 to +150 °C
Package	16 pin DIP	28 pin DIP	16 pin DIP	28 pin DIP

Footnotes

1. The digital inputs are the channel address inputs and the inhibit input.
2. To drive from DTL/TTL circuits, 1K pull-resistors to +5V are recommended. With models MX-1606 and MXD-807, pin 13 should be left open.
3. For a +6.0V threshold with models MX-1606 and MXD-807, pin 13 is connected to +10V.
4. With a load impedance of >100 megohms in parallel with 2 pF.

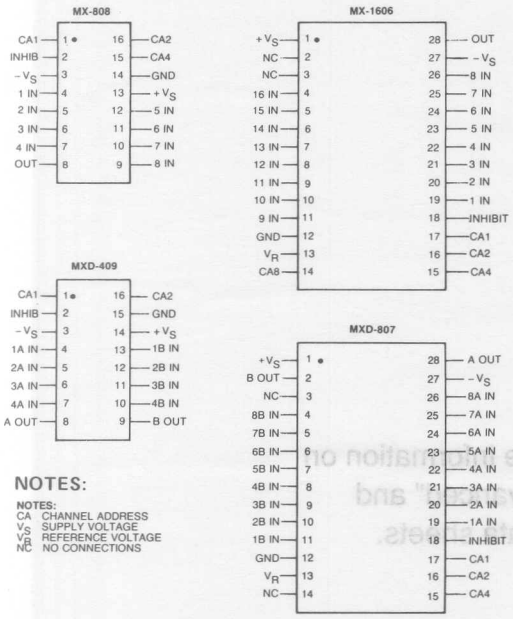
TECHNICAL NOTES

1. The transfer accuracy of these multiplexers depends on both the source resistance and the load resistance. With zero source resistance, and assuming 2K ohms maximum channel ON resistance, the load impedance should be at least 20 megohms to achieve 0.01% accuracy. In practice, it is recommended that a load impedance of at least 100 megohms be used to minimize errors. Source resistance should be kept as low as possible so that accuracy is not affected; less than 1 K ohms is recommended. Higher source resistance, in addition to affecting accuracy, will degrade the settling time of the multiplexer.

2. Channel expansion uses the inhibit input of the multiplexer. A logic 0 on this input disables the mulitplexer.

CONNECTION & APPLICATION

PIN CONNECTIONS



NOTES:

NOTES:
CA CHANNEL ADDRESS
VS SUPPLY VOLTAGE
VR REFERENCE VOLTAGE
NC NO CONNECTIONS

CHANNEL ADDRESSING

MX-1606

8	4	2	1	INHIB.	ON CHANNEL
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

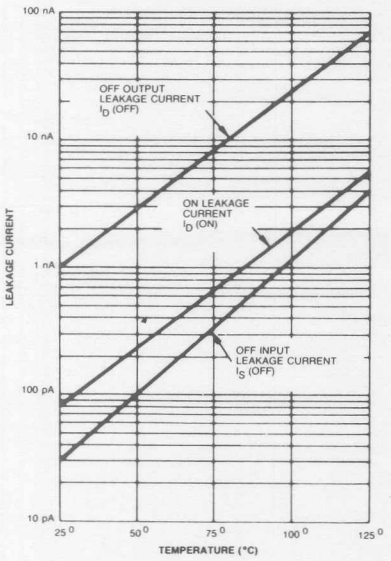
MX-808, MXD-807

4	2	1	INHIB.	ON CHANNEL
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

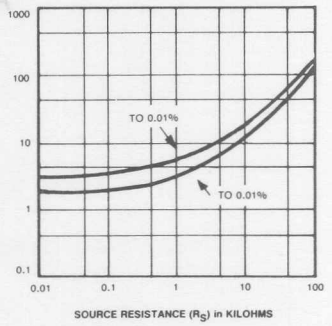
MXD-409

2	1	INHIB.	ON CHANNEL
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

LEAKAGE CURRENT VS. TEMP.



SETTLING TIME VS. SOURCE RESISTANCE (20V STEP)



ORDERING INFORMATION

MODEL NO.	CHANNELS	OPERATING TEMP. RANGE
MX-808	8 S.E.	0°C to +70°C
MX-1606	16 S.E.	0°C to +70°C
MXD-409	4 Diff.	0°C to +70°C
MXD-807	8 Diff.	0°C to +70°C

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MX-1616, MX-818

High-Speed CMOS Analog Multiplexers

FEATURES

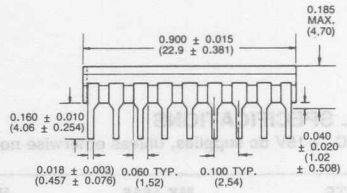
- **800 Nanoseconds settling time**
- **Programmable input mode**
- **Break-before-make switching**
- **Dielectrically isolated CMOS**
- **TTL/CMOS-compatible**

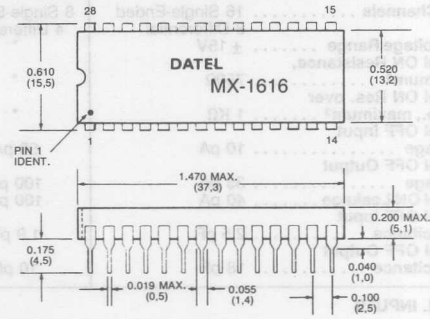
GENERAL DESCRIPTION

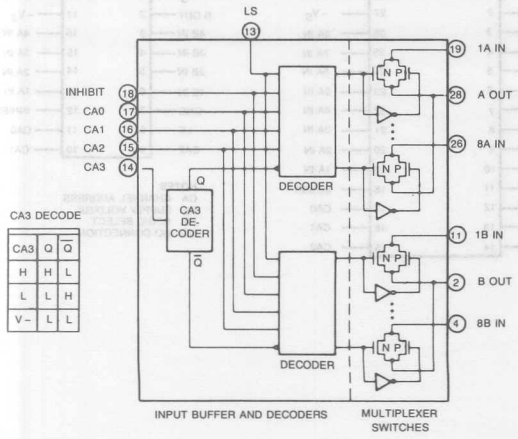
The MX-1616 and MX-818 are high-speed high performance analog multiplexers manufactured with a dielectrically isolated CMOS process. Both devices achieve transfer accuracies of 0.01% at channel sampling rates of up to 1.25 MHz over ±10V signal ranges. These multiplexers are ideal for high-speed, multichannel, data acquisition systems where the multiplexer operates into a high impedance load such as a sample-hold, buffer amplifier or instrumentation amplifier.

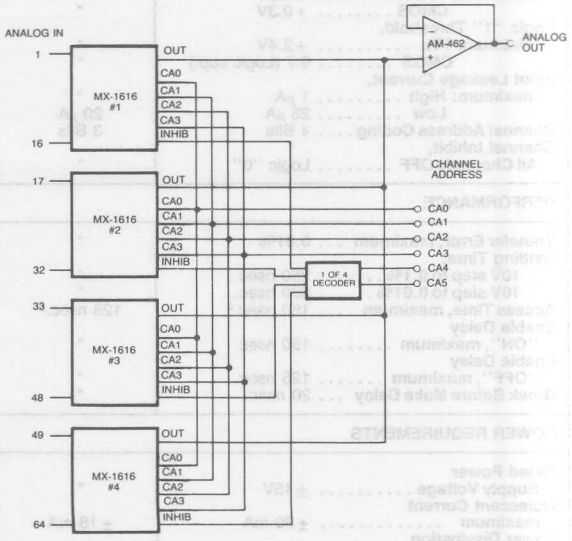
A unique feature of these circuits is tha ability of the use to program their inputs for either single-ended or differential operation. The MX-1616 is user programmable either as a single-ended 16-channel or as a differential 8-channel multiplexer while the MX-818 is user programmable either as a single-ended 8-channel or as a differential 4-channel multiplexer.

MECHANICAL DIMENSIONS INCHES (MM)









64 CHANNEL EXPANSION

ABSOLUTE MAXIMUM RATINGS	MX-1616	MX-818
Voltage Between Supply Pins	33V	*
Analog Input Voltage	$\pm(V_s + 2V)$	*
Digital Input Voltage:		
TTL[1]	CA3 = $(-V_S - 2V)$ < Logic "1" < +6V	CA2 = $(-V_S - 2V)$ *
CMOS[2]	$+V_S + 2V$ GRND − 2V	* *
Package Dissipation, maximum	1200 mW	725 mW

PHYSICAL/ENVIRONMENTAL	MX-1616	MX-818
Operating Temp. Range: C Suffix	0°C to +70°C	*
Storage Temperature Range	−65°C to +155°C	*
Package	28-Pin DIP	18 Pin DIP

* Same specification as column 1.

FOOTNOTES:

1. For TTL compatibility, the Logic Select pin (MX-1616 Pin 13, MX-818 Pin 8) is grounded or left open.
2. For CMOS compatibility, the Logic Select Pin (MX-1616 Pin 13, MX-818 Pin 8) is tied to the system Logic Supply.
3. Vin = ±10V, Iout = −100 μA.
4. 200 nseconds maximum at full rated operating temperature.
5. 150 nseconds maximum at full rated operating temperature.

FUNCTIONAL SPECIFICATIONS

Typical at +25°C, ±15V dc supplies, unless otherwise noted.

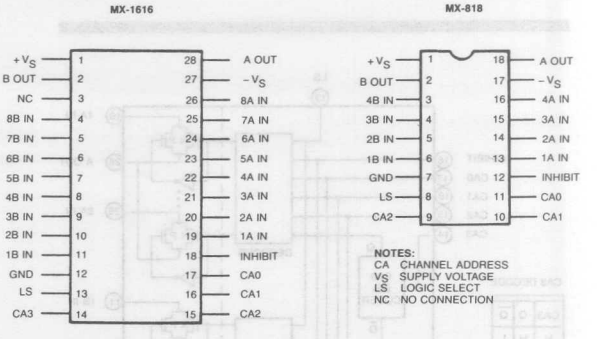
ANALOG INPUTS	MX-1616	MX-818
No. of Channels	16 Single-Ended 8 Differential	8 Single-Ended 4 Differential
Input Voltage Range	±15V	*
Channel ON Resistance, maximum[3]	750Ω	*
Channel ON Res. over Temp., maximum[3]	1 KΩ	*
Channel OFF Input Leakage	10 pA	50 pA
Channel OFF Output Leakage	35 pA	100 pA
Channel ON Leakage	40 pA	100 pA
Channel OFF Input Capacitance	2.5 pF	1.9 pF
Channel OFF Output Capacitance	18 pF	10 pF
DIGITAL INPUTS		
Logic "0" Threshold, maximum: TTL	+0.8V	*
CMOS	+0.3V	*
Logic "1" Threshold, minimum: TTL	+2.4V	*
CMOS	0.7 (Logic sup.)	*
Input Leakage Current, maximum: High	1 μA	*
Low	25 μA	20 μA
Channel Address Coding	4 Bits	3 Bits
Channel Inhibit, All Channels OFF	Logic "0"	*
PERFORMANCE		
Transfer Error, maximum	0.01%	*
Settling Time, 10V step to 0.1%	250 nsec.	*
10V step to 0.01%	800 nsec.	*
Access Time, maximum	150 nsec.[4]	125 nsec.[5]
Enable Delay "ON", maximum	150 nsec.	*
Enable Delay "OFF", maximum	125 nsec.	*
Break Before Make Delay	20 nsec.	*
POWER REQUIREMENTS		
Rated Power Supply Voltage	±15V	*
Quiescent Current maximum	±30 mA	±18 mA
Power Dissipation, maximum	900 mW	540 mW

TECHNICAL NOTES

1. The transfer accuracy of the MX-1616 and MX-818 depends upon both the source and the load resistance. With zero source resistance and assuming 1 KΩ maximum chanel on resistance the load impedance must be at least 10 MΩ to achieve 0.01% accuracy. Source resistance should be kept as low as possible so that accuracy or settling time are not degraded. Less than 500Ω is recommended.

2. Channel expansion is accomplished by the use of the inhibit input of the multiplexers. To expand the number of channels, use multiple multiplexers with the inhibit inputs connected to a decoder.

PIN CONNECTIONS



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CONNECTION & APPLICATION

MX-1616 - USED AS 16 CHANNEL MULTIPLEXER

USE CA3 AS DIGITAL ADDRESS INPUT					CONNECT A OUT TO B OUT ON CHANNEL TO	
3	2	1	0	INHIB.	OUPUT A	OUTPUT B
X	X	X	X	0	NONE	NONE
0	0	0	0	1	1A	____
0	0	0	1	1	2A	____
0	0	1	0	1	3A	____
0	0	1	1	1	4A	____
0	1	0	0	1	5A	____
0	1	0	1	1	6A	____
0	1	1	0	1	7A	____
0	1	1	1	1	8A	____
1	0	0	0	1	____	1B
1	0	0	1	1	____	2B
1	0	1	0	1	____	3B
1	0	1	1	1	____	4B
1	1	0	0	1	____	5B
1	1	0	1	1	____	6B
1	1	1	0	1	____	7B
1	1	1	1	1	____	8B

MX-818 - USED AS 8 CHANNEL MULTIPLEXER

USE CA2 AS DIGITAL ADDRESS INPUT				CONNECT A OUT TO B OUT ON CHANNEL TO	
2	1	0	INHIB.	OUTPUT A	OUTPUT B
X	X	X	0	NONE	NONE
0	0	0	1	1A	____
0	0	1	1	2A	____
0	1	0	1	3A	____
0	1	1	1	4A	____
1	0	0	1	____	1 B
1	0	1	1	____	2 B
1	1	0	1	____	3 B
1	1	1	1	____	4 B

MX-1616 - USED AS DUAL 8 CHANNEL MULTIPLEXER

CONNECT CA3 TO −V SUPPLY				ON CHANNEL TO	
2	1	0	INHIB.	OUTPUT A	OUTPUT B
X	X	X	0	NONE	NONE
0	0	0	1	1A	1B
0	0	1	1	2A	2B
0	1	0	1	3A	3B
0	1	1	1	4A	4B
1	0	0	1	5A	5B
1	0	1	1	6A	6B
1	1	0	1	7A	7B
1	1	1	1	8A	8B

MX-818 - USED AS DUAL 4 CHANNEL MULTIPLEXER

CONNECT CA2 TO −V SUPPLY			ON CHANNEL TO	
1	0	INHIB.	OUTPUT A	OUTPUT B
X	X	0	NONE	NONE
0	0	1	1	1B
0	1	1	2	2B
1	0	1	3	3B
1	1	1	4	4B

ORDERING INFORMATION

MODEL NO.	CHANNELS	OPERATING TEMP. RANGE
MX-818C	8 S.E. or 4 Diff.	0 to +70 °C
MX-1616C	16 S.E. or 8 Diff.	0 to +70 °C

Contact DATEL for up-to-date information on products covered by "Advanced" and "Preliminary" product data sheets.

Dial

1-800-233-2765

for

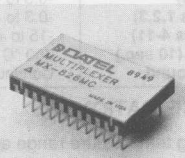
Applications Assistance

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

MX-826
Precision, High-Speed Multiplexer

FEATURES

- **225 nSec. maximum settling time to 0.01%**
- **400 nSec. maximum settling time to 0.003%**
- **150 nSec. maximum settling time to 0.1%**
- **8 Channels single-ended inputs**
- **395 mW Power dissipation**
- **Small 24-pin DDIP package**



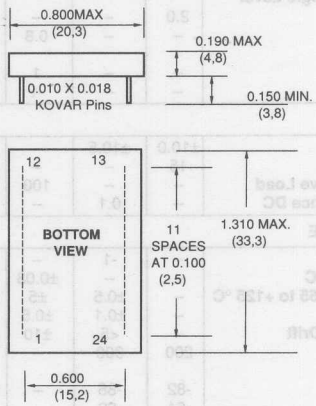
GENERAL DESCRIPTION

The MX-826 is a precision high-speed multiplexer characterized for 10-, 12-, and 14-bit applications. The performance benchmarks are its 225 nanoseconds maximum settling time to 0.01% accuracy and its unprecedented specification of accuracy to 0.003%.

The MX-826 provides eight single-ended inputs. Channel addressing is done by a three-bit binary code. Break-before-make switching assures that no two channels are ever momentarily shorted together.

The MX-826 operates from ±15V and +5V power supplies. Models are available in two operating temperature ranges: 0 to +70 °C and -55 to +125 °C.

MECHANICAL DIMENSIONS
INCHES (mm)



NOTE: Pins have a 0.025 inch, ±0.01 stand-off from case.

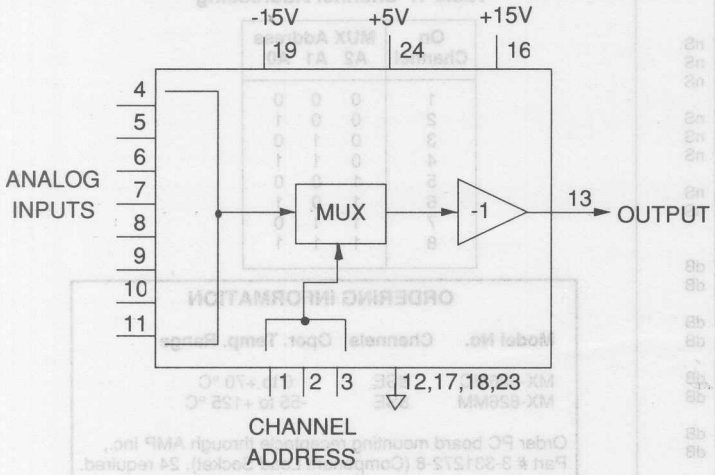


Figure 1. MX-826 Simplified Block Diagram

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	A0	13	OUTPUT
2	A1	14	N/C
3	A2	15	N/C
4	IN1	16	+15V (+V_{CC})
5	IN2	17	GROUND
6	IN3	18	GROUND
7	IN4	19	-15V (-V_{EE})
8	IN5	20	N/C
9	IN6	21	N/C
10	IN7	22	N/C
11	IN8	23	GROUND
12	GROUND	24	+5V (+V_{DD})

ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS
+15V Supply (Pin 16)	0 to +18V dc
-15V Supply (Pin 19)	0 to -18V dc
+5V Supply (Pin 24)	-0.5 to +7V dc
Digital Inputs (Pins 1,2,3)	-0.3 to +5.5V dc
Analog Inputs (Pins 4-11)	-15 to +15V dc
Lead Temperature (10 sec.)	300 °C
Short Circuit to Ground	Continuous

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and over the operating power supply range unless otherwise specified.

INPUTS	MIN	TYP	MAX	UNITS
Input Voltage Ranges	±10.0	±10.5	–	V dc
Digital Input, Logic Level				
Logic 1	2.0	–	–	V dc
Logic 0	–	–	0.8	V dc
Logic Loading				
Logic 1	–	–	1	µA
Logic 0	–	–	-1	µA
OUTPUTS				
Output Range	±10.0	±10.5	–	Volts
Output Current	15	–	–	mA
Stable Capacitive Load	–	–	100	pF
Output Impedance DC	–	0.1	–	Ohms
PERFORMANCE				
Gain	–	-1	–	FS
Gain Error, 25 °C	–	–	±0.03	%FS
Gain Tempco, -55 to +125 °C	–	±0.5	±5	ppm/ °C
Offset, 25 °C	–	±0.1	±0.5	mV
Offset Voltage Drift	–	<5	±10	µV/ °C
Slew Rate	200	300	–	V/µS
Cross Talk				
100 KHz	-82	-86	–	dB
1 MHz	-64	-69	–	dB
Bandwidth				
3 dB Small Signal	8	8.5	–	MHz
Full Power	3	3.5	–	MHz
Input Impedance	2.45	2.5	2.55	KΩ
Output Settling Time				
(10V step, +25 °C) 500Ω Load				
0.1% 10 Bits	–	100	150	nS
0.01% 12 Bits	–	150	225	nS
0.003% 14 Bits	–	300	400	nS
(20V step, +25 °C) 1KΩ Load				
0.1% 10 Bits	–	150	180	nS
0.01% 12Bits	–	200	240	nS
0.003% 14 Bits	–	600	720	nS
Switching Characteristics				
Break before make delay	8	15	25	nS
Turn On/Turn Off	–	20	50	nS
Harmonic Distortion				
DC to 100 KHz, 10V pp				
+25 °C	-90	-92	–	dB
-55 to +125 °C	-88	-92	–	dB
1MHz 10V pp				
+25 °C	-75	-85	–	dB
-55 to +125 °C	-70	-85	–	dB
DC to 100 KHz 20V pp				
+25 °C	-87	-89	–	dB
-55 to +125 °C	-85	-89	–	dB
1MHz to 20V pp				
+25 °C	-72	-83	–	dB
-55 to +125 °C	-67	-83	–	dB
Signal-to-Noise Ratio				
with Distortion	-69	-72	–	dB
without Distortion	-75	-80	–	dB

POWER SUPPLY REQ.	MIN	TYP	MAX	UNITS
Range				
+15V	+14.5	+15	+15.5	Volts
-15V	-14.5	-15	-15.5	Volts
+5V	+4.75	+5	+5.25	Volts
Current (Quiescent)				
+15V	–	+13	+19	mA
-15V	–	-13	-19	mA
+5V	–	<1	+1	mA
Power Supply Reject Ratio	86	–	–	dB
Power Supply Dissipation	–	395	575	mW
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range				
-MC Models	0	–	+70	°C
-MM Models	-55	–	+125	°C
Storage Temp. Range	-65	–	+150	°C
Package Type	24-pin herm. sealed ceramic DIP			
Pin Type	0.010 x 0.018 inch Kovar			
Weight	0.42 oz. (12 gram) maximum			

TECHNICAL NOTES

1. Bypass the ±15V and +5V power supplies with a 1 µF, 25V tantalum electrolytic capacitor in parallel with a 0.1 µF ceramic capacitor.

2. Analog signals up to ±15V may be present while the MUX power supplies are off.

3. The absence of an R_{ON} specification or output leakage specification is related to the architecture of the switching network. The inputs see a constant 2.5 K Ohm input impedance whether the channel is on or off.

4. Typical recovery times from an overvoltage condition of >±3V is approximately 200 nanoseconds from a negative overdrive and 700 nanoseconds from a positive overdrive.

5. Double level multiplexing may be used to provide up to 64 channels (nine MX-826's required).

Table 1. Channel Addressing

On Channel	MUX Address A2	A1	A0
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

ORDERING INFORMATION

Model No.	Channels	Oper. Temp. Range
MX-826MC	8SE	0 to +70 °C
MX-826MM	8SE	-55 to +125 °C

Order PC board mounting receptacle through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 24 required.

For availablilty of MIL-STD-883B version contact DATEL.

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FEATURES

- **50 nSec settling time to 0.01%**
- **70 nSec settling time to 0.003%**
- **100 nSec settling time to 0.001%**
- **4 Channels, single-ended inputs**
- **207 mW power dissipation**
- **Small 14-pin DIP package**

GENERAL DESCRIPTION

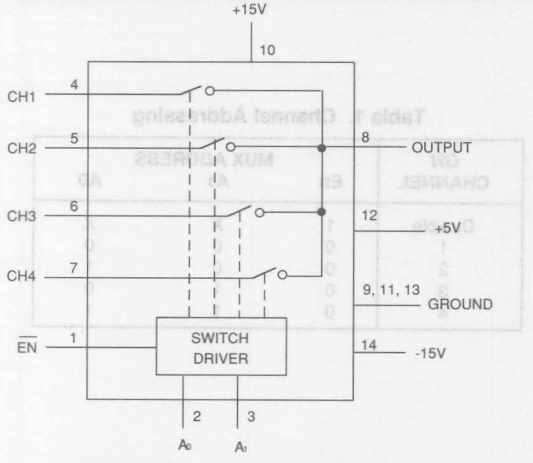
The MX-850 is a precision high-speed multiplexer characterized for 10-, 12-, 14-, and 16-bit applications. The performance benchmarks are its 50 nanosecond maximum settling time to 0.01% accuracy and its unprecedented specification of accuracy to 0.001%.

TECHNICAL NOTES

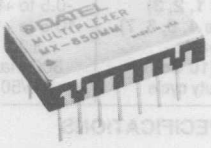
1. Proper operation of the MX-850 multiplexer is dependent upon good board layout and connection practices. Bypass supplies as shown in the connection diagrams. Mount bypass capacitors directly to the supply pins whenever possible.

2. All grounds pins (9, 11, 13) should be tied together and connected to ground as close to the multiplexer as possible.

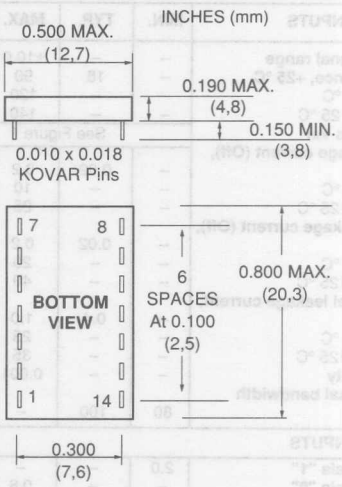
3. When power is off, current limit input signals on pins 4, 5, 6, and 7 to 20 mA. Failure to current limit will cause permanent damage to the device, as when powering up or down, it is possible that two switches might be on at the same time. Excessive current (greater than 20 mA) will flow from the more positive input to the more negative input, permanently damaging the device. Applications where the power supply for the multiplexer also powers the signal sources may not require limiting resistors. See Figure 4.



MX-850 Simplified Block Diagram



MX-850 Mechanical Dimensions



NOTE: Pins have 0.025 Inch ±0.01 stand-off from case.

PIN	FUNCTION
1	$\overline{\text{ENABLE}}$
2	A0
3	A1
4	CH 1 INPUT
5	CH 2 INPUT
6	CH 3 INPUT
7	CH 4 INPUT
8	OUTPUT
9	GROUND
10	+15V
11	GROUND
12	+5V
13	GROUND
14	-15V

ABSOLUTE MAXIMUM RATINGS

PARAMETER	LIMITS	UNITS
+15V Supply (pin 10)	-0.5 to +16.5	Volts
-15V Supply (pin 14)	+0.5 to -16.5	Volts
+5V Supply (pin 12)	-0.5 to +7.0	Volts
Digital inputs (pins 1, 2, 3)	-0.5 to +6.0	Volts
Analog inputs (pins 4, 5, 6, 7)	-10.5 to +10.5	Volts
Analog Input Current	±20	mA
Lead temperature (10 Sec)	300 max.	°C
Switching frequency/duty cycle	10/50	MHz/%

FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and at ±15V and +5V dc unless otherwise specified.

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Analog signal range	–	–	±10.0	Volts
On resistance, +25 °C	–	18	90	Ohm
0 to +70 °C	–	–	120	Ohm
-55 to +125 °C	–	–	140	Ohm
RON versus VIN	See Figure 1			
Input leakage current (Off),				
+25 °C	–	0.02	0.2	nA
0 to +70 °C	–	–	10	nA
-55 to +125 °C	–	–	25	nA
Output leakage current (Off),				
+25 °C	–	0.02	0.2	nA
0 to +70 °C	–	–	20	nA
-55 to +125 °C	–	–	40	nA
On channel leakage current,				
+25 °C	–	0.4	1.0	nA
0 to +70 °C	–	–	25	nA
-55 to +125 °C	–	–	35	nA
Nonlinearity	–	–	0.001	%FSR
Large signal bandwidth				
(-3dB)	80	100	–	MHz
DIGITAL INPUTS				
Logic Levels "1"	2.0	–	–	Volts
Logic Levels "0"	–	–	0.8	Volts
Logic Loading "1"	–	–	1	µA
Logic Loading "0"	–	–	-1	µA
SWITCHING CHARACTERISTICS				
Access time	–	–	20	nS
Break-before-make delay time	–	–	10	nS
Enable delay (On, Off)	–	3	10	nS
Settling time, 10M Load				
(0.1%) 10V step	–	25	30	nS
(0.01%) 10V step	–	40	50	nS
(0.003%) 10V step	–	60	70	nS
(0.001%) 10V step	–	80	100	nS
Settling time, 5K Load				
(0.1%) 10V step	–	25	30	nS
(0.01%) 10V step	–	40	50	nS
(0.003%) 10V step	–	60	70	nS
(0.001%) 10V step	–	80	100	nS
Settling time, 10M Load				
(0.1%) 20V step	–	30	35	nS
(0.01%) 20V step	–	50	60	nS
(0.003%) 20V step	–	75	85	nS
(0.001%) 20V step	–	100	120	nS
Settling time, 5K Load				
(0.1%) 20V step	–	30	35	nS
(0.01%) 20V step	–	50	60	nS
(0.003%) 20V step	–	75	85	nS
(0.001%) 20V step	–	100	120	nS

SWITCHING CHAR. (cont.)	MIN.	TYP.	MAX.	UNITS
Crosstalk ①				
10 KHz (20 Vpp)	–	-105	-100	dB
1 MHz (20 Vpp)	–	-94	-92	dB
10 MHz (5 Vpp)	–	-76	-71	dB
20 MHz (3 Vpp)	–	-64	-62	dB
Chan. input capacitance				
(Off)	–	4	6	pF
(On)	–	10	12	pF
Chan. output capacitance				
(On)	–	8	10	pF
POWER SUPPLY REQUIREMENTS				
Power supply range				
+15V	+14.5	+15	+15.5	Volts
-15V	-14.5	-15	-15.5	Volts
+5V	+4.75	+5	+5.25	Volts
Power supply current, quiescent				
+15V	–	3.0	4.0	mA
-15V	–	10	12	mA
+5V	–	3	3.5	mA
Power sup. rejection ratio	-80	-90	–	dB
Power supply dissipation, quiescent				
+25 °C	–	207	260	mW
0 to +70 °C	–	–	260	mW
-55 to +125 °C	–	–	280	mW
Pd versus frequency	see Figure 3			
PHYSICAL/ENVIRONMENTAL				
Operating temp. range				
-MC	0	–	+70	°C
-MM	-55	–	+125	°C
Storage temp. range	-65	–	+150	°C
Package type				
-MC/MM	14-pin hermetic DIP			
Pin type				
-MC/MM	0.010 x 0.018 inch Kovar			
Weight	0.1 Oz. (3.5 grams) maximum			

① See Figures 2a and 2b.

Table 1. Channel Addressing

ON CHANNEL	MUX ADDRESS En	A1	A0
Disable	1	X	X
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1

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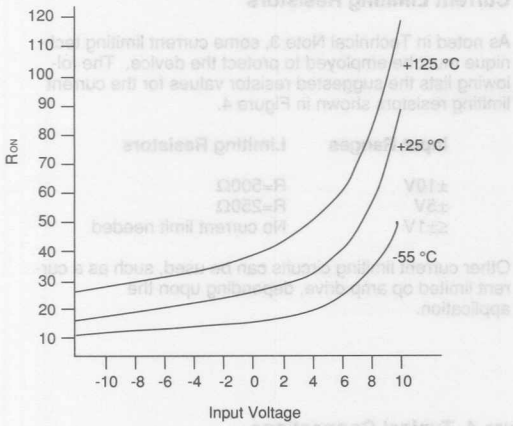

Figure 1. Channel On Resistance Versus Input Voltage

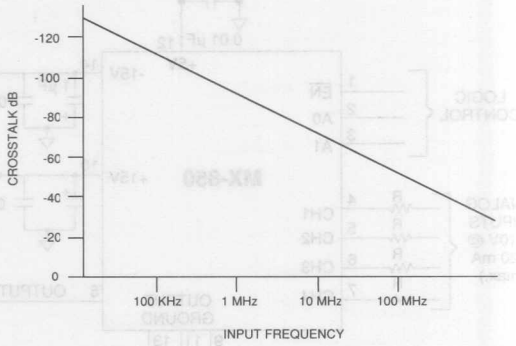

Figure 2a. Small Signal Crosstalk Versus Input Frequency

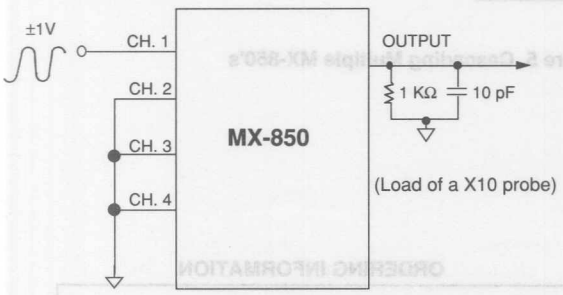

Figure 2b. Crosstalk Test Circuit

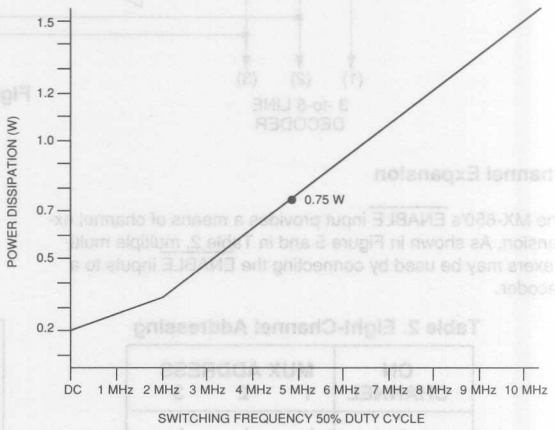

Figure 3. Power Dissipation Versus Switching Frequency

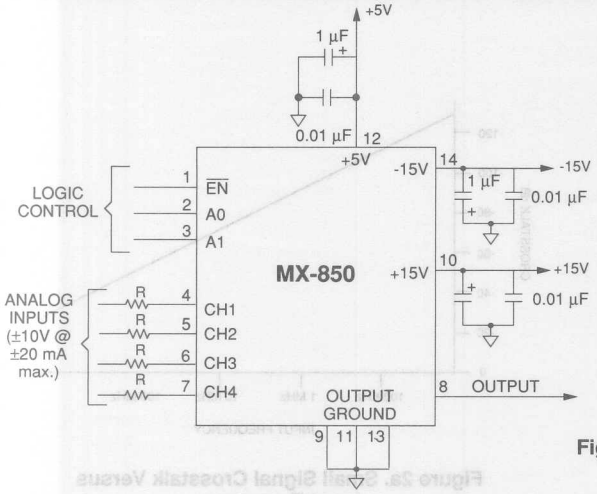

Figure 4. Typical Connections

Current Limiting Resistors

As noted in Technical Note 3, some current limiting technique must be employed to protect the device. The following lists the suggested resistor values for the current limiting resistors shown in Figure 4.

Input Ranges	Limiting Resistors
±10V	R=500Ω
±5V	R=250Ω
≤±1V	No current limit needed

Other current limiting circuits can be used, such as a current limited op amp drive, depending upon the application.

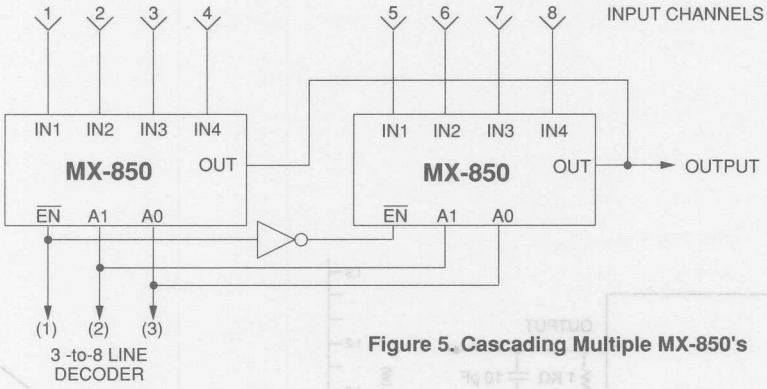

Figure 5. Cascading Multiple MX-850's

Channel Expansion

The MX-850's $\overline{\text{ENABLE}}$ input provides a means of channel expansion. As shown in Figure 5 and in Table 2, multiple multiplexers may be used by connecting the $\overline{\text{ENABLE}}$ inputs to a decoder.

Table 2. Eight-Channel Addressing

ON CHANNEL	MUX ADDRESS 1	2	3
1	L	L	L
2	L	L	H
3	L	H	L
4	L	H	H
5	H	L	L
6	H	L	H
7	H	H	L
8	H	H	H

ORDERING INFORMATION

MODEL NUMBER	OPERATING TEMP. RANGE	SEAL
MX-850MC	0 to +70 °C	Hermetic
MX-850MM	-55 to +125 °C	Hermetic

Receptacle for PC board mounting can be ordered through AMP Inc., Part # 3-331272-8 (Component Lead Socket), 14 required.

For availability of MIL-STD-883B versions of the MX-850, contact DATEL.

OPERATIONAL AMPLIFIERS

Model	DC Open Loop Gain (V/V)	Settling Time (µsec)	Slew Rate (V/µsec)	Gain Bandwidth (MHz)	Case	Page
AM-500	10^6	200 ns/0.01%	1000	100	14-Pin DIP	7-3
AM-1435	10^5	70 ns/0.01%	300	1000	14-Pin DIP	7-1

INSTRUMENTATION AMPLIFIERS

Model	Gain Range	Settling Time	Case	Page
AM-551	1 to 1000	2 µs/0.01%	16-Pin DIP	7-5

RESISTOR TUNEABLE OSCILLATORS

Model	Frequency Range	Accuracy	Case	Page
ROJ-20	20 Hz to 20 KHz	0.5% @ 1 KHz	24-pin DIP	7-7
ROJ-1K	1KHz to 100 KHz	0.5% @ 10 KHz	24-pin DIP	7-7

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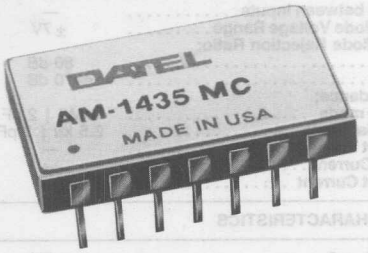
AM-1435

Ultra-High Speed Wideband Operational Amplifier

FEATURES

- **70 Nanoseconds settling to 0.01%**
- **1 GHz Gain bandwidth product**
- **100 dB Open loop gain**
- **80 dB Minimum CMRR**
- **-55°C to +125°C Operation**

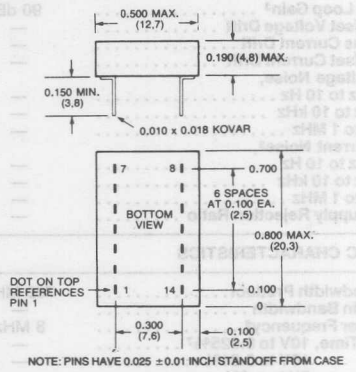


GENERAL DESCRIPTION

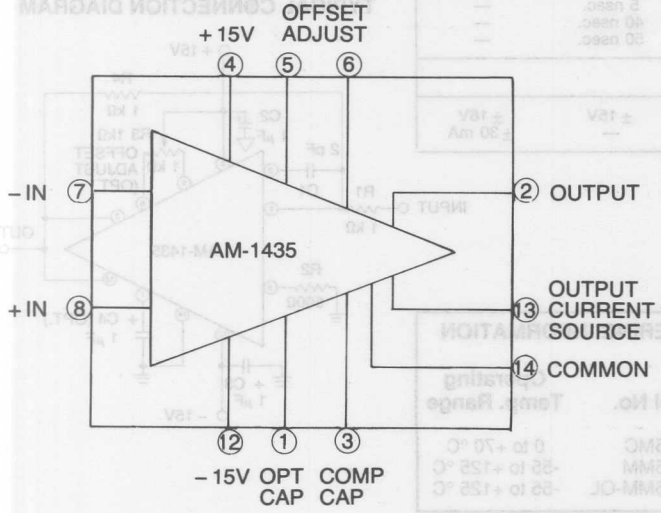
DATEL's AM-1435 is an ultrafast settling, wide-band operational amplifier. Utilizing precision thin-film hybrid construction and differential input operational amplifier design techniques, the AM-1435 achieves a settling time of only 70 nanoseconds for a 10 volt step to 0.01% accuracy. High speed performance is optimized with high open-loop gain, flat frequency response beyond 10 KHz and a roll-off of 6 dB/octave to beyond 100 MHz. Typically, gain bandwidth product is 1 GHz and slew rate is 300 V/microsecond.

AM-1435 dc characteristics include a dc open loop gain of 100 db, 1 MΩ input impedance, and an initial input offset voltage of only ±2 mV. Input offset voltage drift is typically ±5 μV/°C. Also featured is a minimum common mode rejection ratio of 80 dB and full power frequency of 8 MHz.

MECHANICAL DIMENSIONS INCHES (MM)



NOTE: PINS HAVE 0.025 ±0.01 INCH STANDOFF FROM CASE



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	OPTIONAL CAP
2	OUTPUT
3	COMPENSATION CAP.
4	+ 15V SUPPLY (+ V_S)
5	OFFSET ADJUST
6	OFFSET ADJUST
7	– INPUT
8	+ INPUT
9	N.C.
10	N.C.
11	N.C.
12	– 15V SUPPLY (– V_S)
13	OUTPUT CURRENT SOURCE
14	COMMON

FUNCTIONAL SPECIFICATIONS

Typical at +25°C, ±15V dc supplies, unless otherwise noted.

INPUT CHARACTERISTICS	MINIMUM	TYPICAL	MAXIMUM
Differential between inputs	—	—	±4V
Common Mode Voltage Range	±7V	±8.5V	—
Common Mode Rejection Ratio;			
dc	80 dB	—	—
1 MHz	70 dB	—	—
Input Impedance;			
common mode	1 MΩ | 2 pF	—	—
differential mode	2.5 kΩ | 2 pF	—	—
Input Offset Voltage[2]	—	±2 mV	±5 mV
Input Bias Current	—	10 μA	20 μA
Input Offset Current	—	0.3 μA	—
OUTPUT CHARACTERISTICS			
Output Voltage[3]	±5V	±7V	—
Output Current[3]	±10 mA	±14 mA	—
Stable Capacitive Load[4]	—	1000 pF	—
PERFORMANCE			
dc Open Loop Gain[3]	90 dB	100 dB	—
Input Offset Voltage Drift	—	±5 μV/°C	±25 μV/°C
Input Bias Current Drift	—	50 nA/°C	100 nA/°C
Input Offset Current Drift	—	2 nA/°C	—
Input Voltage Noise,			
0.01 Hz to 10 Hz	—	15 μV P-P	—
100 Hz to 10 kHz	—	1.6 μV RMS	—
10 Hz to 1 MHz	—	5.2 μV RMS	—
Input Current Noise[5],			
0.01 Hz to 10 Hz	—	2.5 nA P-P	—
100 Hz to 10 kHz	—	2.5 nA RMS	—
10 Hz to 1 MHz	—	3.5 nA RMS	—
Power Supply Rejection Ratio	—	0.15 mV/V ΔV_S	—
DYNAMIC CHARACTERISTICS			
Gain Bandwidth Product	700 MHz	1000 MHz	—
Unity Gain Bandwidth	—	150 MHz	—
Full Power Frequency[6]	8 MHz	10 MHz	—
Settling Time, 10V to 0.025%[7]	—	60 nsec.	75 nsec.
10V to 0.01%	—	70 nsec.[8]	—
5V to 1.0%	—	25 nsec.	—
5V to 0.1%	—	40 nsec.	60 nsec.
1V to 1.0%	—	10 nsec.	—
1V to 0.1%	—	20 nsec.	—
Slew Rate	250 V/μsec.[6]	300 V/μsec.	
Overshoot	—	—	1%
Propagation Delay	—	5 nsec.	—
Rise Time, 10V Step	—	40 nsec.	—
Overload Recovery Time	—	50 nsec.	—
POWER REQUIREMENTS			
Rated Supply Voltage	±12V	±15V	±16V
Quiescent Current[8]	—	—	±30 mA

PHYSICAL/ENVIRONMENTAL	
Oper. Temp. Range	
AM-1435MC	0 to +70 °C
AM-1435MM[9]/MM-QL	-55 to +125 °C
Storage Temp. Range	-65 to +125 °C
Package	14-pin hermetically sealed ceramic DIP

FOOTNOTES:

1. Specified for dc linear operation. Common mode voltage range prior to fault condition is ±10V dc maximum.
2. Adjustable to zero.
3. R_L = 500Ω.
4. C_1 = 3 pF.
5. Referred to input.
6. C_1 = 0.5 pF.
7. C_f = 1 pF.
8. $\pm V_S$ = ±15V dc.
9. With 18°C/watt heat sink.

ORDERING INFORMATION

Model No.	Operating Temp. Range
AM-1435MC	0 to +70 °C
AM-1435MM	-55 to +125 °C
AM-1435MM-QL	-55 to +125 °C

TECHNICAL NOTES

1. The extensive use of a ground plane for all common connections is recommended. Keep lead length to a minimum with point-to-point connections wired directly to the amplifier pins. Use 1 μF tantalum bypass capacitors the +Vs and -Vs pins.
2. When using the AM-1435MM over the +85 to +125°C temperature range, use an 18°C/W heat sink.
3. Apply negative supply voltage before the positive supply. Power-up prior to applying power to either input. If frequency response is not critical, use an external input protection circuit.

COMPENSATION - The typical connection diagram shows the AM-1435 in a unity gain inverting configuration. Use in any conventional amp circuit, the AM-1435, as a noninverting amplifier, requires a noise gain of at least two (NOISE GAIN = 1 + R_4/R_1).

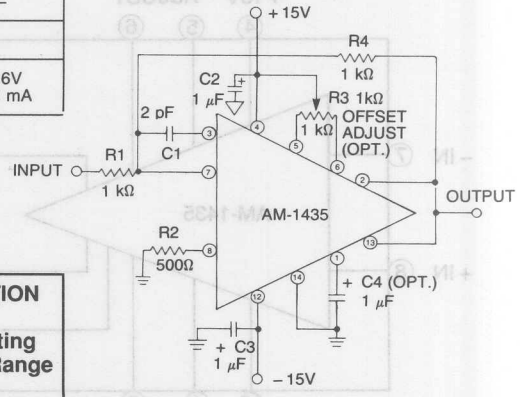
The 2 pF compensation capacitor at C_1 is required for stable operation when the noise gain is less than 10. Compensation for bias current is provided by R_2 and its value determined by the formula

$$R_2 = \frac{(R_1) \times (R_4)}{R_1 + R_4}$$

R_3 and C_4 are optional. Use C_4 when driving capacitive loads to prevent oscillation of the output stage.

When using the AM-1435 at low impedances, include the feedback resistor as a part of the total output load.

TYPICAL CONNECTION DIAGRAM



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AM-500 Series
Ultra-Fast Operational Amplifier

FEATURES

- **200 Nanoseconds settling to 0.01%**
- **1000V/Microsecond slew rate**
- **100 MHz Minimum gain-bandwidth**
- **10^6 Open loop gain**
- **1 Microvolt/°C drift**
- **± 50 mA Output current**

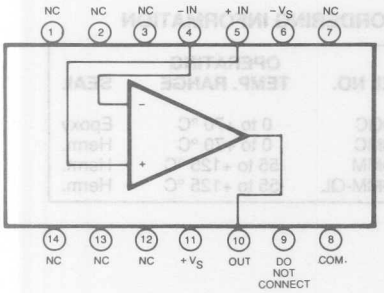
GENERAL DESCRIPTION

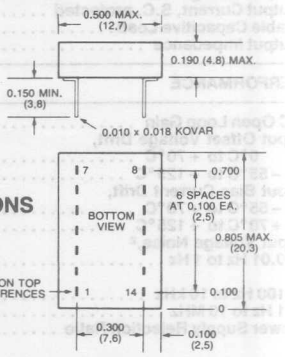
The AM-500 Series amplifiers are ultra-fast settling operational amplifiers for use in inverting applications. A unique feedforward amplifier design combines the characteristics of a low drift dc amplifier with those of a very fast AC amplifier. For optimum fast settling performance, this amplifier has an open loop gain roll-off of 6 dB per octave to beyond 100 MHz.

Output settling time is 200 nanoseconds maximum to 0.01% for a 10 dc volt step change. Slew rate is 1000V/microsecond for positive output transitions and 1800V/microsecond for negative transitions. This high slew rate permits undistorted reproduction of a full load, 20V peak-to-peak sinewave out to 16 MHz. Gain bandwidth product is 100 MHz minimum.

AM-500 series dc characteristics include a dc open loop gain of 10^6, 30 megohm input impedance, and 1 nanoampere bias current. Input offset voltage is ±0.5 mV and input offset voltage drift is 1 microvolt/°C. Although these amplifiers do not operate differentially, a dc offset voltage in the range of ±5V dc can be applied to the positive input terminal.

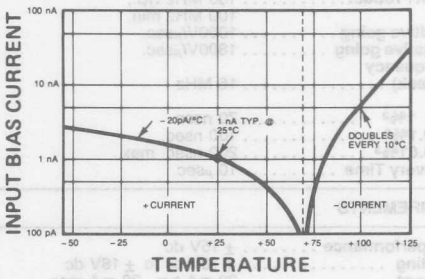
Power supply requirement is ±15V dc at 22 mA quiescent current. The amplifiers will operate over a supply range of ±10V to ±18V dc. Output current capability is ±50 mA with output short circuit protection.





MECHANICAL DIMENSIONS INCHES (MM)

NOTE: PINS HAVE ±0.01 INCH STANDOFF FROM CASE



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	NO CONNECTION
2	NO CONNECTION
3	NO CONNECTION
4	-INPUT
5	+INPUT
6	-SUPPLY
7	NO CONNECTION
8	COMMON
9	DO NOT CONNECT
10	OUTPUT
11	+SUPPLY
12	NO CONNECTION
13	NO CONNECTION
14	NO CONNECTION

FUNCTIONAL SPECIFICATIONS, AM-500 SERIES

Typical at 25°C, ±15V dc supply, unless otherwise noted.

INPUT CHARACTERISTICS	
Input Common Mode Voltage Range[1]	±5V
Maximum Input Voltage, no damage	±18V
Differential Input Impedance	30 Meg. typical, 3 Meg. min.
Input Bias Current	1 nA typical, 4 nA max.
Input Offset Current	0.5 nA typ., 8 nA max.
Input Offset Voltage	0.5 mV typ., 3 mV max.
OUTPUT CHARACTERISTICS	
Output Voltage	±10V min.
Output Current, S.C. protected	±50 mA typ., ±25 mA min.
Stable Capacitive Load	100 pF
Output Impedance	25Ω
PERFORMANCE	
DC Open Loop Gain	10^6 volts/volt
Input Offset Voltage Drift,	
0°C to +70°C	1 μV/°C typ., 5 μV/°C max.
−55°C to +125°C	5 μV/°C typ., 10 μV/°C max.
Input Bias Current Drift,	
−55°C to +70°C	−20 pA/°C
+70°C to +125°C	doubles every 10°C
Input Voltage Noise,[2]	
0.01 Hz to 1 Hz	5 μV peak-to-peak typ., 25 μV peak-to-peak max.
100 Hz to 10 kHz	1 μV RMS typ., 5 μV max.
1 Hz to 10 MHz	20 μV RMS typ., 100 μV max.
Power Supply Rejection Ratio	80 dB min.
DYNAMIC CHARACTERISTICS	
Gain Bandwidth Product	130 MHz typ., 100 MHz min.
Slew Rate, positive going	1000V/μsec.
Slew Rate, negative going	1800V/μsec.
Full Power Frequency (20V peak-to-peak)	16 MHz
Settling Time,	
10V step to 1%[3]	70 nsec.
10V step to 0.1%[3]	100 nsec.
10V step to 0.01%[3]	200 nsec. max.
Overload Recovery Time	10 μsec.
POWER REQUIREMENTS	
Voltage, rated performance	±15V dc
Voltage, operating	±10V dc to ±18V dc
Quiescent Current	22 mA typ., 33 mA max.
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	
AM-500GC	0°C to +70°C
AM-500MC	0°C to +70°C
AM-500MM/MM-QL	−55°C to +125°C
Storage Temperature Range	−55°C to +125°C
Package Type	14 pin ceramic
Pins	0.010x0.018" Kovar
Weight	0.09 ounces (2.5 grams)

FOOTNOTES:

1. dc only
2. −3 dB Single-pole bandwidth
3. 1k Input and feedback resistors, 2.4 pF feedback capacitor

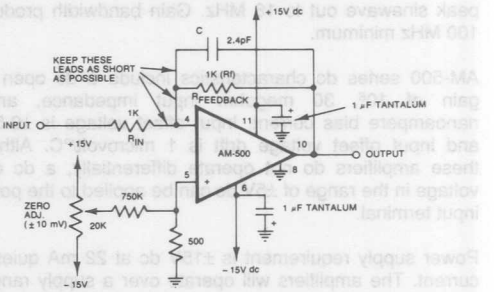
TECHNICAL NOTES

1. The circuit design shows the connection of the AM-500 series for fast settling operation with a closed loop gain of −1. It can be used for fast settling at closed loop gains up to −10. The equivalent resistance seen by the summing junction should be 500 ohms or less. For gains larger than −1 use an input resistor of 500 ohms and pick a feedback resistor for the required closed loop gain (1k for −2, 1.5k for −3, etc.).
2. A small feedback capacitor should be used across the feedback resistor. Determine C in nanofarads from the following formula:

$$C = \frac{1 + |G|}{0.816Rf}$$

   where G is closed loop gain and Rf is in kilohms.
3. Summing point leads must be kept as short as possible. Input and feedback resistors should be soldered close to the body of the resistor directly to the summing point (pin 4). Summing point capacitance to ground must be kept very low.
4. Low output impedance power supplies should be used with 1 μF tantalum bypassing capacitors at the amplifier supply terminals. There are internal 0.03 μF ceramic capacitors in the amplifier.
5. Although these amplifiers are inverting mode only, a dc voltage in the range of ±5V may be applied to the positive input terminal for offsetting the amplifier.
6. For interrupted power applications, apply power to the AM-500 three (3) seconds before operating the device.

CONNECTION FOR FAST SETTLING WITH GAIN OF −1



ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE	SEAL
AM-500GC	0 to +70 °C	Epoxy
AM-500MC	0 to +70 °C	Herm.
AM-500MM	-55 to +125 °C	Herm.
AM-500MM-QL	-55 to +125 °C	Herm.

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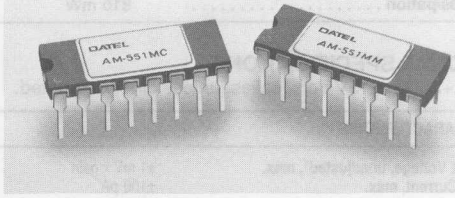
AM-551

Low Cost, Programmable Gain Instrumentation Amplifier

FEATURES

- 1 to 1000 Gain range
- ±0.01% Maximum nonlinearity
- 2 Microseconds settling time
- 100 dB CMRR



GENERAL DESCRIPTION

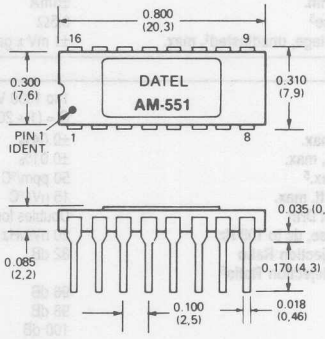
DATEL's AM-551 is a low cost, high performance, programmable gain instrumentation amplifier manufactured with hybrid thin-film technology. Gain is adjustable over a range of 1 to 1000 by the addition of a single external resistor and a simple user-selectable pin-strapping option. Maximum gain nonlinearity is ±0.01%.

The AM-551 dynamic characteristics include a settling time of 2 microseconds for a 20V dc output step to 0.01% accuracy. Slew rate is 23V dc/microsecond and small signal bandwidth is 400 KHz. Other specifications include a common mode rejection ration of 100 dB, a $10^{12}\Omega$ input impedance and a minimum output voltage swing of ±11V dc. Maximum offset voltage drift is ±15 microvolts/°C.

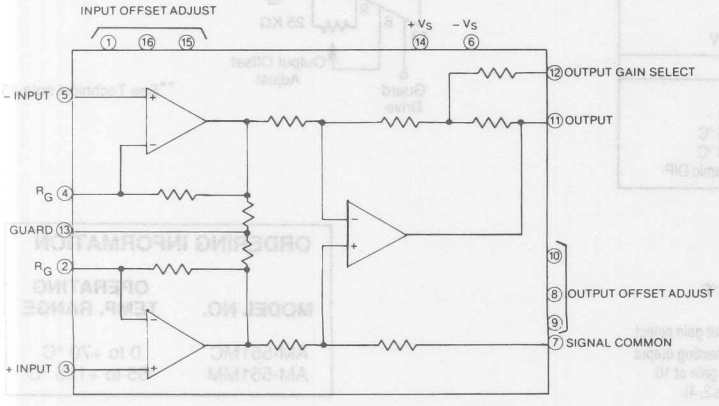
The combination of high accuracy, speed, low cost, and rugged hybrid construction make the AM-551 and ideal choice for applications involving the remote amplification of low-level signals produced by thermocouples, strain gages and RTD's, high performance data acquisition systems and remote instrumentation systems.

Power requirement is ±15V dc and all devices are cased in miniature, hermetically sealed, 16-pin ceramic packages. Models are available for operation over the commercial, 0°C to +70°C, and military, -55°C to +125°C operating temperature ranges.

MECHANICAL DIMENSIONS INCHES (MM)



16-PIN CERAMIC DIP



PIN	FUNCTION
1	INPUT OFFSET ADJUST
2	R_G (Gain Resistor)
3	+ INPUT
4	RG (Gain Resistor)
5	– INPUT
6	$-V_S$
7	SIGNAL COMMON
8	OUTPUT OFFSET ADJ. WIPER
9	OUTPUT OFFSET ADJUST
10	OUTPUT OFFSET ADJUST
11	OUTPUT
12	OUTPUT GAIN SELECT
13	GUARD
14	$+V_S$
15	INPUT OFFSET ADJUST
16	INPUT OFFSET ADJ. WIPER

ABSOLUTE MAXIMUM RATINGS	
Positive Supply, Pin 14	+18V
Negative Supply, Pin 6	−18V
Input Voltage Range	±18V
Differential Input Voltage Range	±30V
Output Short Circuit	Continuous
Power Dissipation	810 mW

FUNCTIONAL SPECIFICATIONS

Typical at +25 °C, ±15V dc supplies, unless otherwise noted.

INPUT CHARACTERISTICS	
Input Offset Voltage, unadjusted[1], max.	±1 mV x gain
Input Bias Current, max.	±100 pA
Input Offset Current, max.	±20 pA
Input Impedance, Diff. or Com. Mode	$10^{12}\Omega$
Common Mode Voltage Range, min.	±11V
OUTPUT CHARACHTERISTICS	
Output Voltage Range, min. (R_L = 2kΩ	±11V
Output Current, min.	±5mA
Output Impedance[3]	0.5Ω
Output Offset Voltage, unadjusted[1], max.	±1 mV x gain
PERFORMANCE	
Gain Range[4]	1 to 1000 V/V
Gain Equation[7]	$G = (1 + 20k/R_G)G_2$
Gain Accuracy, max.	±0.04%
Gain Nonlinearity, max.	±0.01%
Gain Tempco, max.[5]	50 ppm/°C
Offset Voltage Drift, max.	15 µV/ °C
Input Bias Current Drift	Doubles for every 10 °C
Input Voltage Noise, dc to 100 Hz	20 nV/√Hz
Power Supply Rejection Ratio	82 dB
Common Mode Rejection Ratio[6]	
1 KHz	96 dB
100 Hz	98 dB
dc	100 dB
Slew Rate	23V/µS
Small Signal Response, (-3 dB)	
G = 1,10	600 KHz
G = 50	200 KHz
G = 100	100 KHz
G = 1000	40 KHz
Settling Time, 20V to 0.01%	
G = 1	3.0 µS
G = 10	4.0 µS
G = 50	11 µS
G = 100	20 µS
G = 1000	200 µS
POWER REQUIREMENTS	
Rated Power Supply Voltage	±15V dc
Supply Current, max.	±27 mA
Power Supply Range	±5V to ±18V
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	
MC	0 to +70 °C
MM	-55 to +125 °C
Storage Temperature Range	-65 to +150 °C
Package Type	16 pin Ceramic DIP

Footnotes:

1. Adjustable to zero.
3. At 1 KHz, for all gain ranges.
4. To 0.01% accuracy. Higher gains degrade performance
5. Tempco of R_G = ±0 ppm/ °C. For R_G = ∞, Gain Tempco = 5 ppm/ °C
6. 1 kΩ Source Imbalance
7. G_2 is the gain of the second stage of the AM-551. Connecting output gain select (pin 12) to the output (pin 11) sets the second stage gain at 1. Connecting output gain select (pin 12) to signal common (pin 7) sets the second stage gain at 10. R_G is the gain resistor for the first stage and is connected to R_G (pins 2, 4).

TECHNICAL NOTES

1. A 25 kΩ trimpot may be used for both input and output offset adjusts. The trimpot is connected across the input offset adjust pins (Pins 1, 15) and the wiper is connected to Pin 16.

   For output offset adjust, the trimpot is connected across the output offset adjust pins (Pins 10, 9) with the wiper connected to Pin 8.

2. For unity gain, R_G is left open and the output gain select pin (Pin 12) is tied to the output pin (Pin 11). To avoid oscillation in the unity gain configuration, the connection between the output gain select pin and the output pin should be kept as short as possible.

3. Gain selection is accomplished in two stages. The input stage gain (G_1) is selected by an external gain resistor (R_G) connected across the (R_G) pins, (Pins 2, 4) and is expressed as follows:

$$G_1 = 1 + \frac{20k}{R_G}$$

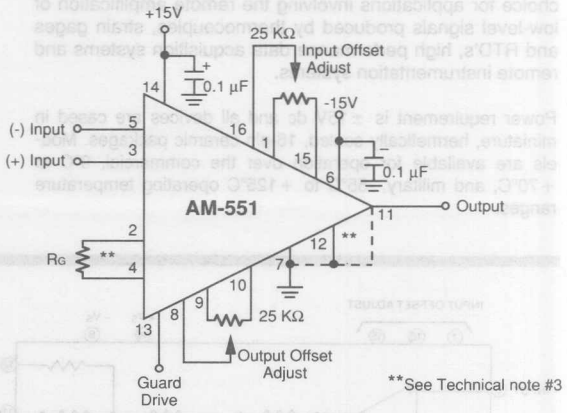
   The output stage gain (G_2) is selected by external pin-strapping: For G_2 = 1, connect the gain select pin (Pin 12) to the output pin (Pin 11). For G_2 = 10, connect the gain select pin (Pin 12) to the signal common pin (Pin 7).

   The total gain of the amplifier is as follows:

$$G_t = G_1 \times G_2 = \left(1 + \frac{20k}{R_G}\right) G_2$$

4. Both power supplies should be bypassed to ground with 0.1 microfarad electrolytic capacitors.

TYPICAL CONNECTION DIAGRAM



ORDERING INFORMATION	
MODEL NO.	OPERATING TEMP. RANGE
AM-551MC	0 to +70 °C
AM-551MM	-55 to +125 °C

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

ROJ-20, 1K
Resistor Tuneable Oscillator

FEATURES

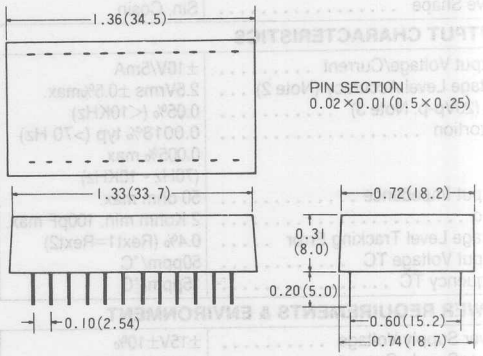
- **Oscillation frequency is set by two external resistors**
- **Ultra low distortion: 0.0018% typical**
- **Stable**
- **Hybrid, small**

GENERAL DESCRIPTION

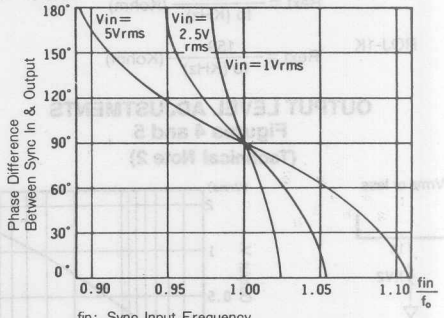
ROJ-20 and ROJ-1K are resistor tuneable oscillators whose oscillation frequency is set with two external resistors. Output frequency range of ROJ-20 is 20Hz to 20KHz while that of ROJ-1K is 1KHz to 100KHz. Output distortion is as low as 0.0018% typical at 1KHz frequency range. Output voltage temperature coefficiency is also as low as 50ppm/°C. Output voltage amplitude is internally trimmed at 2.5Vrms ±0.5% and this amplitude is adjusted to the range from 500mV to 20Vp-p with external resistors. Sine and cosine waves are generated from two output terminals. A synchronization input terminal is provided in order to fine tune the relationship of these two outputs.

Hybrid construction has made it possible to build highly stable oscillators in small size at low cost.

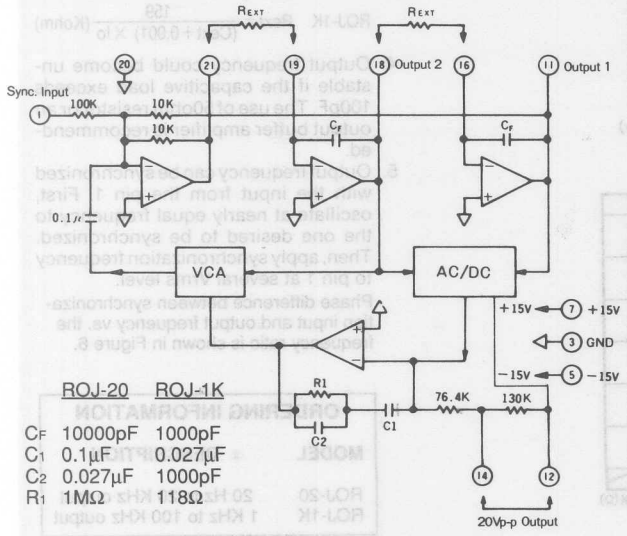
MECHANICAL DIMENSIONS
INCHES (mm)



PHASE DIFFERENCE BETWEEN SYNC INPUT AND OUTPUT
(Fig. 6) (Technical Note 5)



fin: Sync Input Frequency
fo: Frequency when no Sync In is given.



	ROJ-20	ROJ-1K
C_F	10000pF	1000pF
C_1	0.1μF	0.027μF
C_2	0.027μF	1000pF
R_1	1MΩ	118Ω

PIN CONNECTIONS

PIN	FUNCTION
1	SYNCHRONIZATION INPUT
3	GND
5	−15V POWER SUPPLY
7	+15V POWER SUPPLY
11	OUTPUT 1
12	20Vp-p
14	20Vp-p
16	REXT
18	OUTPUT 2 (-90°)
19	REXT
20	GND
21	REXT

DO NOT CONNECT UNUSED PINS

SPECIFICATIONS

Typical value at 25°C with ±15VDC supplies unless otherwise specified.

	ROJ-20	ROJ-1K
OSCILLATED FREQUENCY		
Frequency Range (Note 1)	20Hz - 20KHz	1KHz - 100KHz
Accuracy, Calculated Frequency	0.5%@1KHz	0.5%@10KHz
Wave Shape	Sin, Cosin	* Same as left
OUTPUT CHARACTERISTICS		
Output Voltage/Current	±10V/5mA	*
Voltage Level Accuracy (Note 2)	2.5Vrms ±0.5%max.	*
" (20Vp-p, Note 3)	0.05% (<10KHz)	0.1% (<50KHz)
Distortion	0.0018% typ (>70 Hz)	*
	0.005% max.	* (2KHz - 50KHz)
	(70Hz - 10KHz)	0.01% max. (>50KHz)
Output Impedance	50 ohm max.	*
Load	2 Kohm min. 100pF max.	*
Voltage Level Tracking Error	0.4% (Rext1=Rext2)	*
Output Voltage TC	50ppm/°C	*
Frequency TC	15ppm/°C	25ppm/°C
POWER REQUIREMENTS & ENVIRONMENT		
Power Supply Voltage	±15V±10%	*
Power Supply Current	+14mA, -21mA	*
Operating Temperature Range	-20°C to +70°C	*
Storage Temperature Range	-30°C to +80°C	*
Relative Humidity	10% to 95% Non Condensing	*

Note 1. Two external resistors are:

ROJ-20 $Rext = \frac{15.9}{fo\ (KHz)}$ (Kohm)

ROJ-1K $Rext = \frac{159}{fo\ (KHz)}$ (Kohm)

Note 2. Pins 12 and 14 OPEN.

Note 3. Pins 12 and 14 CONNECTED.

OUTPUT LEVEL ADJUSTMENTS
Figures 4 and 5
(Technical Note 2)

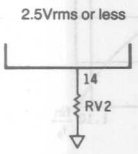


Figure 4a.

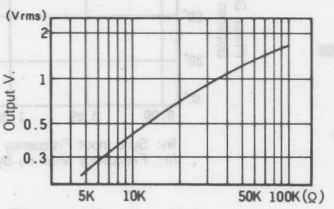


Figure 4b.

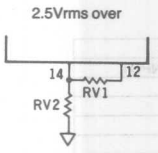


Figure 5a.

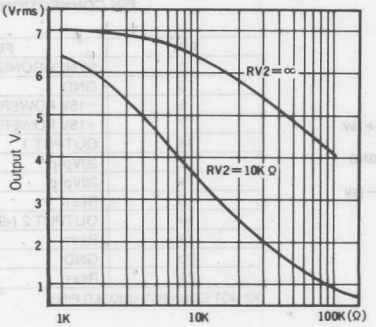
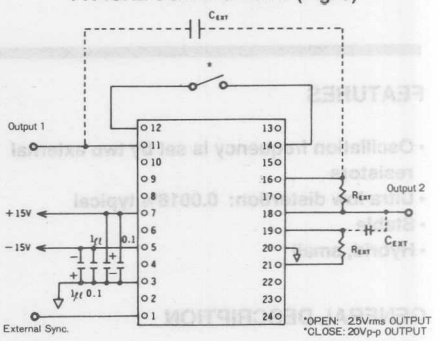


Figure 5b.

TYPICAL CONNECTIONS (Fig. 3)



TECHNICAL NOTES

1. Typical connections are shown in Figure 3. Do not connect unused pins to any points. The external synchronization pin (Pin 1) is left open normally.
2. Output voltage level is 20Vp-p when the pins 12 and 14 are connected, 2.5Vrms when these pins are disconnected.
   Any output voltage level can be set using external resistors RV1 and RV2 as shown Figure 4-a and 5-a.
   The curves 4-b and 5-b show approximate values. The use of potentiometers are recommended when an accurate level of output is desired.
3. Output frequency can be slightly shifted toward lower frequency range if two Cext are added. See Figure 3.
   Relationship among Rext, Cext and fo are:

   ROJ-20 $Rext = \frac{159}{(Cext + 0.01) \times fo}$ (Kohm)

   Cext : μF fo : Hz

   ROJ-1K $Rext = \frac{159}{(Cext + 0.001) \times fo}$ (Kohm)
4. Output frequency could become unstable if the capacitive load exceeds 100pF. The use of 50ohm resistor or an output buffer amplifier is recommended.
5. Output frequency can be synchronized with the input from the pin 1. First, oscillate at nearly equal frequency to the one desired to be synchronized. Then, apply synchronization frequency to pin 1 at several Vrms level.
   Phase difference between synchronization input and output frequency vs. the frequency ratio is shown in Figure 6.

ORDERING INFORMATION

MODEL	DESCRIPTION
ROJ-20	20 Hz to 20 KHz output
ROJ-1K	1 KHz to 100 KHz output

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TUNABLE ACTIVE FILTERS

Model	Poles	Low Pass	High Pass	Band Pass	Band Reject	Rolloff (dB/Oct)	Frequency Cutoff Range (FC)	Filter Type	Gain	Case	Page
FLT-DL41*	4	♦				30	100 to 400KHz	CA	+1	32 DIP	8-25
FLT-DL42*	4	♦				30	250 to 1000 KHz	CA	+1	32 DIP	8-25
FLT-DL51*	5	♦				50	120 to 470 KHz	CA	+1	32 DIP	8-25
FLT-DL52*	5	♦				50	300 to 1200KHz	CA	+1	32 DIP	8-25
FLT-DL41/DL51 § *	7	♦				50	100 to 400KHz	CA	+1	2-32 DIP	8-25
FLT-DL42/DL52 § *	7	♦				50	0.25 to 1.0MHz	CA	+1	2-32 DIP	8-25
FLT-C1	7	♦				52	78 Hz-20 KHz	CH	1, 2, 4, 8	32 DIP	8-21
FLJ-DC	2	♦	♦	♦	♦	12	1 Hz-159 KHz	BU,CH,BE	1 ~ 10	40 QDIP	8-5
FLJ-D1	2	♦	♦	♦	♦	12	1 Hz-1.599 KHz	BU	1 ~ 10	40 QDIP	8-5
FLJ-D2	2	♦	♦	♦	♦	12	100 Hz-159.9 KHz	BU	1 ~ 10	40 QDIP	8-5
FLJ-D5LA1	5	♦				60	10 Hz-2 KHz	CA	0 ±0.3 dB max	40 QDIP	8-9
FLJ-D5LA2	5	♦				60	100 Hz-20 KHz	CA	0 ±0.3 dB max	40 QDIP	8-9
FLJ-D6LA1	6	♦				80	10 Hz-2 KHz	CA	0 ±0.3 dB max	40 QDIP	8-9
FLJ-D6LA2	6	♦				80	100 Hz-20 KHz	CA	0 ±0.3 dB max	40 QDIP	8-9
FLJ-VB	2			♦		12	200Hz-20KHz	BU	±1dB	40 QDIP	8-12
FLJ-VH	4		♦			24	20Hz-20KHz	BU	±0.5dB	40 QDIP	8-17
FLJ-VL	4	♦				24	100Hz-100KHz	BU	±0.5dB	40 QDIP	8-17
FLJ-R3BA1	3			♦		—	10Hz-2KHz	CA	0 ±1dB max	40 QDIP	8-11
FLJ-R3BA2	3			♦		—	100Hz-20KHz	CA	0 ±1dB max	40 QDIP	8-11
FLJ-R8LA1	8	♦				135	10Hz-2KHz	CA	0 ±0.1dB max	40 QDIP	8-11
FLJ-R8LA2	8	♦				135	100Hz-20KHz	CA	0 ±0.1dB max	40 QDIP	8-11
FLJ-R8LB1	8	♦				100	10Hz-2KHz	CA	0 ±0.1dB max	40 QDIP	8-11
FLJ-R8LB2	8	♦				100	100Hz-20KHz	CA	0 ±0.1dB max	40 QDIP	8-11
FLJ-UR1BA1	1			♦		—	40Hz-1.6KHz	BU	0 ±1dB	20 SIP	8-13
FLJ-UR2BA1	2			♦		--	40Hz-1.6KHz	BU	0 ±1dB	20 SIP	8-13
FLJ-UR2EA1	2				♦	—	40Hz-1.6KHz	BU	0 ±0.3dB	20 SIP	8-13
FLJ-UR2LH1	2	♦	♦			12	40Hz-1.6KHz	BU	0 ±0.3dB	20 SIP	8-13
FLJ-UR4HA1	4		♦			24	40Hz-1.6KHz	BU	0 ±1dB	20 SIP	8-13
FLJ-UR4HB1	4		♦			42	40Hz-1.6KHz	CH	0 ±1dB	20 SIP	8-13
FLJ-UR4LA1	4	♦				24	40Hz-1.6KHz	BU	0 ±0.3dB	20 SIP	8-13
FLJ-UR4LB1	4	♦				42	40Hz-1.6KHz	CH	0 ±0.3dB	20 SIP	8-13
FLJ-UR1BA2	1			♦		—	400Hz-10KHz	BU	0 ±1dB	20 SIP	8-13
FLJ-UR2BA2	2			♦		--	400Hz-10KHz	BU	0 ±1dB	20 SIP	8-13
FLJ-UR2EA2	2				♦	—	400Hz-10KHz	BU	0 ±0.3dB	20 SIP	8-13
FLJ-UR2LH2	2	♦	♦			12	400Hz-20KHz	BU	0 ±0.3dB	20 SIP	8-13
FLJ-UR4HA2	4		♦			24	400Hz-5KHz	BU	0 ±1dB	20 SIP	8-13
FLJ-UR4HB2	4		♦			42	400Hz-5KHz	CH	0 ±1dB	20 SIP	8-13
FLJ-UR4LA2	4	♦				24	400Hz-20KHz	BU	0 ±0.3dB	20 SIP	8-13
FLJ-UR4LB2	4	♦				42	400Hz-20KHz	CH	0 ±0.3dB	20 SIP	8-13
FLT-U2	2	♦	♦	♦		12	0.001Hz-200KHz	BU,CH,BE,CA	0.1-1000	16 DIP	8-29

BU = Butterworth BE = Bessel
CH = Chebyshev CA = Cauer/Elliptical

All Filters operate over the commercial temperature range -20°C to +70°
Model FLT-U2 also operates at -55°C to +125°C
§ Cascaded Pair * Preliminary

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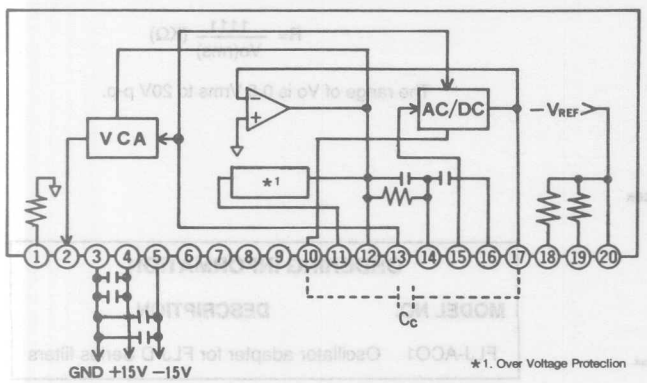
FLJ-ACO1
Oscillator Adaptor for FLJ-D Series

FEATURES

- **Output 2.5Vms ±0.5% accuracy**
- **500mV ~ 20Vp-p wide amplitude range**
- **Single inline small package**

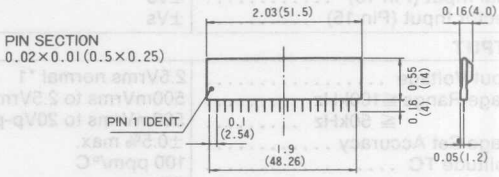
GENERAL DESCRIPTION

FLJ-ACO1 is an accessory used with the FLJ-D1, D2 and DC filters to build a digitally programmable oscillator. The oscillator is controlled with 3 digits of BCD logic input. The setting method, set frequency accuracy and TC depend on the filters which are to be used with this FLJ-ACO1, but the specifications related to output voltage such as output voltage accuracy, stability and amplitude TC are determined by the FLJ-ACO1. The output voltage is trimmed internally to provide 2.5Vrms ±0.5% output.

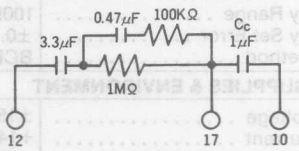


★1. Over Voltage Protection

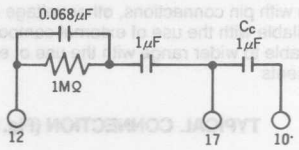
MECHANICAL DIMENSIONS
INCHES (mm)



FLJ-D1 FOR LOWER FREQUENCY (Fig. 4)

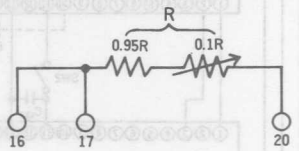


FLJ-DC FOR LOWER FREQUENCY (Fig. 5)



Note: FLJ-D1 or FLJ-DC with 5000pF of Cext for lower than 10Hz oscillation, use one of these circuits.

OUTPUT VOLTAGE ADJUSTMENT (Fig. 6)



PIN CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	Rq	11	OUTPUT PROTECTION
2	LOOP OUTPUT	12	COMPENSATION 1
3	GND	13	SUB (-90°) OUTPUT
4	+15V Supply	14	COMPENSATION 3
5	−15V Supply	15	MAIN OUTPUT
6	NC	16	−Vref IN
7	NC	17	COMPENSATION 2
8	NC	18	OUTPUT RANGE 1
9	NC	19	OUTPUT RANGE 2
10	Cext	20	−Vref OUT

DO NOT CONNECT NC PINS
PIN 14 SHOULD BE LEFT OPEN NORMALLY.

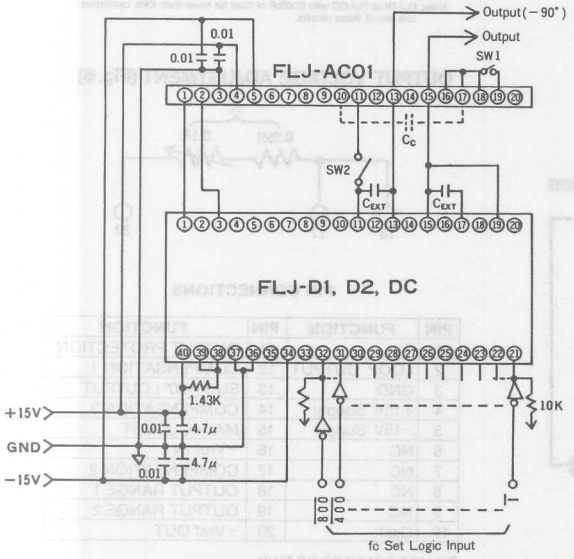
SPECIFICATIONS

Typical at 25 °C, with ±15V power supplies unless otherwise specified.

ABSOLUTE RATINGS	
Power Supply Voltage (±Vs)	±18V
Signal Input (Pin 13)	±Vs
Detector Input (Pin 15)	±Vs
OUTPUT	
Output Voltage	2.5Vrms normal *1
Voltage Range ≦100kHz	500mVrms to 2.5Vrms
≦ 50kHz	500mVrms to 20Vp-p
Voltage Set Accuracy	±0.5% max.
Amplitude TC	100 ppm/°C
Output Resistance	5Ω max.
Distortion	0.01%@10kHz
Sub Output	−90° phase of Main
FREQUENCY	
Frequency Range	100Hz to 100kHz *2
Frequency Set Error	±0.1%
Setting Method	BCD 3 digits
POWER SUPPLIES & ENVIRONMENT	
Supply Voltage	±15V ±10%
Supply Current	+14mA, −24mA
Operating Temperature Range	−20°C to 70°C
Storage Temperature Range	−30°C to 80°C
Operating/Storage Humidity	10% to 95%/80% RH

*1. 20V p-p with pin connections, other voltage output ranges are available with the use of external components.
*2. Expandable to wider range with the use of external components

TYPICAL CONNECTION (Fig. 3)



Note 1. Open SW1 and SW2 for 2.5VrmS output. Close SW1 and SW2 for 20Vp-p output.
2. Two Cext are required for FLJ-DC.

TECHNICAL NOTES

1. Oscillation frequency range varies depending on the Digital Tuneable Filter to be used with FLJ-ACO1.
   FLJ-D1 1 Hz ~ 1.599 KHz
   FLJ-D2 100 Hz ~ 159.9 KHz
   FLJ-DC Determined by external capacitors
   Any model can be used connected as shown in Figure 3 to get the performance that meets the values shown in the specification table.

2. FLJ-DC needs two external capacitors. The relationship between capacitance and oscillation frequency fc is:

$$fc = \frac{N}{20 \cdot Cext}$$ fc: Hz, Cext: μF, N: Digital Number

   For example, once Cext of 0.005 μF and N of 1000 are given, fc shall be 10 KHz. Therefore, with N of 1 to 1599, fc can be set at any frequency of 10 Hz to 15.99 KHz range with BCD logic inputs.

3. Expansion to higher frequency range: The maximum frequency is 50 KHz for 20V p-p output even if FLJ-D2 is used. Connect pin 11 of both FLJ-DC and FLJ-ACO1 together to expand the oscillation frequency range to higher levels. Up to 100 KHz of frequency range is obtained for 20V p-p amplitude even though distortion ratio is slightly derated as the protection circuit in FLJ-ACO1 works. Up to 159.9 KHz of oscillation shall be available for 2.5 Vrms output with the same connection.

4. Distortion at lower frequency range shall be improved with the addition of a few external components.
   a. With the FLJ-D1 connect as shown in Figure 4. As little as 0.01% distortion can be attained at 4 Hz oscillation.
   b. With the FLJ-DC, Cext = 5000 pF connect as shown in Figure 5. Distortion at 10 Hz shall be improved to 0.005%.

5. Adjustment of output voltage: Normal 2.5 Vrms output voltage is obtained with SW1 of Figure 3 open and 20V p-p is obtained with SW1 closed. For other output voltage, follow Figure 6 and the following equation.

$$R = \frac{1111}{Vo(rms)}\ (K\Omega)$$

   The range of Vo is 0.5 Vrms to 20V p-p.

ORDERING INFORMATION

MODEL NO.	DESCRIPTION
FLJ-ACO1	Oscillator adapter for FLJ-D Series filters

DATEL, Inc. 11 Cabot Boulevard, Mansfield. MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

FLJ-ACR1, 2
Logic Controlled Resistor Network

FEATURES

- **Cutoff frequency of resistor tuneable filters can be set with BCD logic.**
- **Single inline hybrid.**
- **Small size, low cost**

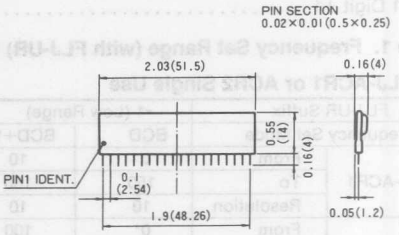
GENERAL DESCRIPTION

FLJ-ACR series are logic controlled resistor networks. They are designed to be used with resistor tuneable filters such as FLJ-UR series.

Four separate resistor networks are included in one package. One network consists of four resistors such as R, R/2, R/4 and R/8. The value of R in FLJ-ACR1 is 1.59MΩ while that of FLJ-ACR2 is 150kΩ.

A combination of an FLJ-ACR and an FLJ-UR makes it possible to make a filter whose cutoff frequency or center frequency is set with BCD logic. It is also possible to use this resistor network in the negative feedback loop of an amplifier circuit and control the gain with BCD logic.

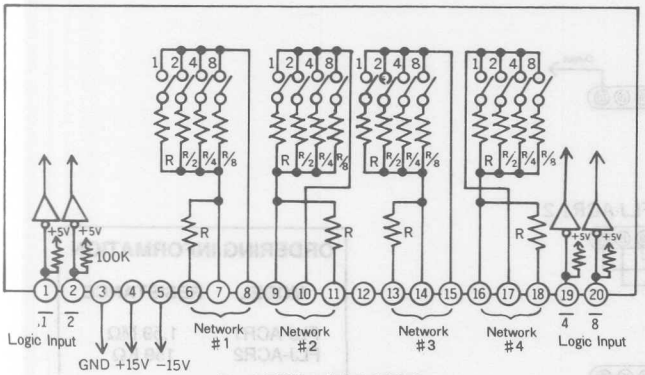
MECHANICAL DIMENSIONS (Fig. 2)
INCHES (mm)



FLJ-UR Series List

Model No.	fc Range	No. of Pole	Type
FLJ-UR4LA1		4	LP, Butt.
FLJ-UR4LB1		4	LP, Cheb.
FLJ-UR4HA1		4	HP, Butt.
FLJ-UR4HB1	40Hz ~	4	HP, Cheb.
FLJ-UR2LH1	1.6KHz	2	LP/HP, Butt.
FLJ-UR1BA1		1 pair	BP, Butt.
FLJ-UR2BA1		2 pair	BP, Butt.
FLJ-UR2EA1		2 pair	BE, Butt.
FLJ-UR4LA2		4	LP, Butt.
FLJ-UR4LB2		4	LP, Cheb.
FLJ-UR4HA2		4	HP, Butt.
FLJ-UR4HB2	400Hz ~	4	HP, Cheb.
FLJ-UR2LH2	20KHz	2	LP/HP, Butt.
FLJ-UR1BA2		1 pair	BP, Butt.
FLJ-UR2BA2		2 pair	BP, Butt.
FLJ-UR2EA2		2 pair	BE, Butt.

LP: Lowpass — BE: Band elimination
HP: Highpass — Butt.: Butterworth
BP: Bandpass — Cheb.: Chebychev



R=1.59MΩ (FLJ-ACR1)
R= 159kΩ (FLJ-ACR2)

SPECIFICATIONS

Typical at 25°C, ±15VDC power supplies unless otherwise specified.

ABSOLUTE RATINGS

Power Supply Voltage (±Vs) ..... ±18V
Input Signal Voltage ..... ±Vs
Control Logic Voltage ..... +5.5Vmax., -0.5V min.

FREQUENCY SET MODE

BCD 1 Digit ..... 0 to 15
BCD 1 Digit +1 ..... 1 to 16

Table 1. Frequency Set Range (with FLJ-UR) Unit: Hz

1a. FLJ-ACR1 or ACR2 Single Use

FLJ-UR Suffix		-1 (Low Range)		-2 (High Range)	
Frequency Set Mode		BCD	BCD+1	BCD	BCD+1
FLJ-ACR1	From	0*	10	0*	100
	To	150	160	1.5k	1.6k
	Resolution	10	10	100	100
FLJ-ACR2	From	0*	100	0*	1k
	To	1.5k	1.6k	15k	16k
	Resolution	100	100	1k	1k

1b. FLJ-ACR1 and ACR2 (Parallel Use) for Greater Frequency Resolution

FLJ-UR Suffix		-1 (Low Range)			-2 (High Range)		
Frequency	-ACR2	BCD	BCD	BCD+1	BCD	BCD	BCD+1
Set Mode	-ACR1	BCD	BCD+1	BCD	BCD	BCD+1	BCD
From		0*	10	100	0*	100	1k
To		1.59k	1.60k	1.69k	15.9k	16.0k	16.9k
Resolution		10	10	10	100	100	100

* Output saturates at 11V dc with zero logic code input (0000); however, digital code corresponds to value of fc directly.

PERFORMANCE

Frequency Set Error ..... ±1% or less

CONTROL CHARACTERISTICS Logic Code ..... BCD 1 digit (1, 2, 4, 8)
Logic and Level ..... 0V: ON
+5V or Open: OFF

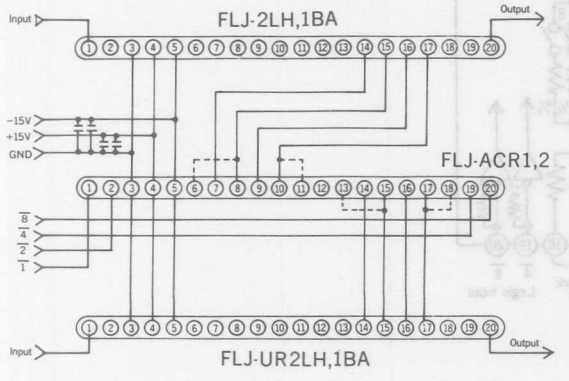
POWER SUPPLIES AND ENVIRONMENT

Power Supply (Operating Range) ..... ±15V (±5V to ±18V)
Current ..... +6.2mA, −1.2mA
Operating Temperature Range ..... 0 to 70°C
Storage Temperature Range ..... −30°C to 80°C
Operating Humidity Range ..... 10% to 95% RH
Storage Temperature Range ..... 10% to 80% RH

TECHNICAL NOTES

1. FLJ-ACR1 and FLJ-ARC2 contain four separate resistor networks which are controlled by common logic inputs. There are two types of FLJ-UR's (resistor tuneable filters) which are to be connected with FLJ-ACR's to build BCD Logic Programmable Filters. One type such as FLJ-UR2LH or FLJ-UR1BA requires two external resistors while all other FLJ-UR's require four external resistors to set a cutoff frequency. Therefore, one FLJ-ACR can control two FLJ-UR2LH's or FLJ-UR1BA's. See Figure 3.
2. BCD + 1 connections are made by connecting pins 6 to 8, 11 to 10, 13 to 15, and 18 to 17 on the units required per Table 1a. or 1b.

TYPICAL CONNECTION (Fig. 3)



ORDERING INFORMATION

MODEL	RESISTANCE
FLJ-ACR1	1.59 MΩ
FLJ-ACR2	159 KΩ

for FLJ-UR Filter Series

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

FLJ-D1, D2, DC
Digital-Programmable Filter

FEATURES

- **Cutoff frequency is set by logic inputs**
- **Lowpass, Highpass and Bandpass output functions are available simultaneously**
- **Gain and Q are set by external components**
- **High accuracy, high stable**

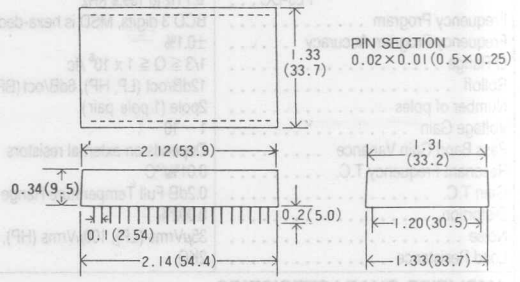
GENERAL DESCRIPTION

FLJ-D1, D2, and DC are digitally programmable filters which can set the cutoff frequency and center frequency with 3 digit BCD inputs.

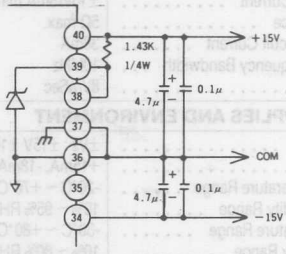
Two-pole lowpass, bandpass, and highpass output functions are available simultaneously from three different outputs and notch function is available by combining these outputs to the uncommitted op amp.

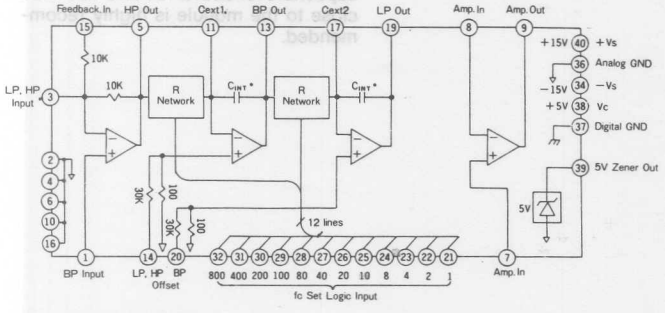
To realize higher order filters, several filters can be cascaded. And to obtain higher performance of higher order filters, both Gain and Q are designed to be set with external components.

MECHANICAL DIMENSIONS
INCHES(mm)



ZENER OUTPUT (Fig. 3)





*C_{INT} FLJ-D1 50,000pF
FLJ-D2 500pF
FLJ-DC None. Need Cext.

PIN CONNECTIONS (Table 1)

FUNCTION	PIN		FUNCTION
INPUT (BP)	1	40	+Vs (+15V)
ANALOG GND	2	39	5V ZENER OUTPUT
INPUT (HP, LP)	3	38	Vc(+5V)
ANALOG GND	4	37	DIGITAL GND
OUTPUT (HP)	5	36	ANALOG GND
ANALOG GND	6	35	NC
AMP. (+) INPUT	7	34	-Vs(-15V)
AMP. (−) INPUT	8	33	NC
AMP. OUTPUT	9	32	LOGIC 800
ANALOG GND	10	31	LOGIC 400
Cext 1.	11	30	LOGIC 200
NC	12	29	LOGIC 100
OUTPUT (BP)	13	28	LOGIC 80
ZERO ADJ. (HP, LP)	14	27	LOGIC 40
NEG. FEEDBACK IN	15	26	LOGIC 20
ANALOG GND	16	25	LOGIC 10
Cext 2.	17	24	LOGIC 8
NC	18	23	LOGIC 4
OUTPUT (LP)	19	22	LOGIC 2
ZERO ADJ. (BP)	20	21	LOGIC 1

DO NOT CONNECT NC PINS TO OTHERS.

SPECIFICATIONS (Table 2)

Typical at 25°C, ±15V and +5V supplies, gain of -1, Q = $\sqrt{2}/2$ unless otherwise specified.

ABSOLUTE RATINGS

Power Supplies ..... ±Vs : ±20V, Vc : +5.5V
Control Logic Input ..... Vc+0.5V
Analog Input ..... ±Vs

FILTER CHARACTERISTICS	
Frequency Program Range : FLJ-D1 ...	1Hz ~ 1.599KHz
FLJ-D2 ...	100Hz ~ 159.9KHz
FLJ-DC ...	0.1 Hz to 159.9 KHz
Frequency Program	BCD 3 digits, MSD is hexa-decimal (0~15)
Frequency Program Accuracy	±0.1%
Q Range	$1/3 \leqq Q \leqq 1 \times 10^6$ /fc
Rolloff	12dB/oct (LP, HP), 6dB/oct (BP)
Number of poles	2pole (1 pole pair)
Voltage Gain	1 ~ 10
Pass Band Gain Variance	Depends on external resistors
Resonant Frequency T.C.	0.01%/°C
Gain T.C.	0.2dB Full Temperature Range
Distortion	0.002%
Noise	35μVrms (LP), 100μVrms (HP), 30μVrms (BP)
Load Resistance	2KΩ
AMPLIFIER CHARACTERISTICS	
Input Voltage Range	±10V min.
Input Impedance	300KΩ
Input Offset Voltage	0.5mV
Input Bias Current	200nA
Input Offset Drift	5μV/°C
Output Voltage/Current	±10V/5mA min.
Output Impedance	5Ω max.
Output Short Circuit Current	38mA
Small Signal Frequency Bandwidth ...	10MHz
Slew Rate	8V/μSec
POWER SUPPLIES AND ENVIRONMENT	
Supply Voltages	±Vs : ±15V ±10%, Vc : +5V ±10%
Supply Current	+15mA, -18mA +2.2mA
Operating Temperature Range	-20°C ~ +70°C
Operating Humidity Range	10% ~ 95% RH
Storage Temperature Range	-30°C ~ +80°C
Storage Humidity Range	10% ~ 80% RH

TECHNICAL NOTES

1. The cutoff frequency of lowpass and highpass, and the center frequency of bandpass filters can be set with three digit BCD, TTL compatible logic inputs. The MSD is hexadecimal. See Table 2.
2. The cutoff frequency is shown as either one equation of the following:

   $fc = \frac{N}{20 \cdot C}$ Hz, C : μF, N : Digital Number

   $fc = \frac{N}{2\pi \cdot C \cdot Rf}$ Hz, C : F, Rf : Ω, N : Digital Number

   C = 50,000pF is contained in FLJ-D1 and C = 500pF is contained in FLJ-D2 respectively, while no capacitor is contained in FLJ-DC.
   The fc's of each model are:

   FLJ-D1 : $fc = N$ or $fc = \frac{N}{2\pi \cdot 5 \times 10^{-8} \cdot Rf}$

   FLJ-D2 : $fc = 100N$ or $fc = \frac{N}{2\pi \cdot 5 \times 10^{-10} \cdot Rf}$

   FLJ-DC : $fc = \frac{N}{20 \cdot C}$ or $fc = \frac{N}{2\pi \cdot Cext \cdot Rf}$

   The value of Rf is 3.183 MΩ.
   The value of Cext is calculated taking these factors into consideration.
3. Each logic input is connected to CMOS4000 series internally. Then each input is pulled down with 100KΩ resistors. The use of 10KΩ pull-up resistors to +5V is recommended when filters are programmed with TTL logic.
4. An independent +5V zener diode is contained in the filter. The output voltage range of this diode is +4.87V ~ +5.12V. The connection shown in Figure 3 is recommended if a filter is driven by ±15V supplies only.
5. Analog GND (Pin36) and logic GND (Pin37) are separated. Connect grounds of ±15V and +5V externally. No return current of the digital power supply should flow through the analog ground.
6. The use of 4.7μF and 0.1μF bypass capacitors for both ±15V and +5V lines close to the module is highly recommended.

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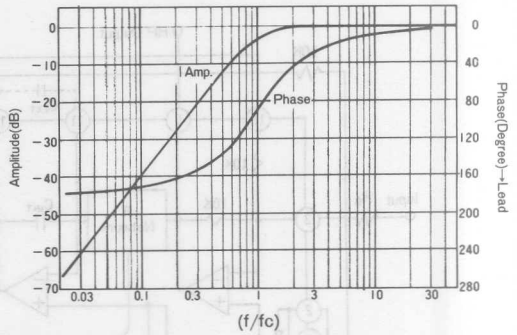
LOGIC INPUT CODING TABLE (Table 2)

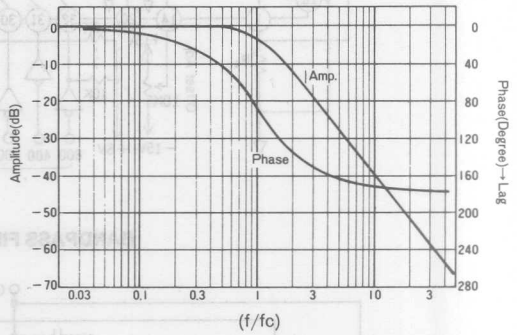
Logic Input *1 (MSD)			(LSD)	Decimal Number	fc (Cutoff Frequency)		
					FLJ-D1	FLJ-D2	FLJ-DC*2
0 0 0 0	0 0 0 0	0 0 0 1		1	1Hz	100Hz	0.1Hz
0 0 0 0	0 0 0 0	0 0 1 0		2	2	200	0.2
0 0 0 0	0 0 0 0	0 1 0 0		4	4	400	0.4
0 0 0 0	0 0 0 0	1 0 0 0		8	8	800	0.8
0 0 0 0	0 0 0 1	0 0 0 0		10	10	1KHz	1
0 0 0 0	0 0 1 0	0 0 0 0		20	20	2	2
0 0 0 0	0 1 0 0	0 0 0 0		40	40	4	4
0 0 0 0	1 0 0 0	0 0 0 0		80	80	8	8
0 0 0 1	0 0 0 0	0 0 0 0		100	100	10	10
0 0 1 0	0 0 0 0	0 0 0 0		200	200	20	20
0 1 0 0	0 0 0 0	0 0 0 0		400	400	40	40
1 0 0 0	0 0 0 0	0 0 0 0		800	800	80	80
1 0 0 1	0 0 0 0	0 0 0 0		900	900	90	90
1 0 1 0	0 0 0 0	0 0 0 0		1000	1000	100	100
1 1 0 0	0 0 0 0	0 0 0 0		1200	1200	120	120
1 1 1 0	0 0 0 0	0 0 0 0		1400	1400	140	140
1 1 1 1	0 0 0 0	0 0 0 0		1500	1500	150	150
1 1 1 1	1 0 0 1	1 0 0 1		1599	1599Hz	159.9KHz	159.9Hz

Note: *1. Logic 1 = +5V
Logic 0 = GND or OPEN
*2. FLJ-DC needs external capacitors.
These values are ones when two 0.5μF are used as external capacitors.

BUTTERWORTH HIGHPASS (Fig. 4)



BUTTERWORTH LOWPASS (Fig. 5)



GAIN AND Q

The gain and Q of these filters are set with the following equations.

1. Lowpass and highpass filters

Gain: $G = \frac{-1}{Rg} \times 10^4$ (Rg : Ω)

Q: $Q = \frac{Rg \cdot (Rq + 10^4)}{Rq \cdot (2Rg + 10^4)}$

Rg = 10KΩ when G = -1. Then, $Rq = \frac{10^4}{3Q-1}$

Then, the following values are obtained:

	Q	Rq
Butterworth	0.70711	8.918KΩ
Bessel	0.57735	13.66KΩ

See Figures 4 and 5 for "Amplitude/Phase vs. Frequency" characteristics, and Figure 7 for typical connections.

2. Bandpass filter

Gain: $G = \frac{-1}{Rg} \times 10^4$ (Rg : Ω)

Q: $Q = \frac{1 + (1/Rg + 1/Rq) \cdot 10^4}{2}$

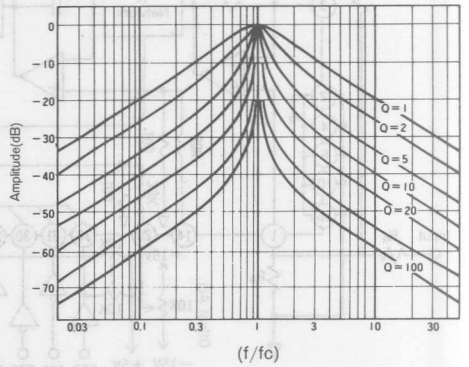
Rg = 10KΩ when G = -1. Then, $Rq = \frac{10^4}{2(Q-1)}$

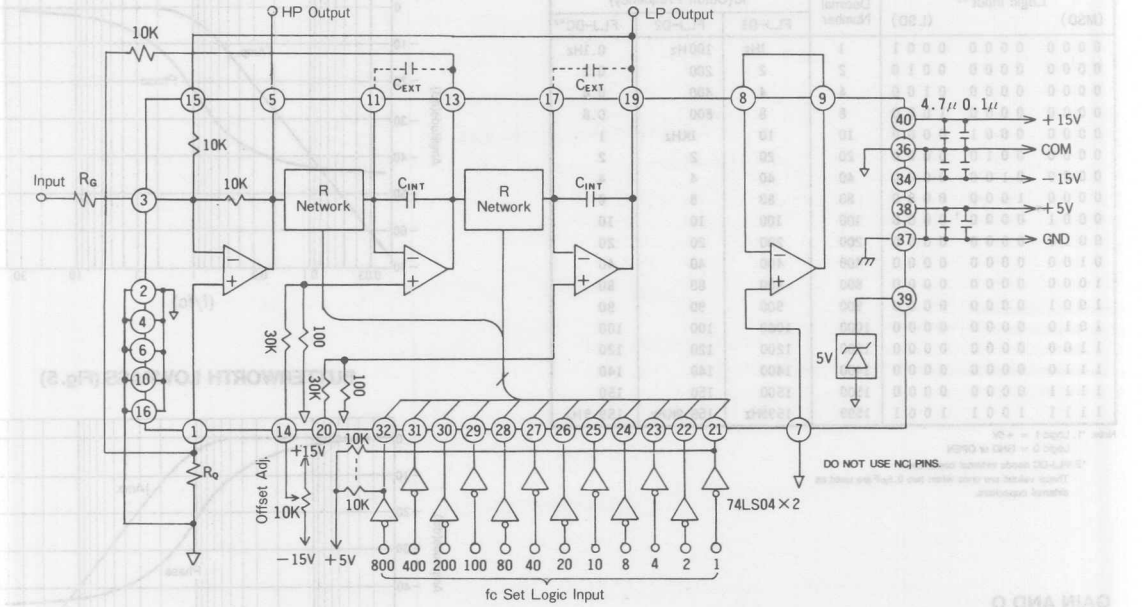
Then, the following values are obtained:

Q	Rq
2	5.00KΩ
5	1.25KΩ
10	556Ω

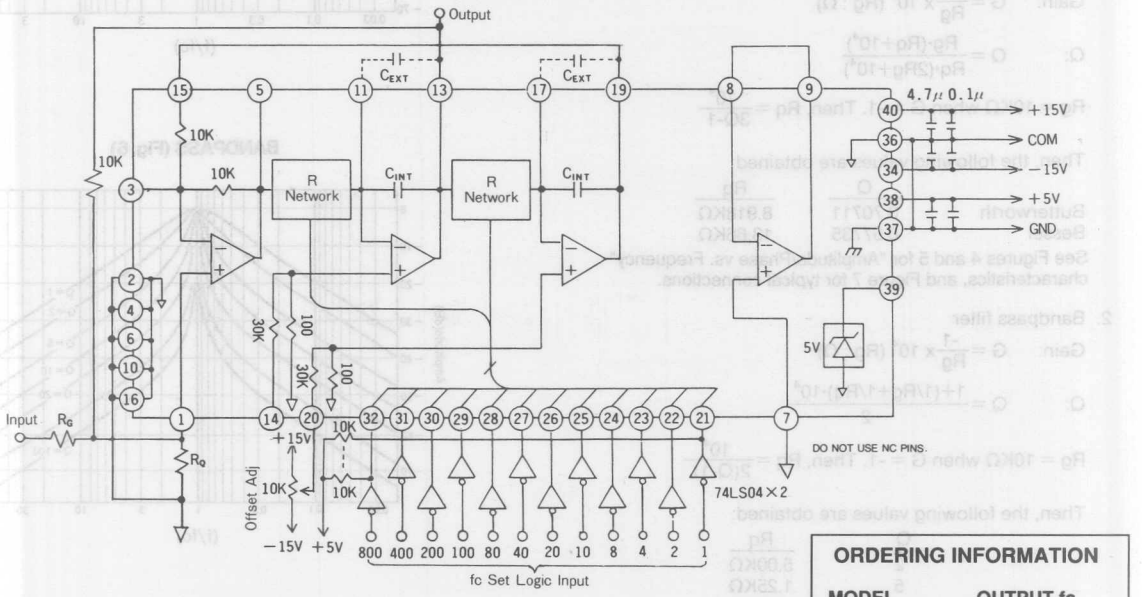
See Figure 6 for amplitude vs. frequency characteristics and Figure 8 for typical connections.

BANDPASS (Fig. 6)





BANDPASS FILTER CONNECTIONS (Fig.8)



ORDERING INFORMATION

MODEL	OUTPUT fc
FLJ-D1	1 Hz to 1.599 KHz
FLJ-D2	100 Hz to 159.9 KHz
FLJ-DC	0.1 Hz to 159.9 KHz

FLJ-D5, D6
Digital-Programmable, High-Order Lowpass Filter

FEATURES

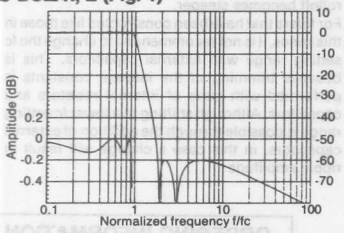
- **60dB, 80dB/octave rolloff low-pass filter**
- **Cutoff frequency programmed by logic at 8 points**
- **Compact, lightweight, hybrid IC construction**

GENERAL DESCRIPTION

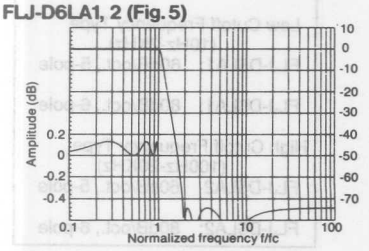
FLJ-D5, and D6 series are lowpass filters that, although compact, have higher order and high attenuation performance. They are Chebyshev type filters. The FLJ-D5LA is a 5-pole filter which has a rolloff of 60 dB/oct and the FLJ-D6LA is a 6-pole filter with a rolloff of 80 dB/oct. The cutoff frequency is programmed with 3-bit, TTL-compatible digital logic and the settings can be changed to 8 different levels. Cut-off frequency range of the lower range type (which has suffix 1) is 10Hz-2kHz, and the higher range type (with suffix 2) is 100Hz-20KHz.

Ripple within the pass band is minimal at 0.13dBp-p and the distortion rate is held extremely low at 0.05%. These filters are optimal as anti-aliasing filters in A/D conversion circuits of data acquisition systems.

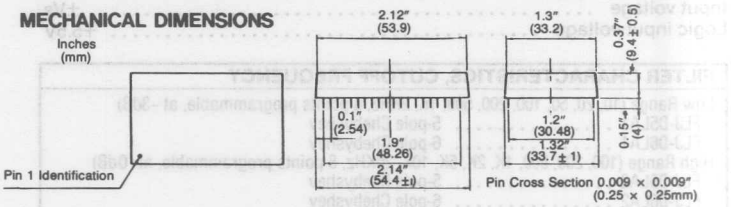
FLJ-D5LA1, 2 (Fig. 4)

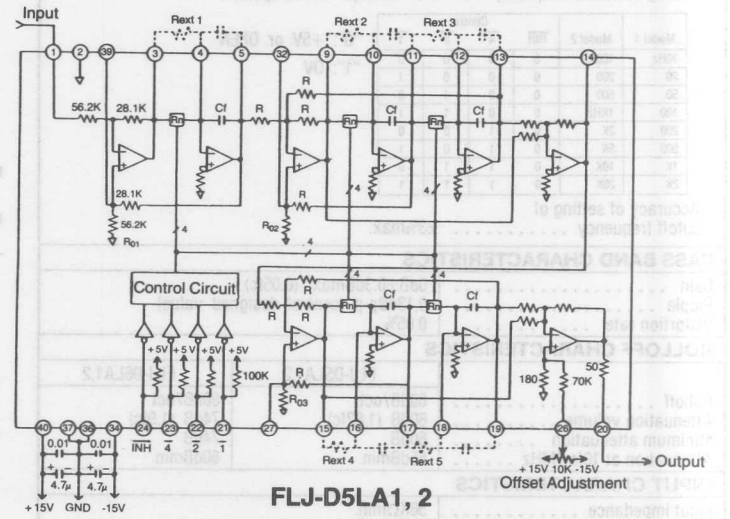


FLJ-D6LA1, 2 (Fig. 5)



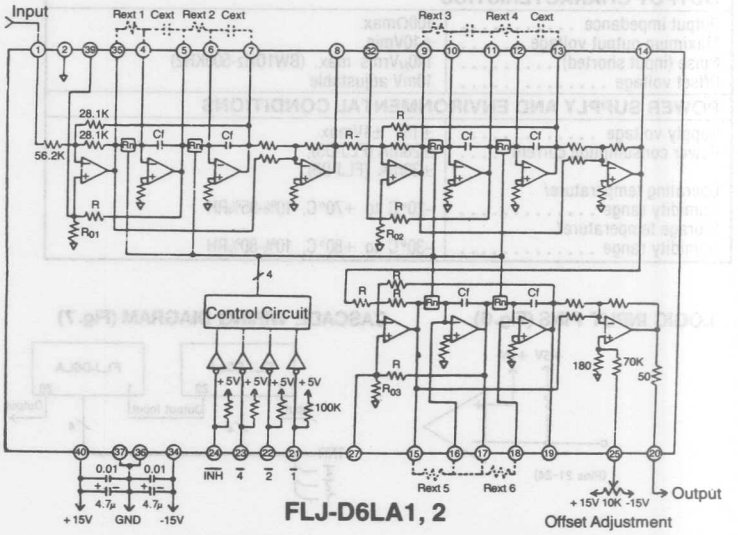
MECHANICAL DIMENSIONS





FLJ-D5LA1, 2

Cf in the diagram is 10000pF for the Suffix 1 model and 1000pF for the Suffix 2 model.



FLJ-D6LA1, 2

Cf in the diagram is 10000pF for.the Suffix 1 model and 1000pF for the Suffix 2 model.

SPECIFICATIONS (Table 1)

Typical at 25° C and ±15V supply voltage unless otherwise specified.

ABSOLUTE RATINGS

Supply voltage (±Vs) ..... ±16V
Input voltage ..... ±Vs
Logic input voltage ..... +5.5V

FILTER CHARACTERISTICS, CUTOFF FREQUENCY

Low Range (10, 20, 50, 100, 200, 500, 1K, 2KHz, 8 points programmable, at -3dB)
FLJ-D5LA1 ..... 5-pole Chebyshev
FLJ-D6LA1 ..... 6-pole Chebyshev
High Range (100, 200, 500, 1K, 2K, 5K, 10K, 20KHz, 8 points programmable, at 0dB)
FLJ-D5LA2 ..... 5-pole Chebyshev
FLJ-D6LA2 ..... 6-pole Chebyshev
Setting of Cutoff Frequency ... 3-bit binary, TTL-compatible

Model 1	Model 2	Control $\overline{INH}$	4	2	1
10Hz	100Hz	0	0	0	0
20	200	0	0	0	1
50	500	0	0	1	0
100	1KHz	0	0	1	1
200	2K	0	1	0	0
500	5K	0	1	0	1
1K	10K	0	1	1	0
2K	20K	0	1	1	1

"0": +5V or OPEN
"1": 0V

Accuracy of setting of cutoff frequency ..... ±3%max.

PASS BAND CHARACTERISTICS

Gain	0dB±0.3dBmax. (0.05fc)
Ripple	0.13dBp-p (central designed value)
Distortion rate	0.05%

ROLLOFF CHARACTERISTICS

	FLJ-D5LA1,2	FLJ-D6LA1,2
Rolloff	60dB/oct	80dB/oct
Attenuation volume	60dB (1.82fc)	74dB (1.9fc)
Minimum attenuation	60dB	74dB
Attenuation at 10fc-1MHz	55dBmin.	60dBmin.

INPUT CHARACTERISTICS

Input impedance	50KΩmin.
Maximum input voltage	±10Vmin.

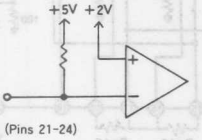
OUTPUT CHARACTERISTICS

Output impedance	100Ωmax.
Maximum output voltage	±10Vmin.
Noise (input shorted)	140μVrms max. (BW10Hz-500KHz)
Offset voltage	10mV adjustable

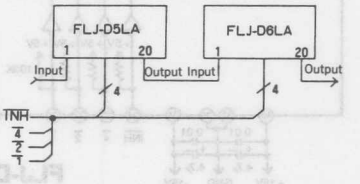
POWER SUPPLY AND ENVIRONMENTAL CONDITIONS

Supply voltage	±15V ±1Vmax.
Power consumption current	±28mA (FLJ-D5), ±33mA (FLJ-D6)
Operating temperature/ Humidity range	-20°C to +70°C, 10%-95%RH
Storage temperature/ Humidity range	-30°C to +80°C, 10%-80%RH

LOGIC INPUT PINS (Fig. 6)



CASCADE WIRING DIAGRAM (Fig. 7)



TECHNICAL NOTES

1. A switching-type power supply is not recommended. Install 0.01 μF multilayer ceramic and 4.7 μF tantalum bypass capacitors in parallel as close to the filter as possible.
2. Each logic input (Pins 21-24) which programs the cutoff frequency has an internal analog comparator as shown in Fig. 6. External logic signals are TTL-compatible.
3. The fc setting input logic is negative true. Terminal open or +5V represents logic "0", while GND level is logic "1". The $\overline{INH}$ terminal is used normally open. Once $\overline{INH}$ is given logic "1", all 4, 2 and $\overline{1}$ logic inputs are inhibited and all internal resistor network switches are opened. The fc setting with external resistors becomes available with logic "1" at this $\overline{INH}$ terminal. The relationship between fc and the external resistors in this case is as follows:

FLJ-D5LA1 (Low Range Type)

$$Rext1 = \frac{31.423 \times 10^3}{fc\ (Hz)}\ (K\Omega)$$

$$Rext2 = Rext3 = \frac{21.399 \times 10^3}{fc\ (Hz)}\ (K\Omega)$$

$$Rext4 = Rext5 = \frac{16.358 \times 10^3}{fc\ (Hz)}\ (K\Omega)$$

FLJ-D6LA1 (Low Range Type)

$$Rext1 = Rext2 = \frac{29.622 \times 10^3}{fc\ (Hz)}\ (K\Omega)$$

$$Rext3 = Rext4 = \frac{18.633 \times 10^3}{fc\ (Hz)}\ (K\Omega)$$

$$Rext5 = Rext6 = \frac{15.215 \times 10^3}{fc\ (Hz)}\ (K\Omega)$$

FLJ-D5LA2 (High Range Type)

$$Rext1 = \frac{314.23 \times 10^3}{fc\ (Hz)}\ (K\Omega)$$

$$Rext2 = Rext3 = \frac{213.99 \times 10^3}{fc\ (Hz)}\ (K\Omega)$$

$$Rext4 = Rext5 = \frac{163.58 \times 10^3}{fc\ (Hz)}\ (K\Omega)$$

FLJ-D6LA2 (High Range Type)

$$Rext1 = Rext2 = \frac{296.22 \times 10^3}{fc\ (Hz)}\ (K\Omega)$$

$$Rext3 = Rext4 = \frac{186.33 \times 10^3}{fc\ (Hz)}\ (K\Omega)$$

$$Rext5 = Rext6 = \frac{152.15 \times 10^3}{fc\ (Hz)}\ (K\Omega)$$

4. An 11-pole ultra-high attenuation filter is available once cascaded as shown in Fig. 7. As can be seen from the curves (Figs. 4,5), the amplitude of the ripple in the pass band is reversed between FLJ-D5LA and FLJ-D6LA. As a result, when connected in a cascade, the pass band ripple amplitude is greatly reduced, and moreover, the rolloff becomes steeper.
5. For filters that have been constructed like those in this series, it is not recommended to change the fc setting range with external capacitors. This is because trimming of the internal constants is performed with pairs of internal resistors and capacitors. Although shifting to a lower fc setting range is possible through the addition of external capacitors, in this case a change will result in ripple amplitude.

ORDERING INFORMATION

Low Cutoff Frequency Type (10Hz-2KHz)
FLJ-D5LA1: 60dB/oct., 5-pole
FLJ-D6LA1: 80dB/oct., 6-pole

High Cutoff Frequency Type (100Hz-20KHz)
FLJ-D5LA2 60dB/oct., 5-pole
FLJ-D6LA2: 80dB/oct., 6-pole

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FLJ-R Series
Higher Order, Resistor-Tuneable Filter

FEATURES

- **135dB, 100dB/octave high order, lowpass filter**
- **1/3 octave bandwidth (Q=4.32) bandpass filter**
- **Can set cutoff (fc) frequency with 6 or 8 external resistors**
- **Ultra-compact size, high-function hybrid construction**

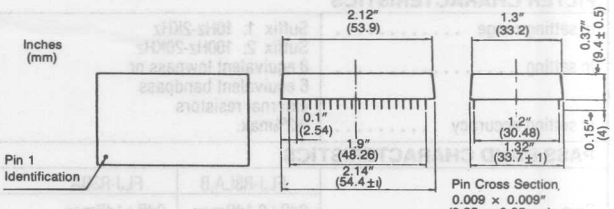
GENERAL DESCRIPTION

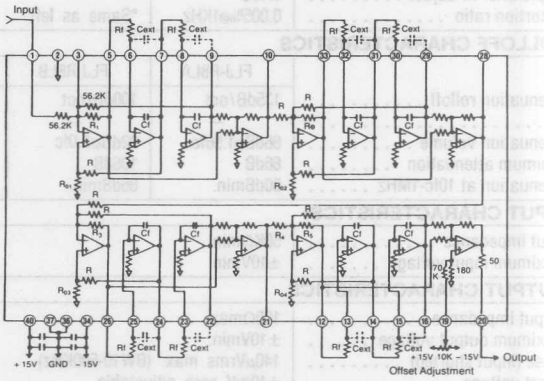
The FLJ-R series filters are of the highest order and have the highest attenuation characteristics among the entire group of DATEL filter products. Through the use of hybrid techniques, even though compact in size, the FLJ-R series filters have complete 8-pole lowpass and 3-pole pair bandpass filter functions. The cutoff (central) frequency can be set with only 6 or 8 external resistors.

Bandpass ripple in the lowpass filter is 0.1dB and boasts outstanding performance with the distortion ratios for all models being a mere 0.005%. Each model is composed of the Suffix 1 and Suffix 2 types and varies according to cutoff frequency setting range. The Suffix 1 model has a range from 10Hz-2KHz and the Suffix 2 model has a range from 100Hz-20KHz. The FLJ-R series filters are optimum as anti-aliasing filters in A/D conversion circuits of data acquisition systems.

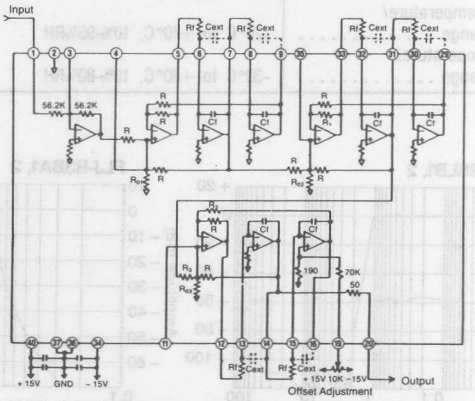
The FLJ-R3BA1, 2 are 1/3 octave, bandpass filters that meet IEC-225 Standard requirements.

MECHANICAL DIMENSIONS



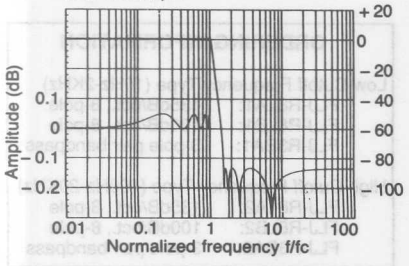


FLJ-R8LA, B Block Diagram with External Connections (Fig. 1)



FLJ-R3BA Block Diagram with External Connections (Fig. 2)

FLJ-R8LA1, 2



SPECIFICATIONS

Typical at 25°C and ±15V supply voltage unless otherwise specified.

ABSOLUTE RATINGS

Supply voltage (±Vs) ..... ±18V
Input voltage ..... ±Vs

FILTER CHARACTERISTICS	
fc setting range	Suffix 1: 10Hz-2KHz Suffix 2: 100Hz-20KHz
fc setting	8 equivalent lowpass or 6 equivalent bandpass external resistors
fc setting accuracy	±2%max.

PASS BAND CHARACTERISTICS	FLJ-R8LA,B	FLJ-R3BA
Gain	0dB±0.1dBmax.	0dB±1dBmax.
Gain after Rf adjustment	—	0dB±
Ripple p-p	0.15dB	—
Ripple ≦0.9fc	0.3dBmax.	—
Ripple after Rf adjust	0.1dB	—
Distortion ratio	0.005%@1KHz	*Same as left

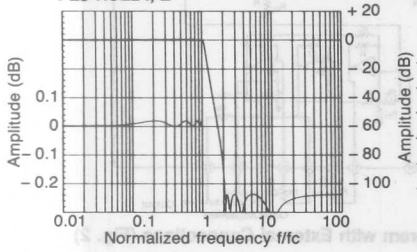
ROLLOFF CHARACTERISTICS	FLJ-R8LA	FLJ-R8LB	FLJ-R3BA
Attenuation rolloff	135dB/oct	100dB/oct	—
Q	—	—	4.32(BW1/3oct)
Attenuation volume	86dB@1.56fc	92dB@2.0fc	18dB/octBW
Minimum attenuation	86dB	106dB	—
Attenuation at 10fc-1MHz	80dBmin.	86dBmin.	80dBmin.

INPUT CHARACTERISTICS	
Input impedance	50KΩmin.
Maximum input voltage	±10Vmin.

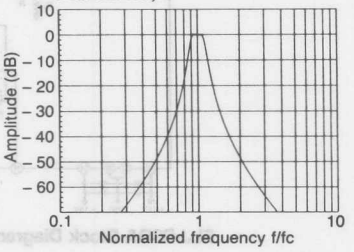
OUTPUT CHARACTERISTICS	
Output impedance	100Ωmax.
Maximum output voltage	±10Vmin.
Noise (input shorted)	140μVrms max. (BW10-500KHz)
Offset voltage	±10mV zero adjustable

POWER SUPPLY AND ENVIRONMENTAL CONDITIONS	
Supply voltage (operating range)	±15V (±5V-±18V)
Power consumption current	40mA (FLJ-R8), 25mA (FLJ-R3)
Operating temperature/ Humidity range	-20°C to +70°C, 10%-95%RH
Storage temperature/ Humidity range	-30°C to +80°C, 10%-80%RH

FLJ-R8LB1, 2



FLJ-R3BA1, 2



TECHNICAL NOTES

1. Setting the cutoff (central) frequency is accomplished with 8 external resistors which are equal in value for lowpass filters and 6 external resistors which are equal in value for bandpass filters. The relationship between the resistance Rf of the external resistors and the cutoff frequency fc is as follows:

Suffix 1 model (10Hz-2KHz) $Rf = \frac{15.9 \times 10^3}{fc} (K\Omega)$ *Suffix 2 model (100Hz-20KHz)* $Rf = \frac{159 \times 10^3}{fc} (K\Omega)$

where fc is measured in Hz.

The FC setting range can be shifted to a lower band by adding external capacitors Cext. The equation shown below should be used for reference.

Suffix 1 model $Cext = \frac{159}{(Cext + 0.01) \times fc} (K\Omega)$ *Suffix 2 model* $Cext = \frac{159}{(Cext + 0.001) \times fc} (K\Omega)$

where Cext is measured in μF and fc in Hz.

In this case, the external capacitors should have high dielectric characteristics. It is recommended to use multilayer ceramic capacitors. Further, tolerance of these capacitors should be within ±0.25%. For filters such as these of higher order and with high attenuation characteristics, the uniformity of the tolerance of external resistors and capacitors has an effect not only on the accuracy of the setting range, but also on the size of pass band ripple.

2. Use series type power supplies for the ±15V power supplies because switching-type power supplies are not recommended. Install 4.7μF tantalum and 0.01μF multilayer ceramic bypass capacitors. It is recommended that these be installed in parallel, and as close to the filter as possible, between the ±15V power supplies and ground.
3. Use metal film resistors with a tolerance better than 1% for the 6 or 8 fc setting resistors.

ORDERING INFORMATION

Low Cutoff Frequency Type (10Hz-2KHz)
- FLJ-R8LA1: 135dB/oct., 8-pole
- FLJ-R8LB1: 100dB/oct., 8-pole
- FLJ-R3BA1: 3-pole pair bandpass

High Cutoff Frequency Type (100Hz-20KHz)
- FLJ-R8LA2: 135dB/oct., 8-pole
- FLJ-R8LB2: 100dB/oct., 8-pole
- FLJ-R3BA2: 3-pole pair bandpass

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FLJ-UR Series
Single In-line Hybrid Resistor Tuneable Filter

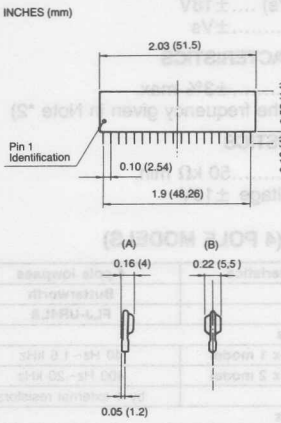
FEATURES

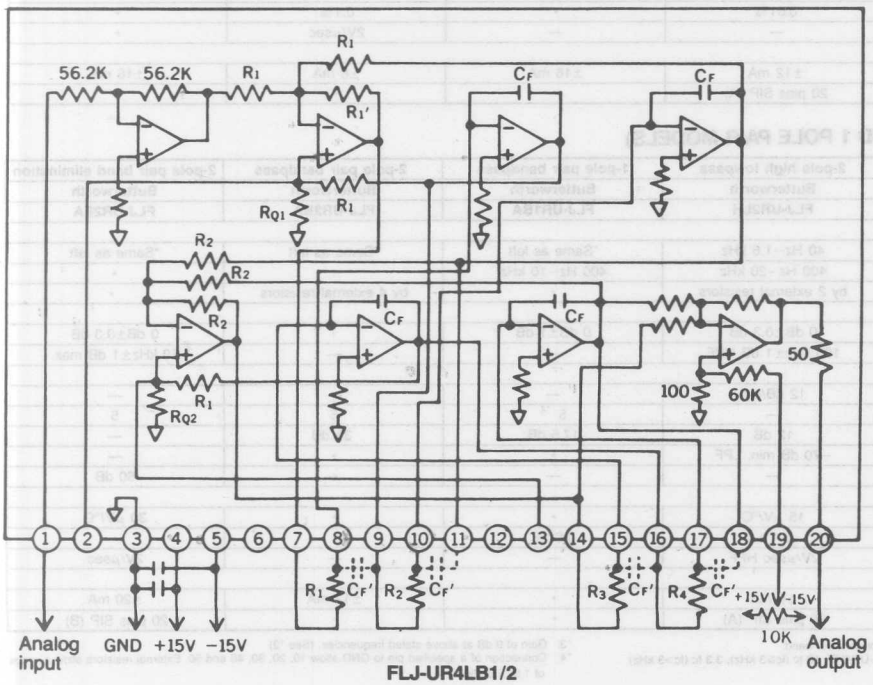
- **Small and thin size**
- **A variety of families**
- **Cutoff frequency fc is set by only two or four resistors**
- **Light weight, low cost**

GENERAL DESCRIPTION

The FLJ-UR series filters are single in-line package resistor tuneable filters. They are small in size and can reduce installation space on the printed circuit board. The cutoff frequency can be easily set by only two or four external resistors. The series has a variety of products, allowing system designers flexibility in selecting filters to suit their application.

MECHANICAL DIMENSIONS (Fig. 2)





FLJ-UR4LB1/2

SPECIFICATIONS

Typical at R=31.8 kΩ, 25°C and ±15V supply voltage unless otherwise specified.

COMMON SPECIFICATIONS TO ALL MODELS

ABSOLUTE RATINGS

Supply voltage (±Vs) ....±18V
Input voltage.....±Vs

FREQUENCY CHARACTERISTICS

fc accuracy.....±3% max.
(with 0 dB gain at the frequency given in Note *2)

INPUT CHARACTERISTICS

Input Impedance.....50 kΩ min.
Maximum Input Voltage ±10V

OUTPUT CHARACTERISTICS

Output Impedance .....100Ω max.
Maximum Output Voltage ...±10V min.
Load Resistance.....10 kΩ min.
Noise (10~500 kHz).....140 μV max.
Offset Voltage .....±30 mV max. zero adjustable

POWER SUPPLY AND ENVIRONMENTS

Supply Voltage.....±15V
Supply Voltage,
Operating Range.....±5V~±18V
Operating Temerature/
Humidity Range .....−20°C~70°C, 10~95%RH
Storage Temperature/
Humidity Range .....−30°C~80°C, 10~80%RH

SPECIFICATIONS 1 (4 POLE MODELS)

No. of poles/characteristics		4-pole lowpass	4-pole lowpass	4-pole highpass	4-pole highpass
Type		Butterworth	Chebyshev	Butterworth	Chebyshev
Model		FLJ-UR4LA	FLJ-UR4LB	FLJ-UR4HA	FLJ-UR4HB
fc (−3 dB) characteristics					
Range*1	Suffix 1 model	40 Hz~1.6 kHz	*Same as left	*Same as left	*Same as left
	Suffix 2 model	400 Hz~20 kHz	•	400 Hz~5 kHz	•
Setting		by 4 external resistors	•	•	•
Pass band characteristics					
Gain*2		0 dB±0.3 dB	•	0 dB±1 dB	•
Ripple		—	0.28 dBp-p	—	0.28 dBp-p
Upper-limit frequency (small signal)		—	—	50 kHz±1 dB max.*3	•
Rolloff characteristics					
Rolloff		24 dB/oct	42 dB/oct or equivalent	24 dB/oct	42 dB/oct or equivalent
Attenuation volume (1/2 fc or 2 fc)		24 dB	55 dB	24 dB	55 dB
Minimum attenuation		—	46 dB	—	46 dB
Attenuation at 1 MHz		70 dB min.	•	—	—
Output characteristics					
Offset drift		30 μV/°C	•	15 μV/°C	•
Distortion rate*2		0.01%	•	0.1%	•
Slew rate		—	—	2V/μsec	•
Quiescent current/package					
Quiescent current (@±15V)		±12 mA	±16 mA	±8 mA	±16 mA
Package		20 pins SIP (A)	•	•	•

SPECIFICATIONS 2 (2 POLE AND 1 POLE PAIR MODELS)

No. of poles/characteristics		2-pole high lowpass	1-pole pair bandpass	2-pole pair bandpass	2-pole pair band elimination
Type		Butterworth	Butterworth	Butterworth	Butterworth
Model		FLJ-UR2LH	FLJ-UR1BA	FLJ-UR2BA	FLJ-UR2EA
fc (−3 dB) characteristics					
Range*1	Suffix 1 model	40 Hz~1.6 kHz	*Same as left	*Same as left	*Same as left
	Suffix 2 model	400 Hz~20 kHz	400 Hz~10 kHz	•	•
Setting		by 2 external resistors	•	by 4 external resistors	•
Pass band characteristics					
Gain*2		0 dB±0.3 dB	0 dB±1 dB	•	0 dB±0.3 dB
Upper-limit frequency (small signal)*3		100 kHz±1 dB HPF	—	—	50 kHz±1 dB max.
Rolloff characteristics					
Rolloff		12 dB/oct	—	—	—
Q		—	5 *4	5	5
Attenuation volume (1/2 fc or 2 fc)		12 dB	17.5 dB	35 dB	—
Attenuation at 1 MHz		−70 dB min. LPF	•	•	—
Maximum attenuation (f_0)		—	—	—	60 dB
Output characteristics					
Offset drift		15 μV/°C	•	•	30 μV/°C
Distortion rate*2		0.1%	0.01%	•	•
Slew rate		2V/μsec HPF	—	—	2V/μsec
Quiescent current/package					
Quiescent current (@±15V)		±8 mA	•	±12 mA	±20 mA
Package		20 pins SIP (A)	•	•	20 pins SIP (B)

*1: Addition of 2 or 4 external capacitors allow extension to lower band.
*2: FLJ-UR4LA, 4LB; fc/10, FLJ-UR4HA; 3.3 fc, FLJ-UR4HB; 10 fc (fc≦3 kHz), 3.3 fc (fc>3 kHz)
FLJ-UR2LH; fc/10 (LPF), 10 fc (HPF)
*3: Gain of 0 dB at above stated frequencies. (See *2)
*4: Connection of a specified pin to GND allow 10, 20, 30, 40 and 50. External resistors allow a range of 1.81≦Q≦50.

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TECHNICAL NOTES

1. Do not use a switching regulator. Use a well regulated ±15V power supply. Install 0.01 μF bypass capacitors as close to the filter as possible.

2. Use metal film resistors of 1% tolerance for fc setting. When making a higher-order filter, use more accurate resistors.

3. Connect external resistors with short leads as close to the filter as possible.

4. Use external capacitors with good stability and high dielectric resistance. It is recommended to use multilayer ceramic capacitors or plastic film capacitors.

5. Regulate output offset voltage by using an external trimmer (10 KΩ to 50 KΩ).

6. The FLJ-UR series filters are packaged single inline and are compact in size. Installation at high-density may cause temperature rises between elements. Installation with 0.8" or more of space between filters can eliminate the problem.

7. Relation between fc and external resistor/capacitor:
With the FLJ-UR series, a cutoff or center frequency can be set by 2 or 4 external resistors. The values of R of 2 or 4 external resistors for normal use can be calculated as;

$$R = \frac{15.9\times10^6}{fc\ (Hz)}\ (\Omega) \quad \text{Suffix 1 model}$$

$$R = \frac{159\times10^6}{fc\ (Hz)}\ (\Omega) \quad \text{Suffix 2 model}$$

Note: $R_1 = R_2 = R_3 = R_4$

In certain applications the resistance of each of 2 or 4 resistors may be changed. R_1 to R_4 shown in the block diagrams are the external resistors explained here. In standard use, the fc can be set to a minimum of 40 Hz. This is because the values of R have to be increased to about 400K according to the relation between R and fc. The fc setting range can be expanded to lower band by adding 2 or 4 external capacitors.

$$R = \frac{159\times10^3}{(Cext+0.01)\ fc}\ (\Omega) \quad \text{Suffix 1 model}$$

$$R = \frac{159\times10^3}{(Cext+0.001)\ fc}\ (\Omega) \quad \text{Suffix 2 model}$$

where Cext is measured in μF and Fc in Hz.

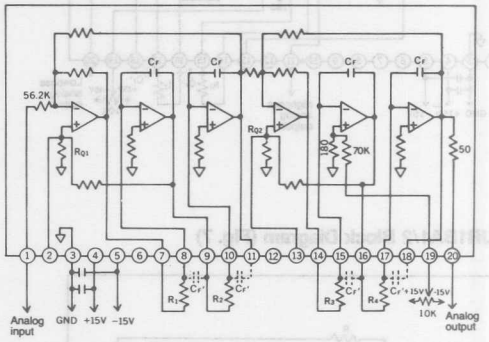
In the applications in which the output offset, time drift, or output noise must be minimal, use the above external capacitors if the values of external resistors exceed 100 kΩ each.

8. How to tune fc
As shown in the specifications, the fc setting accuracy is 3% depending on the accuracy of elements used. There is no practical problem in tuning when they are used as low-pass or highpass filters. However, bandpass filters and band elimination filters may require sharp tuning. Such filters can be tuned with external trimmers as shown in Fig. 10. R_1, R_2 and VR_1 are not used with the FLJ-UR1BA1/2.

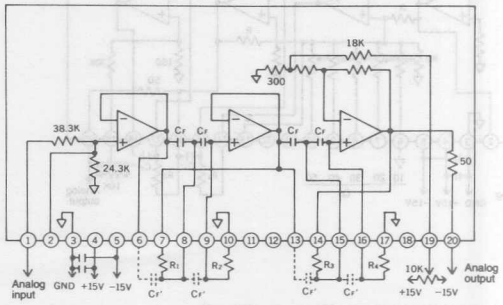
   a. FLJ-UR1BA1/2
   - An input signal of oscillating frequency fc is given.
   - I/O signals are monitored with a phase measuring instrument such as an oscilloscope.
   - Tune VR_2 until the phase difference between I/O signals can be reduced to 0°.

   b. FLJ-UR2BA1/2
   - An input frequency of 1.0734×fc is provided.
   - Tune VR_1 until the phase difference between the input signal and the output signal at pin 9 reaches at 180° looking at a phase measuring instrument such as an oscilloscope.
   - An input signal of frequency fc is given.
   - Tune VR2 until the phase difference between the input signal and the output signal at pin 20 is set at 0°.

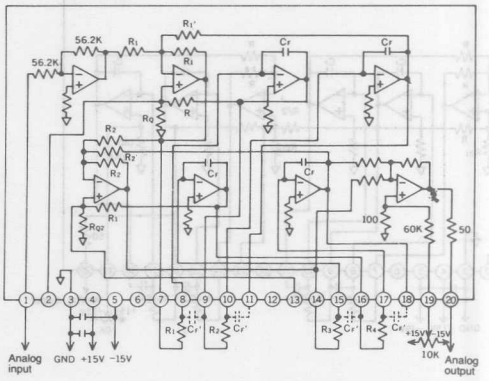
FLJ-UR4LA1/2 Block Diagram (Fig. 3)



FLJ-UR4HA1/2 Block Diagram (Fig. 4)

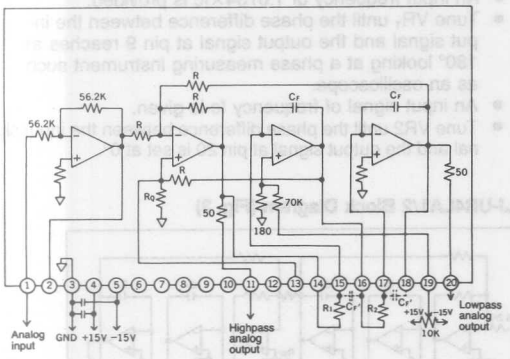


FLJ-UR4HB1/2 Block Diagram (Fig. 5)

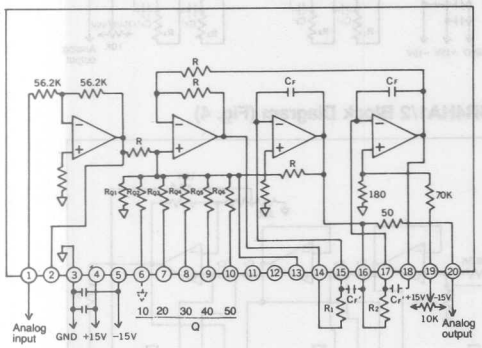


Cf in each figure is 10000 pF for suffix 1 model and 1000 pF for suffix 2 model.

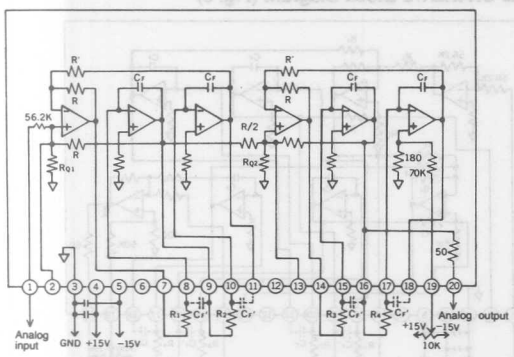
FLJ-UR2LH1/2 Block Diagram (Fig. 6)



FLJ-UR1BA1/2 Block Diagram (Fig. 7)

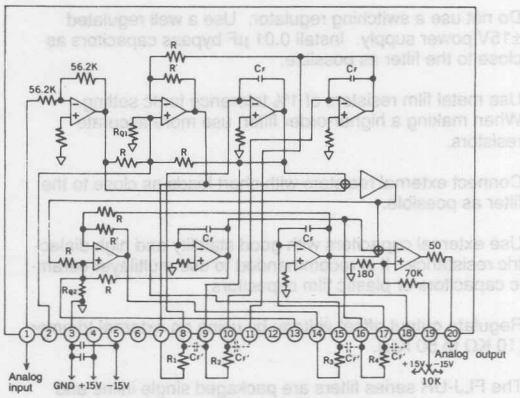


FLJ-UR2BA1/2 Block Diagram (Fig. 8)

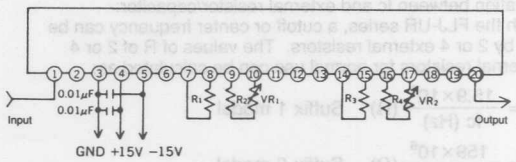


Cf in each figure is 10000 pF for suffix 1 model and 1000 pF for suffix 2 model.

FLJ-UR2EA1/2 Block Diagram (Fig. 9)



fc tuning method (Fig. 10)



ORDERING INFORMATION

LOW CUTOFF FREQUENCY TYPE (40 Hz~1.6 kHz)

FLJ-UR4LA1: 4-pole lowpass, Butterworth
FLJ-UR4LB1: 4-pole lowpass, Chebyshev
FLJ-UR4HA1: 4-pole highpass, Butterworth
FLJ-UR4HB1: 4-pole highpass, Chebyshev
FLJ-UR2LH1: 2-pole lowpass/highpass, Butterworth
FLJ-UR1BA1: 1-pole pair bandpass, Butterworth
FLJ-UR2BA1: 2-pole pair bandpass, Butterworth
FLJ-UR2EA1: 2-pole pair band elimination, Butterworth

HIGH CUTOFF FREQUENCY TYPE (400 Hz~5 k/10 k/20 kHz)

FLJ-UR4LA2: 4-pole lowpass, Butterworth
FLJ-UR4LB2: 4-pole lowpass, Chebyshev
FLJ-UR4HA2: 4-pole highpass, Butterworth
FLJ-UR4HB2: 4-pole highpass, Chebyshev
FLJ-UR2LH2: 2-pole highpass/lowpass, Butterworth
FLJ-UR1BA2: 1-pole pair bandpass, Butterworth
FLJ-UR2BA2: 2-pole pair bandpass, Butterworth
FLJ-UR2EA2: 2-pole pair band elimination, Butterworth

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FLJ-VL, VH, VB
Voltage Tuneable Filter

FEATURES

- **Cutoff frequency is tuned by external voltage**
- **Wide range of control frequency**
- **Small in hybrid**

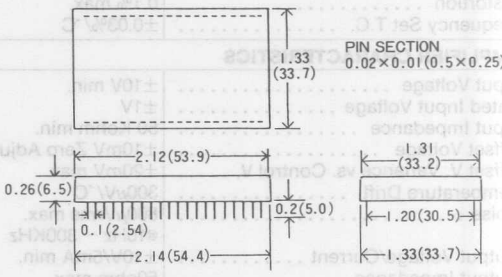
GENERAL DESCRIPTION

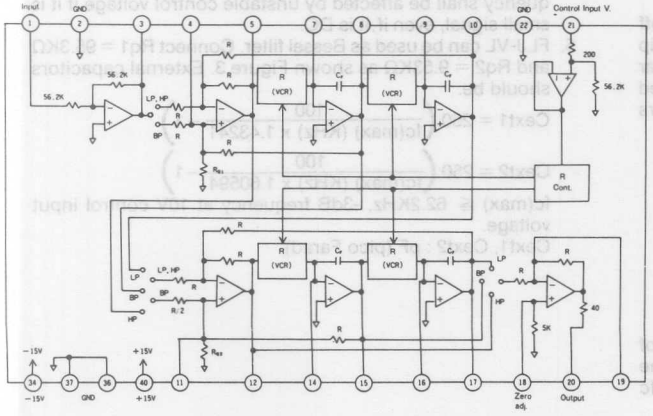
FLJ-V Series filters cutoff frequency or center frequency can be set with an external control voltage.

Hybrid construction has made it possible to build highly reliable, high performance filters in small size at low cost.

FLJ-VL is a lowpass filter and FLJ-VH is a highpass filter. Both filters have 24dB/oct of rolloff characteristics. FLJ-VB is a bandpass filter which has 12dB/octBW at Q=5.

MECHANICAL DIMENSIONS
INCHES (mm)





PIN CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	INPUT	21	CONTROL V. INPUT
2	GND	22	GND
4	Rq1	34	-Vcc (-15V)
7	Cext1-1	36	GND
8	Rq1, Cext1-1	37	GND
9	Cext1-2	40	+Vcc (+15V)
10	Cext1-2		
11	Rq2		
14	Cext2-1		
15	Rq2, Cext2-1		
16	Cext 2-2		
17	Cext2-2		
18	ZERO ADJ.		
20	OUTPUT		

DO NOT CONNECT UNUSED PINS TO OTHERS.

SPECIFICATIONS

Typical values at 25°C with ±15V supply, 10V control voltage, ±1V rated input unless otherwise specified.

	FLJ-VL (Lowpass Filter)	FLJ-VB (Bandpass Filter)	FLJ-VH (Highpass Filter)
ABSOLUTE MAXIMUM			
Power Supply Voltage	±18V	* "Same as FLJ-VL"	* "Same as FLJ-VL"
Input Voltage	±Vcc	* "Same as FLJ-VL"	* "Same as FLJ-VL"
Control Input Voltage	±Vcc	* "Same as FLJ-VL"	* "Same as FLJ-VL"
FILTER CHARACTERISTICS			
Frequency Set Range	100Hz ~ 100KHz	200Hz ~ 20KHz	20Hz ~ 20KHz
Frequency Set Accuracy	± (3%+0.01% F.S.) max.	*	*
Control Input Voltage Range	+10mV ~ +10V	+100mV ~ +10V	+10mV ~ +10V
Control Input Impedance	50 Kohm min.	*	*
Characteristic	4 pole Butterworth	2 pole pair Butterworth	4 pole Butterworth
Rolloff	24dB/oct	12dB/oct BW(Q=5)	24dB/oct
Pass Gain vs. Control Input V.	±0.5dB	±1dB	±0.5dB
Distortion	0.1% max.	*	*
Frequency Set T.C.	±0.03%/°C	*	*
AMPLIFIER CHARACTERISTICS			
Input Voltage	±10V min.	±2V min.	±10V min.
Rated Input Voltage	±1V	*	*
Input Impedance	50 Kohm min.	*	*
Offset Voltage	±10mV Zero Adjustable	*	*
Offset V. Variance vs. Control V.	±20mV max.	*	*
Temperature Drift	300μV/°C	*	*
Noise ①	800μVrms max. @10Hz ~ 300KHz	*	*
Output Voltage/Current	±10V/5mA min.	±2V/5mA min.	±10V/5mA min.
Output Impedance	50ohm max.	*	*
Load Resistance	10Kohm min.	*	*
Small Signal BW	DC ~ fc	-	fc ~ 300KHz
POWER REQUIREMENTS & ENVIRONMENT			
Power Supply Voltage	±15V, +10%, -5%	*	*
Current	±36mA	*	*
Operating Temperature Range	-20°C ~ +70°C	*	*
Operating Humidity Range	10% ~ 95%RH	*	*
Storage Temperature Range	-30°C ~ +80°C	*	*
Storage Humidity Range	10% ~ 80%RH	*	*

① Typically <300 μVrms for the FLJ-VH. The FLJ-VL/VB are typically <300 μVrms for control voltages up to 2V and <500 μVrms for control voltages from 2 to 10 Volts.

TECHNICAL NOTES

1. The rated input voltage is ±1V. The maximum performance is obtained if input voltage does not exceed this range.
2. These filters are 4pole Butterworth (2pole pair) filters. Cutoff frequency is controlled by external voltage. The relationship between control voltage and cutoff frequency is linear (=proportional). Cutoff frequency ranges can be shifted toward lower frequency region if four external capacitors are added. See Figure 3.
   FLJ-VL:
   $$Cext1,\ Cext\ 2 = \frac{1}{fc(max) \times 2\pi \times 6.36 \times 10^3} - 250 \times 10^{-12}$$
   FLJ-VB, VH:
   $$Cext1,\ Cext\ 2 = \frac{1}{fc(max) \times 2\pi \times 6.36 \times 10^3} - 1250 \times 10^{-12}$$
   Cext1, Cext 2 : F (Farad)
   fc(max) : -3dB frequency at 10V control voltage.
3. Zero offset adjustment range is approximately ±50mV.
4. Control input voltage signal has approximately 10KHz of frequency response. However, it takes long time before the output DC offset (=approx. 10mV) settles under the new fc set. It is not recommended to use alternating signals for the control input, depending on applications. The cutoff frequency shall be affected by unstable control voltage if it is small signal, even if it is DC.
5. FLJ-VL can be used as Bessel filter. Connect Rq1 = 95.3KΩ and Rq2 = 9.53KΩ as shown Figure 3. External capacitors should be:
   $$Cext1 = 250\left(\frac{100}{fc(max)\ (KHz) \times 1.43241} - 1\right)$$
   $$Cext2 = 250\left(\frac{100}{fc(max)\ (KHz) \times 1.60594} - 1\right)$$
   fc(max) ≦ 62.2KHz, -3dB frequency at 10V control input voltage.
   Cext1, Cext2 : pF (pico Farad)

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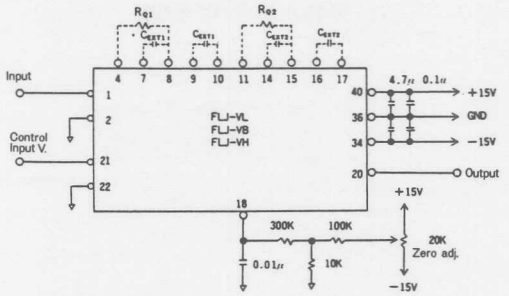
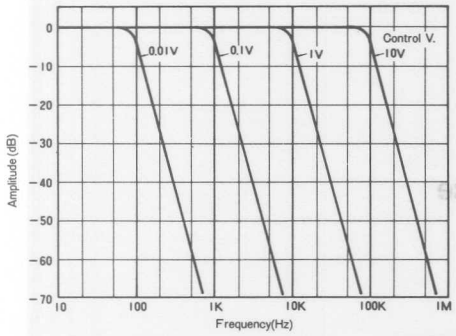
TYPICAL CONNECTION (Fig. 3)

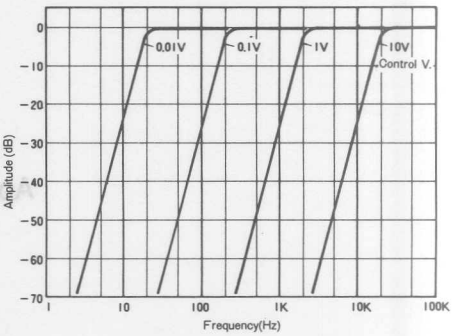


AMPLITUDE VS. FREQUENCY (Fig. 4)

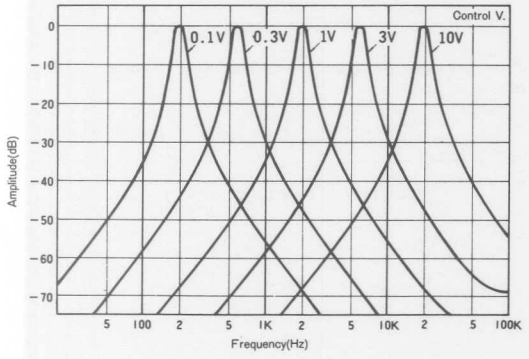
FLJ-VL (Fig. 4-1)



FLJ-VH (Fig. 4-2)



FLJ-VB (Fig. 4-3)



ORDERING INFORMATION

MODEL NO.	DESCRIPTION
FLJ-VL	Low-pass filter Butterworth 4 pole
FLJ-VB	Band-pass filter Butterworth 4 pole
FLJ-VH	High-pass filter Butterworth 4 pole

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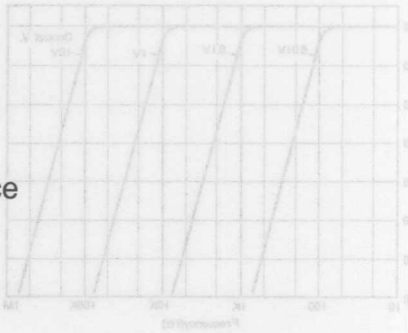

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FLT-C1

Programmable 7th Order, Low-pass, Switched Capacitor Active Filter

FEATURES

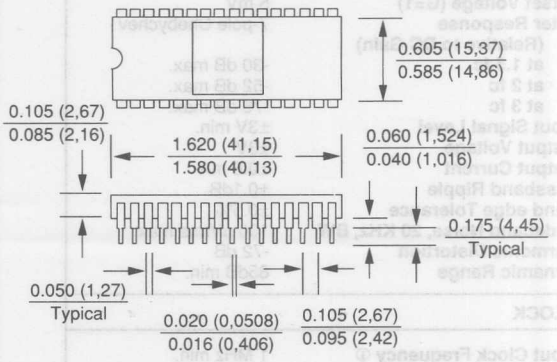
- **Digital tuning**
- **Stopband attenuation >76dB at 3*f*C**
- **Built-in sample-hold**
- **Programmable gain of 1, 2, 4, 8**
- **Dynamic range of 85dB**
- **12-Bit precision**

DESCRIPTION

DATEL's Model FLT-C1 is a monolithic, 7th order, lowpass active filter for applications requiring sharp, fast attenuation rolloff. Exceptionally low noise performance of this switched capacitor filter permit it to be used in applications requiring 12-bit accuracy.

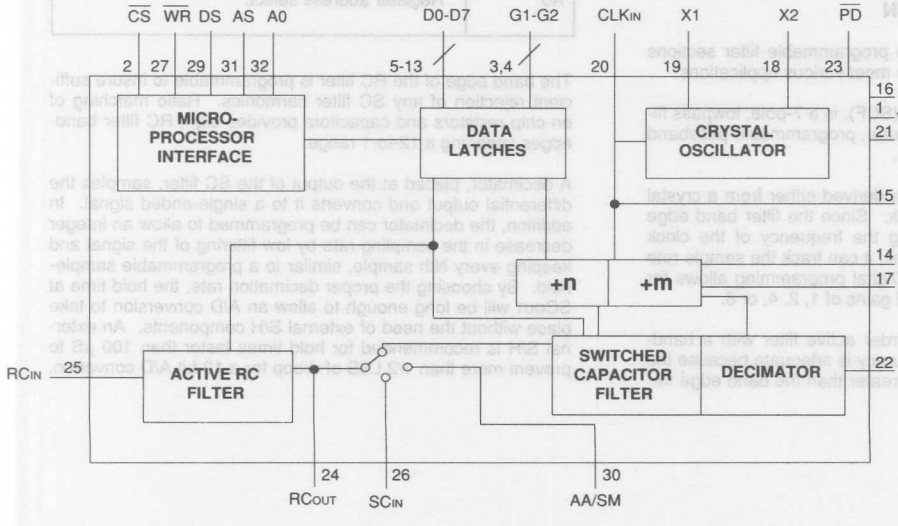
A combination of an 8-bit control input and the clock frequency set the corner frequency over a range of 78 Hz to 20 KHz. A 2-bit control input selects the gain. A built-in oscillator (less crystal) is provided for systems where a system clock is not available.

FLT-C1 Mechanical Dimensions



ORDERING INFORMATION

MODEL	DESCRIPTION
FLT-C1	7th Order, Low-pass, Switched Capacitor Active Filter



FUNCTIONAL SPECIFICATIONS

Typical at 25 °C range unless otherwise noted. Specifications subject to change without notice.

FILTER CHARACTERISTICS	
Frequency Range	78 Hz to 20 KHz
Voltage Gain	1, 2, 4, or 8
Gain Accuracy (G=1)	±0.1%
Offset Voltage (G=1)	5 mV
Filter Response	7-pole Chebychev
(Relative to DC Gain)	
at 1.5 fc	-30 dB max.
at 2 fc	-52 dB max.
at 3 fc	-76 dB max.
Input Signal Level	±3V min.
Output Voltage	±3V
Output Current	±0.6 mA
Passband Ripple	±0.1dB
Band edge Tolerance	±0.5%
Wideband Noise, 20 KHz, BW	100 µVrms max.
Harmonic Distortion	-72 dB
Dynamic Range	85dB min.
CLOCK	
Input Clock Frequency ①	1 MHz min. 4 MHz typ.
DIGITAL INPUTS	
Input High	2.0V min.
Input Low	0.8V max.
Leakage Current	1 µA max.
Input Capacitance	10 pF max.
POWER SUPPLY REQUIREMENTS	
Supply Voltage	±5V (±5%)
Supply Current	±15 mA
Power Dissipation	150 mW

① Also internal clock frequency. Internal clock requires external crystal.

Pin Functions

Name	Function
VSS	Negative supply voltage.
CS	Chip select; active low.
G1-G2	The digital inputs that control the DC gain of the SC filter.
D0-D7	The digital inputs that control the RC filter band edge, SC filter band edge, and SC filter decimation rate.
$\overline{\text{SYNC}}$	This digital input controls the sampling instant for the SC filter decimated output; active low.
CLKOUT	Master clock output capable of driving 1 standard TTL load. It is a buffered version of either CLKIN or the internally generated crystal oscillator output.
VDD	Positive supply voltage
$\overline{\text{CNVRT}}$	This digital output indicates that the SCOUT output has settled and can now be converted or sampled (drive capatibility is 1 standard TTL load); active low.
X1-X2	An external crystal is connected between these pins to generate an accurate clock for chip operation.
CLKIN	The master clock input. Forcing CLKIN to VSS enables the on-chip oscillator (external crystal).
GND	Ground.
SCOUT	SC filter output.
$\overline{\text{PD}}$	This digital input is used to power down the analog circuitry; active low.
RCOUT	RC filter output.
RCIN	RC filter input.
SCIN	SC filter input (only valid when AA/$\overline{\text{SM}}$ is forced low).
$\overline{\text{WR}}$	Write strobe; active low.
DS	Data strobe.
AA/$\overline{\text{SM}}$	This digital input controls whether the input to the SC filter comes from RCOUT or SCIN.
AS	Address strobe.
A0	Register address select.

FUNCTIONAL DESCRIPTION

The FLT-C1 is made up of two programmable filter sections used in different combinations to meet various applications.

The **switched capacitor stage** (SCF), is a 7-pole, lowpass filter designed to provide an accurate, programmable passband for fixed or dynamic applications.

The switching frequency may be derived either from a crystal oscillator or from a system clock. Since the filter band edge can be programmed by varying the frequency of the clock which controls the filter's switches, it can track the sample rate of an external A/D converter. Digital programming allows for band edges of up to 20 KHz and gains of 1, 2, 4, or 8.

The **RC filter stage** is a low-order active filter with a band-edge accuracy of 5%. This accuracy is adequate because the filter sampling rate is 50 times greater than the band edge frequency.

The band edge of the RC filter is programmable to insure sufficient rejection of any SC filter harmonics. Ratio matching of on-chip resistors and capacitors provides eight RC filter band-edges spanning a 12-to-1 range.

A decimator, placed at the output of the SC filter, samples the differential output and converts it to a single-ended signal. In addition, the decimator can be programmed to allow an integer decrease in the sampling rate by low filtering of the signal and keeping every Nth sample, similar to a programmable sample-hold. By choosing the proper decimation rate, the hold time at SCOUT will be long enough to allow an A/D conversion to take place without the need of external S/H components. An external S/H is recommended for hold times faster than 100 µS to prevent more than 1/2 LSB of droop for a 12-bit A/D converion.

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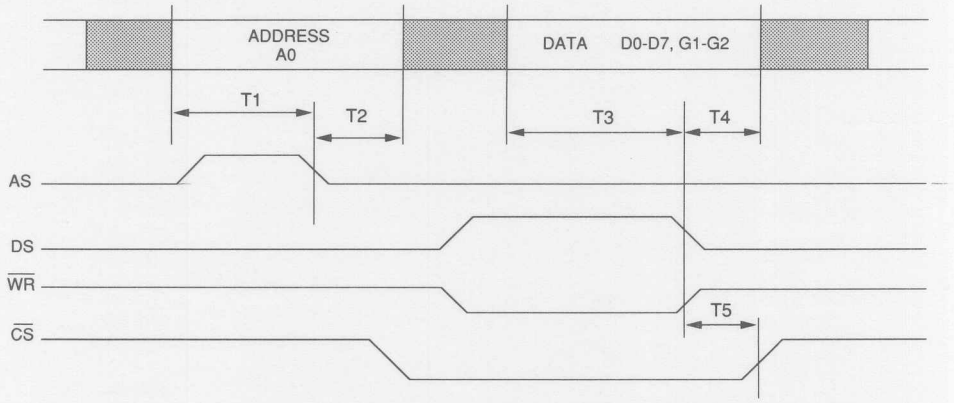
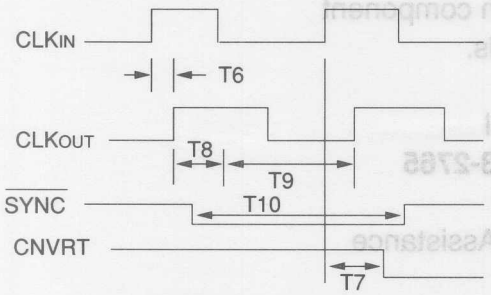
Microprocessor Interface Timing Characteristics



SCOUT Synchronization Timing



µP Interface Timing	Ref.	Duration
CS Hold Time	T5	10 nSec. min.
Data Hold Time	T4	10 nSec. min.
Data Set-up Time	T3	100 nSec. min.
Address Hold Time	T2	10 nSec. min.
Address Set-up Time	T1	20 nSec. min.

SCOUT	Ref.	Duration
Synchronization Timing		
SyncB Delay Time	T8	100 nSec. min.
SyncB Set-up Time	T9	75 nSec. min.
CLKIN To CLKOUT Delay	T6	50 nSec. max.
CLKIN To CNVRT Delay	T7	75 nSec. max.
Sync Pulse Width	T10	75 nSec. min.

RCF band edge

RCF 3dB BW	D7	D6	D5
80 KHz	0	0	0
56KHz	0	0	1
40KHz	0	1	0
28KHz	0	1	1
14KHz	1	0	1
10KHz	1	1	0
7KHz	1	1	1

DC Gain

DC Gain	G1	G2
1	1	1
2	1	0
4	0	1
8	0	0

Clock to SCF bandedge Divide Down Ratio

f_{CLK}/f_C	D0	D1	D2
200	0	0	0
400	0	0	1
800	0	1	0
1,600	0	1	1
3,200	1	0	0
6,400	1	0	1
12,800	1	1	X

Decimator Sample Rate

$f_{S/H}/f_C$	D3	D4
25.000	0	0
12.500	0	1
6.250	1	0
4.167	1	1

f_C = 0.1dB Bandwidth of the SC filter.
f_{CLK} = Master clock frequency at CLKOUT.
$f_{S/H}$ = Sample rate at SCOUT output.

TOP VIEW

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FLT-DL

4-and 5-Pole High Frequency Digitally Programable Active Filters

FEATURES

- **Digitally programmable**
- **4- and 5-Pole Cauer response**
- **Cascadable 7 Pole Cauer response**
- **Cutoff Frequencies to 1.2 MHz**
- **Small 32-pin DIP**
- **-55 °C to +125 °C operation**

GENERAL DESCRIPTION

DATEL's FLT-DL series of 4- and 5-pole digitally programmable active filters are functionally complete, simple to use, and offer a wide range of frequency response options. The models offered operate over the frequency ranges of 100 KHz to 470 KHz and 250 KHz to 1200 KHz.

The FLT-DL Series are Cauer response filters which can be cascaded to provide equivalent 7 pole Cauer performance.

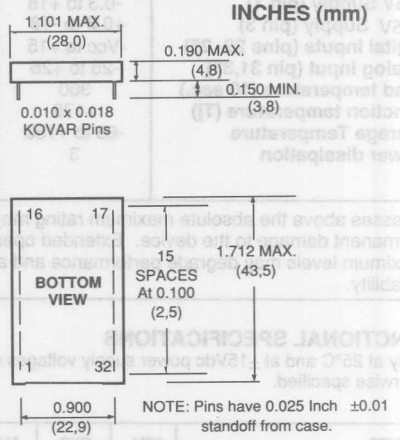
DATEL's FLT-DL Series filters are manufactured using thick-film and thin-film hybrid technology and unique laser trimming schemes. These filters are packaged in a space-saving 32-pin ceramic DIP. Units are specified for operation over the commercial temperature range of 0 to +70 °C and the military temperature range of -55 to +125 °C.

TECHNICAL NOTES

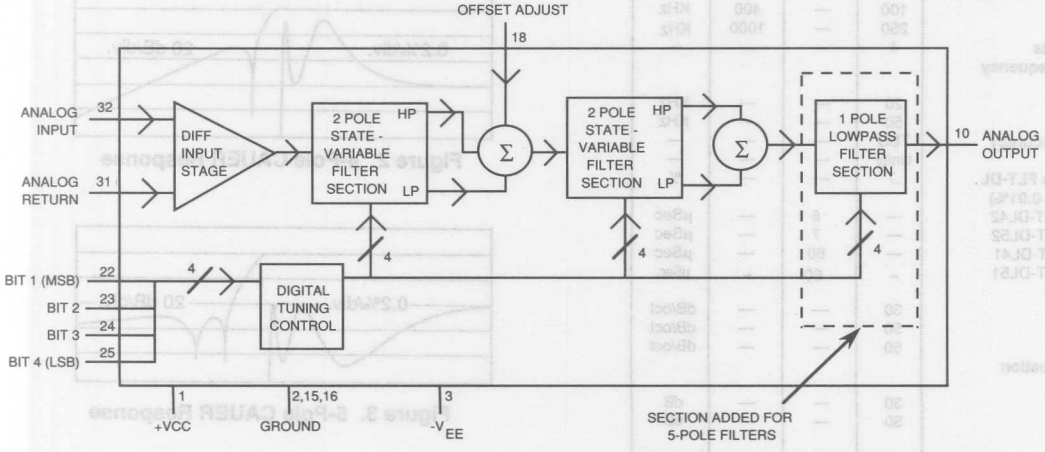
1. Use an external 50 Kohm potentiometer to reduce the small initial offset error to zero. Tie the wiper to pin 18, OFFSET ADJUST. Connect the other terminals of the potentiometer to the +/-15 volt power supplies. For operation without adjustments, leave pin 18 unconnected.

MECHANICAL DIMENSIONS

INCHES (mm)



PIN	FUNCTION
1	+VCC
2	GROUND
3	-VEE
4-9	NO CONNECTION
10	ANALOG OUT
11-14	NO CONNECTION
15	GROUND
16	GROUND
17	NO CONNECTION
18	OFFSET ADJUST
19-21	NO CONNECTION
22	BIT 1 (MSB)
23	BIT 2
24	BIT 3
25	BIT 4 (LSB)
26-30	NO CONNECTION
31	ANALOG RETURN
32	ANALOG INPUT



ABSOLUTE MAXIMUM RATINGS

PARAMETERS	LIMITS	UNITS
+15V Supply (pin 1)	-0.3 to +18	V dc
-15V Supply (pin 3)	+0.3 to -18	V dc
Digital inputs (pins 22- 25)	-Vcc to +15	Vdc
Analog input (pin 31,32)	-25 to +25	V dc
Lead temperature (10 sec.)	300	°C
Junction temperature (Tj)	+175	°C
Storage Temperature	-65 to +150	°C
Power dissipation	3	Watts

Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

FUNCTIONAL SPECIFICATIONS

Apply at 25°C and at ±15Vdc power supply voltages unless otherwise specified.

INPUTS	MIN	TYP	MAX	UNITS
Input Voltage Range	±10	—	—	Volts
Input Impedance (Noninverting)				
Pin 1	4	—	—	Kohms
Pin 3	6	—	—	Kohms
DIGITAL INPUTS				
Logic Threshold		.1Vcc ±20%		Volts
Logic Input Impedance	100	—	—	Kohms
OUTPUT CHARACTERISTICS				
Output Voltage Range	±10	—	—	Volts
DC Output Resistance	1	—	—	Ohms
Output Current Limit				
(Short Circuit Protected)	—	—	±25	mA
Recommended Load Resistance	2	–	—	Kohms
FILTER CHARACTERISTICS				
Freq. Range (cascaded pair)				
FLT-DL41/51	100	—	400	KHz
FLT-DL42/52	250	—	1000	KHz
Programming Bits	4	—	—	—
Programming Frequency Increments				
FLT-DL41/51	20	—	—	KHz
FLT-DL42/52	50	—	—	KHz
Programming Accuracy	TBD	—	—	—
Voltage Gain	Unity	—	—	—
Passband Ripple FLT-DL	.7	—	—	%
Settling Time (to 0.01%)				
fc=1MHz FLT-DL42	—	6	—	µSec
FLT-DL52	—	7	—	µSec
fc=100KHz FLT-DL41	—	60	—	µSec
FLT-DL51	–	60	–	µSec.
Transition Slope				
FLT-DL41/42	30	—	—	dB/oct
FLT-DL51/52	50	—	—	dB/oct
FLT-DL4/5	80	—	—	dB/oct
StopBand Attenuation (to 10MHz)				
FLT-DL41/42	30	—	—	dB
FLT-DL51/52	50	—	—	dB

FILTER CHARACTERISTICS CONT.	MIN	TYP	MAX	UNITS
Offset Voltage	—	—	TBD	—
Offset Voltage Drift				
0 to +70 °C	—	—	TBD	—
-55 to +125 °C	—	—	TBD	—
Noise	—	—	TBD	—
POWER REQUIREMENTS				
Rated Voltage	±14.25	±15	±15.75	Volts
Quiescent Current FLT-DL5	±70	—	—	mA
FLT-DL4	±60	—	—	mA
Power Dissipation	—	—	3	W
PHYSICAL/ENVIRONMENTAL				
Operating Temperature Range			MC 0 to +70 °C MM -55 to + 125 °C	
Storage Temperature Range			-65 to +150 °C	
Case			Ceramic 32-Pin DIP	
Weight			TBD	

2. Bypass each power supply with a 0.1 microfarad tantalum electrolytic capacitor.

3. Digital inputs are binary. The truth table (Table 1) details the cutoff frequency for each filter and for cascaded pairs of filters as a function of input coding.

4. The frequency responses of the 4-pole and 5-pole Gauer filters are shown in Figures 2 and 3 respectively. Figure 4 details the response of a cascaded pair of frequency matched 4- and 5-pole filters. The response for a cascaded pair is similar to a 7-pole Gauer, as shown in Figure 5.

5. When cascading a 4-and a 5-pole filter pair, the order of connection is not important. The filters must, however, be frequency matched.

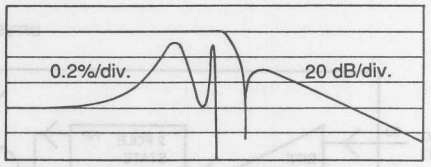


Figure 2. 4-Pole CAUER Response

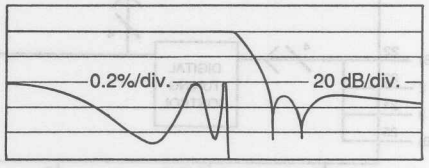


Figure 3. 5-Pole CAUER Response

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Table 1. Cutoff Frequencies for Digitally Tuned Filters, and for Cascaded Combinations of Two Filters

DIGITAL INPUT (BIN)	CUTOFF FREQUENCY (KHz)					
					CASCADED	
	FLT-DL41	FLT-DL42	FLT-DL51	FLT-DL52	41X51	42X52
0000	103.8	259.5	121.5	303.8	100	250
0001	124.6	311.4	145.0	364.5	120	300
0010	145.3	363.3	170.1	425.3	140	350
0011	166.1	415.2	194.4	486.0	160	400
0100	186.8	467.1	218.7	546.8	180	450
0101	207.6	519.0	243.0	607.5	200	500
0110	228.4	570.9	267.3	668.3	220	550
0111	249.1	622.8	291.6	729.0	240	600
1000	269.9	674.7	315.9	789.8	260	650
1001	290.6	726.6	340.2	850.5	280	700
1010	311.4	778.5	364.5	911.3	300	750
1011	332.2	830.4	388.8	972.0	320	800
1100	352.9	882.3	413.1	1032.8	340	850
1101	373.7	934.2	437.4	1093.5	360	900
1110	394.4	986.1	461.7	1154.3	380	950
1111	415.2	1038.0	468.0	1215.0	400	1000

Figure 4. 4- and 5-Pole Pair Response

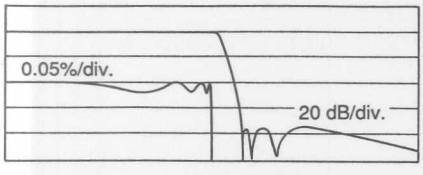

Figure 5. 7-Pole CAUER Response

ORDERING INFORMATION

MODEL NO.	DESCRIPTION	TEMP. RANGE
FLT-DL41MC	100 KHz,4 Pole	0 to 70 °C
FLT-DL41MM	100 KHz,4 Pole	-55 to 125 °C
FLT-DL51MC	100 KHz,5 Pole	0 to 70 °C
FLT-DL51MM	100 KHz,5 Pole	-55 to 125 °C
FLT-DL42MC	250 KHz, 4 Pole	0 to 70 °C
FLT-DL42MM	250 KHz, 4 Pole	-55 to 125 °C
FLT-DL52MC	250 KHz, 5 Pole	0 to 70 °C
FLT-DL52MM	250 KHz, 5 Pole	-55 to 125 °C

Receptacle for PC board mounting can be ordered through AMP Inc., Part #3-331272-8 (Component Lead Socket) 24 required.

For availability of MIL-STD-883 versions, contact DATEL.

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FLT-U2
Micro-electronic Universal Active Filter

FEATURES

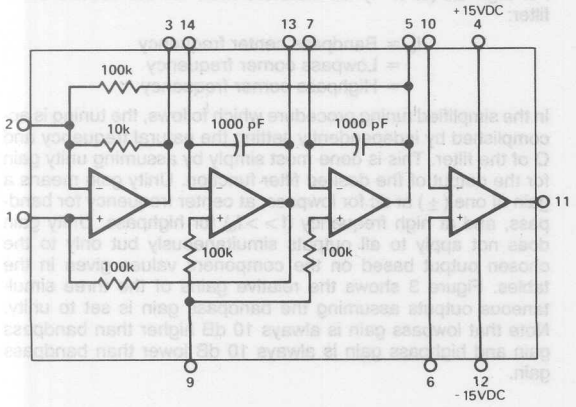
- State variable filter
- LP, BP, or HP functions
- 2-pole response
- Low-noise operational amplifiers
- -55°C to +125°C operation
- Low cost

GENERAL DESCRIPTION

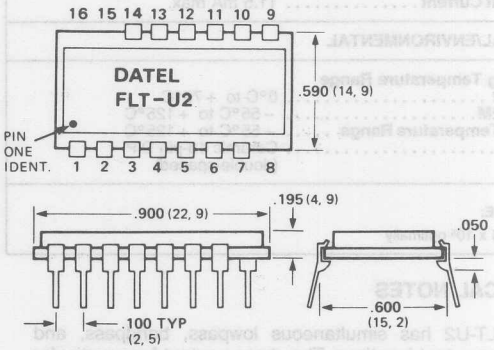
The FLT-U2 is a universal active filter manufactured with a thick-film hybrid technology. It uses the state variable active filter principle to implement a second order transfer function. Three committed operational amplifiers are used for the second order function while a fourth uncommitted operational amplifier can be used a a gain stage, summing amplifier, buffer amplifier or to add another independent real pole.

Two-pole low-pass, bandpass, and highpass output functions are available simultaneously from three different outputs, and notch and allpass functions are available by combining these outputs in the uncommitted operational amplifier. To realize higher order filters, several FLT-U2's can be cascaded. Q range is from 0.1 to 1,000 and resonant frequency range is 0.001Hz to 200kHz. Frequency stability is 0.01%/°C and resonant frequency accuracy is within ±5% of calculated values. Frequency tuning is done by two external resistors and Q tuning by a third external resistor. For resonant frequencies below 50Hz, two external tuning capacitors must be added. Exact tuning of the resonant frequency is done by varying one of the resistors around its calculated value.

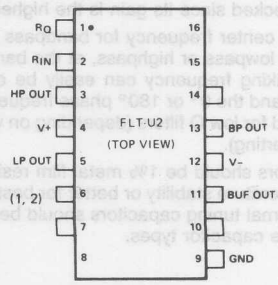
The internal operational amplifiers in the FLT-U2 have 3 MHz gain bandwidth products and a wideband input noise specification of only 10nV/√Hz.



MECHANICAL DIMENSIONS INCHES (MM)



CONNECTIONS DIAGRAM



FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±15V supplies, unless otherwise stated.

FILTER CHARACTERISTICS	
Frequency Range[1]	0.001 Hz to 200 kHz
Q Range[1]	0.1 to 1.000
f_0 Accuracy	±5%
f_0 Temperature Coefficient	0.01%/°C
Voltage Gain[1]	0.1 to 1.000
AMPLIFIER CHARACTERISTICS	
Input Offset Voltage	0.5 mV typ., 6 mV max.
Input Bias Current	40 nA typ., 500 nA max.
Input Offset Current	5 nA typ., 200 nA max.
Input Impedance	5 Megohms
Input Com. Mode Voltage Range	±12V min.
Input Voltage Noise, wideband	10 nV/√Hz
Output Voltage Range	±10V min.
Output Current	±5 mA min.
Open Loop Voltage Gain	300,000
Common Mode Rejection Ratio	100 dB
Power Supply Rejection	10 μV/V
Unity Gain Bandwidth	3 MHz
Slew Rate	1 V/μsec.
POWER SUPPLY REQUIREMENTS	
Voltage, rated performance	±15V dc
Voltage Range, operating	±5V to ±18V
Quiescent Current	11.5 mA max.
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	
FLT-U2	0°C to +70°C
FLT-U2M	−55°C to +125°C
Storage Temperature Range	−55°C to +125°C
Case	Ceramic 16-pin DIP (double-spaced)

FOOTNOTE:

1. $f_0Q \leq 5 \times 10^5$ optimally

TECHNICAL NOTES

1. The FLT-U2 has simultaneous lowpass, bandpass, and highpass output functions. The chosen output for a particular function will be at unity gain based on Tables II and III. This means that the other two unused outputs will be at other gain levels. The gain of the lowpass output is always 10 dB higher than the gain of the bandpass output and 20 dB higher than the gain of the highpass output.
2. When tuning the filter and checking it over its frequency range, the outputs should be checked with a scope to make sure there is no waveform clipping present, as this will affect the operation of the filter. In particular the lowpass output should be checked since its gain is the highest.
3. Check f_1, the center frequency for bandpass and the cutoff frequency for lowpass or highpass, at the bandpass output. Here the peaking frequency can easily be determined for high Q filters and the 0° or 180° phase frequency can easily be determined for low Q filters (depending on whether inverting or noninverting).
4. Tuning resistors should be 1% metal film resistors with 100 ppm/°C temperature stability or better for best performance. Likewise external tuning capacitors should be NPO ceramic or other stable capacitor types.

THEORY OF OPERATION

The FLT-U2 block diagram is shown in Figure 1. This is a second order state-variable filter using three operational amplifiers. Lowpass, bandpass, and highpass transfer functions are simultaneously produced at its three output terminals. These three transfer functions are characterized by the following second order equations:

$$H(s) = \frac{K_1}{S^2 + \frac{\omega_0}{Q}S + \omega_0^2} \quad \text{LOWPASS}$$

$$H(s) = \frac{K_2 S}{S^2 + \frac{\omega_0}{Q}S + \omega_0^2} \quad \text{BANDPASS}$$

$$H(s) = \frac{K_3 S^2}{S^2 + \frac{\omega_0}{Q}S + \omega_0^2} \quad \text{HIGHPASS}$$

where K_1, K_2, and K_3 are arbitrary gain constants.

A second order system is characterized by the location of its poles in the s-plane as shown in Figure 2. The natural radian frequency of this system is ω_0. In Hertz this is $f_0 = \frac{\omega_0}{2\pi}$.

The resonant radian frequency of the circuit is different from the natural radian frequency and is:

$$\omega_1 = \omega_0 \sin \phi = \sqrt{\omega_0^2 - \sigma_1^2}$$

The damping factor d determines the amount of peaking in the filter frequency response and is defined as:

$$d = \cos \phi$$

The point at which the peaking becomes zero is called critical damping and is $d = \sqrt{2}/2$.

Q is found from d and is a measure of the sharpness of the resonance of the peaking:

$$Q = \frac{1}{2d}$$

$$\text{Also, } Q = \frac{f_0}{-3 \text{ dB Bandwidth}} = \frac{\omega_0}{2\sigma_1}$$

For high Q filters the natural frequency and resonant frequency are approximately equal.

$$\omega_1 \simeq \omega_0 \text{ or } f_1 \simeq f_0$$

This is true since $\omega_1 = \omega_0 \sin \phi$ and $\sin \phi \simeq 1$ as the poles move close to the jω axis in the s-plane.

For high Qs ($Q > 1$) we therefore have for the second order filter:

$f_0 \simeq$ Bandpass center frequency
$\simeq$ Lowpass corner frequency
$\simeq$ Highpass corner frequency

In the simplified tuning procedure which follows, the tuning is accomplished by independently setting the natural frequency and Q of the filter. This is done most simply by assuming unity gain for the output of the desired filter function. Unity gain means a gain of one (±) at dc for lowpass, at center frequency for bandpass, and at high frequency ($f >> f_0$) for highpass. Unity gain does not apply to all outputs simultaneously but only to the chosen output based on the component values given in the tables. Figure 3 shows the relative gains of the three simultaneous outputs assuming the bandpass gain is set to unity. Note that lowpass gain is always 10 dB higher than bandpass gain and highpass gain is always 10 dB lower than bandpass gain.

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SIMPLIFIED TUNING PROCEDURE

1. Select the desired transfer function (lowpass, bandpass, or highpass) and inverted or noninverted output. From this determine the filter configuration (inverting or noninverting) using Table I.

TABLE I FILTER CONFIGURATION

	LP	BP	HP
INVERTING INPUT	INV	NON-INV	INV
NONINVERTING INPUT	NON-INV	INV	NON-INV

2. Starting with the desired natural frequency and Q (determined from the filter transfer function or s-plane diagram), compute f_0Q. For $f_0Q > 10^4$ the actual realized Q will exceed the calculated value. At $f_0Q = 10^4$ the increase is about 1% and at $f_0Q = 10^5$ it is about 20%.

3. **Inverting Configuration.** Using the value of Q from Step 2 find R_1 and R_3 from Table II. R_2 is open, or infinite.

TABLE II INVERTING CONFIGURATION

	R_1	R_2	R_3
LOWPASS	100K	OPEN	$\frac{100K}{3.80\ Q-1}$
BANDPASS	Q X 31.6K	OPEN	$\frac{100K}{3.48\ Q}$
HIGHPASS	10K	OPEN	$\frac{100K}{6.64\ Q-1}$

4. **Noninverting Configuration.** Using the value of Q from Step 2 find R_2 and R_3 from Table III. R_1 is open, or infinite.

TABLE III NONINVERTING CONFIGURATION

	R_1	R_2	R_3
LOWPASS	OPEN	$\frac{316K}{Q}$	$\frac{100K}{3.16\ Q-1}$
BANDPASS	OPEN	100k	$\frac{100K}{3.48\ Q-1}$
HIGHPASS	OPEN	$\frac{31.6K}{Q}$	$\frac{100K}{0.316\ Q-1}$

5. Using the value of f_0 from Step 2, set the natural frequency of the filter by finding R_4 and R_5 from the equation:

$$R_4 = R_5 = \frac{5.03 \times 10^7}{f_0}$$

where R_4 and R_5 are in ohms and f_0 is in Hertz. The natural frequency varies as $\sqrt{R_4R_5}$ and therefore one value may be increased and the other decreased and the natural frequency will be constant if the geometric mean is constant. To maintain constant bandwidth at the bandpass output while varying center frequency, fix R_4 and vary R_5.

6. For $f_0 < 50$ Hz the internal 1000 pF capacitors should be shunted with external capacitors across pins 5 & 7 and 13 & 14. If equal value capacitors are used, R_4 and R_5 are then computed from:

$$R_4 = R_5 = \frac{5.03 \times 10^{10}}{f_0C} \text{ (C in pF)}$$

For unequal value capacitors this becomes:

$$R_4 = R_5 = \frac{5.03 \times 10^{10}}{f_0\sqrt{C_1C_2}} \text{ (C_1C_2 in pF)}$$

In both cases the capacitance is the sum of the external values and the internal 1000 pF values.

7. This procedure is based on unity gain output for the desired function. For additional gain, the fourth uncommitted operational amplifier should be used as an inverting or noninverting gain stage following the selected output. See Figure 4. A third pole on the real axis of the s-plane may also be added to the transfer function by adding a capacitor to the gain stage as shown in Figure 5.

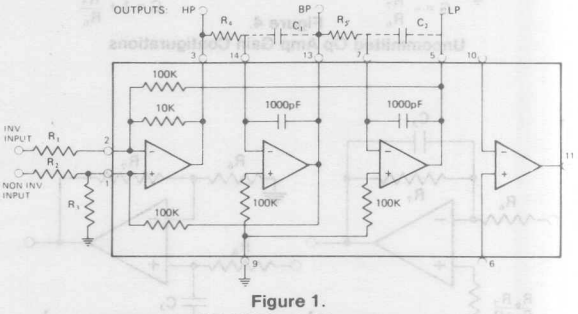

Figure 1.
FLT-U2 Block Diagram

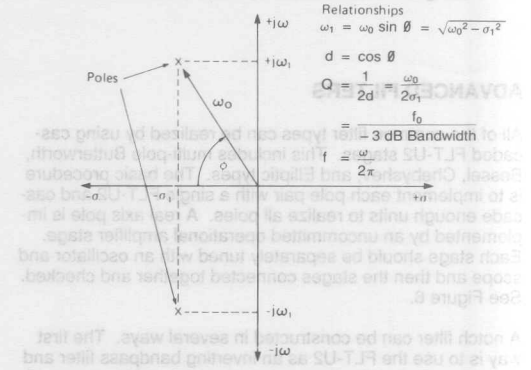

Figure 2.
S-Plane Diagram

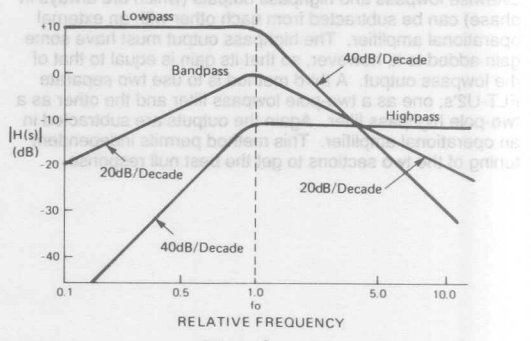

Figure 3.
Relative Gains of Simultaneous Outputs, Q=1

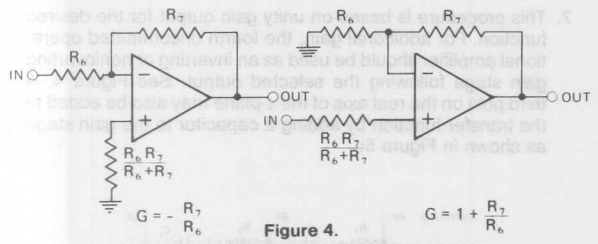

Figure 4.
Uncommitted Op Amp Gain Configurations

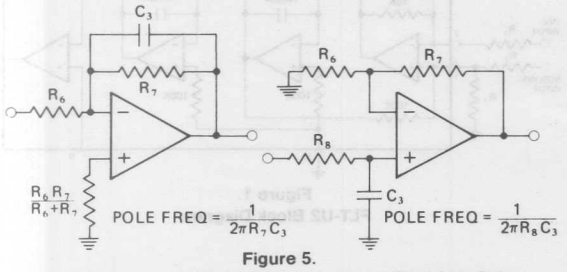

Figure 5.
Using the Uncommitted Op Amp to Add a Real Axis Pole

ADVANCED FILTERS

All of the common filter types can be realized by using cascaded FLT-U2 stages. This includes multi-pole Butterworth, Bessel, Chebyshev, and Elliptic types. The basic procedure is to implement each pole pair with a single FLT-U2 and cascade enough units to realize all poles. A real axis pole is implemented by an uncommitted operational amplifier stage. Each stage should be separately tuned with an oscillator and scope and then the stages connected together and checked. See Figure 6.

A notch filter can be constructed in several ways. The first way is to use the FLT-U2 as an inverting bandpass filter and sum the output of the filter with the input signal by means of the uncommitted operational amplifier. This produces a net subtraction at the center frequency of the bandpass which produces a null at the output of the amplifier. (see Figure 7). Likewise lowpass and highpass outputs (which are always in phase) can be subtracted from each other with an external operational amplifier. The highpass output must have some gain added to it, however, so that its gain is equal to that of the lowpass output. A third method is to use two separate FLT-U2's, one as a two-pole lowpass filter and the other as a two-pole highpass filter. Again the outputs are subtracted in an operational amplifier. This method permits independent tuning of the two sections to get the best null response.

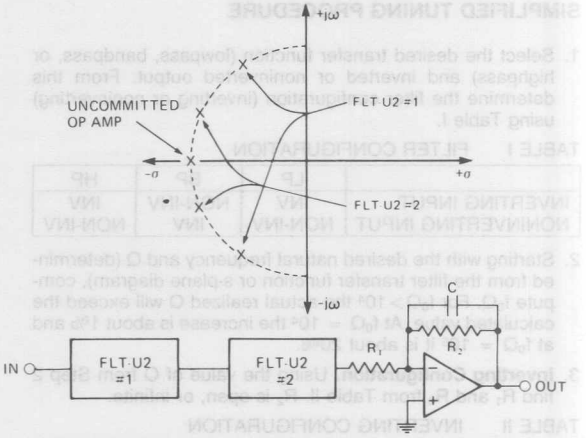

Figure 6.
Realization of a Complex Multipole Filter

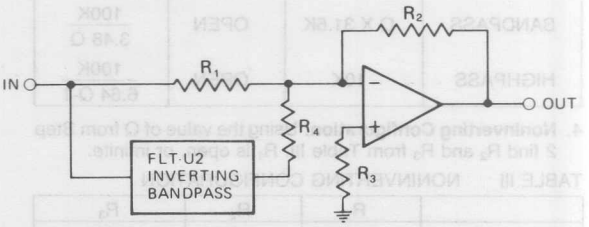

Figure 7.
Realization of Notch Filter

ORDERING INFORMATION

MODEL	OPERATING TEMP. RANGE
FLT-U2	0°C to +70°C
FLT-U2M	−55°C to +125°C

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WIDE-RANGING, DC-DC POWER CONVERTERS

NEW 20 WATT, WIDE-RANGING, DC-DC POWER CONVERTERS (2" x 2" x 0.45")

Input (Vdc)	Output	Input Current No Load/Full Load	Output Noise & RIPPLE (TYP)	Efficiency (Min @ F.L.)	Line/Load Regulation	Model
4.6 - 13.2V (5V, Nom)	3.3V,4.25 A	25 mA/3.78 A	50 mV p-p	75%	±0.2% / ±0.5%	**UWR-3.3/4250-D5**
9.0 - 18V (12V, Nom)	3.3V,4.85 A	20 mA/1.77 A	50 mV p-p	76%	±0.2% / ±0.5%	**UWR-3.3/4850-D12**
18 - 72V (48V, Nom)	3.3V,4.85 A	15 mA/0.843 A	50 mV p-p	79%	±0.2% / ±0.5%	**UWR-3.3/4850-D48**
4.6-13.2V (5V, Nom)	5.0V,3.60 A	10 mA/1.875 A	50 mV p-p	80%	±0.2% / ±0.5%	**UWR-5/3000-D5**
9.0 - 18V (12V, Nom)	5.0V,4.0 A	15 mA/2.032 A	50 mV p-p	82%	±0.2% / ±0.5%	**UWR-5/4000-D12**
18 - 72V (48V, Nom)	5.0V,4.0 A	10 mA/0.505 A	50 mV p-p	82%	±0.2% / ±0.5%	**UWR-5/4000-D48**
4.6-13.2V (5V, Nom)	±12V,0.625 A	40 mA/1.829 A	85 mV p-p	82%	±0.2% / ±1%	**BWR-12/625-D5**
9.0 - 18V (12V, Nom)	±12V,0.830 A	40 mA/2.00 A	75 mV p-p	84%	±0.2% / ±1%	**BWR-12/830-D12**
18 - 72V (48V, Nom)	±12V,0.830 A	10 mA/0.508 A	85 mV p-p	82%	±0.2% / ±1%	**BWR-12/830-D48**
4.6 - 13.2V (5V, Nom)	±15V,0.600 A	40 mA/1.829 A	85 mV p-p	82%	±0.2% / ±1%	**BWR-15/500-D5**
9.0 - 18V (12V, Nom)	±15V,0.670 A	30 mA/1.587 A	85 mV p-p	84%	±0.2% / ±1%	**BWR-15/670-D12**
18 - 72V (48V, Nom)	±15V,0.670 A	10 mA/0.508 A	85 mV p-p	82%	±0.2% / ±1%	**BWR-15/670-D48**

NEW, 10 WATT, WIDE RANGING, DC-DC POWER CONVERTERS (2" x 1" x 0.375")

4.7 - 7.0V (5V, Nom)	3.3V,1.8 A	30 mA/1.715 A	50 mV p-p	70%	±0.2% / ±0.5%	**UWR-3.3/1800-D5**
9.0 - 18V (12V, Nom)	3.3V,2.5 A	30 mA/0.915 A	50 mV p-p	75%	±0.2% / ±0.5%	**UWR-3.3/2500-D12**
18 - 72V (48V, Nom)	3.3V,1.80 A	15 mA/0.170 A	50 mV p-p	75%	±0.2% / ±0.5%	**UWR-3.3/1800-D48**
4.7 - 7.0V (5V, Nom)	5.0V,1.60 A	30 mA/2.160 A	50 mV p-p	74%	±0.2% / ±0.5%	**UWR-5/1600-D5**
9.0 - 18V (12V, Nom)	5.0V,2.0 A	15 mA/1.03 A	50 mV p-p	81%	±0.2% / ±0.5%	**UWR-5/2000-D12**
18 - 72V (24/48V)	5.0V,1.80 A	15 mA/0.240 A	50 mV p-p	78%	±0.2% / ±0.5%	**UWR-5/1800-D48**
4.7 - 7.0V (5V, Nom)	±5.0V,0.70 A	30 mA/1.842 A	50 mV p-p	76%	±0.2% / ±1%	**BWR-5/700-D5**
9.0 - 18V (12V, Nom)	±5.0V,0.80 A	15mA/0.830 A	50 mV p-p	80%	±0.2% / ±1%	**BWR-5/800-D12**
4.7 - 7.0V (5V, Nom)	±12V,0.335 A	40 mA/2.1 A	15 mV p-p	76%	±0.2% / ±1%	**BWR-12/335-D5**
9.0 - 18 (12V, Nom)	±12V,0.415 A	35 mA/1.00 A	25 mV p-p	83%	±0.2% / ±1%	**BWR-12/415-D12**
18 - 72V (24/48V, Nom)	±12V,0.415 A	15 mA/0.260 A	50 mV p-p	80%	±0.2% / ±1%	**BWR-12/415-D48**
4.6 - 13.2V (5V, Nom)	±15V,0.275 A	40 mA/2.142 A	15 mV p-p	77%	±0.2% / ±1%	**BWR-15/275-D5**
9.0 - 18V (12V, Nom)	±15V,0.330 A	35 mA/0.992 A	25 mV p-p	84%	±0.2% / ±1%	**BWR-15/330-D12**
18 - 72V (24/48V, Nom)	±15V,0.330 A	15 mA/0.257 A	50 mV p-p	81%	±0.2% / ±1%	**BWR-15/330-D48**

NEW, 3 WATT, WIDE RANGING, DC-DC POWER CONVERTERS (1.25"x0.8"x0.435")

4.5 - 9.0V (5V, Nom)	5.0V,0.50 A	25 mA/0.714 A	100 mV p-p	70%	±0.2% / ±0.5%	**UWR-5/500-D5**
9.0 - 18V (12V, Nom)	5.0V,0.50 A	15 mA/0.278 A	100 mV p-p	70%	±0.2% / ±0.5%	**UWR-5/500-D12**
18 - 72V (48V, Nom)	5.0V,0.50 A	10 mA/0.069 A	100 mV p-p	75%	±0.2% / ±0.5%	**UWR-5/500-D48**
4.5 - 9.0V (5V, Nom)	±12V,0.105 A	25 mA/0.714 A	75 mV p-p	70%	±0.2% / ±1%	**BWR-12/105-D5**
9.0 - 18V (12V, Nom)	±12V,0.125 A	15 mA/0.333 A	75 mV p-p	75%	±0.2% / ±1%	**BWR-12/125-D12**
18 - 72V (48V, Nom)	±12V,0.125 A	10 mA/0.076 A	75 mV p-p	82%	±0.2% / ±1%	**BWR-12/125-D48**
4.5 - 9.0V (5V, Nom)	±15V,0.085 A	25 mA/0.729 A	75 mV p-p	70%	±0.2% / ±1%	**BWR-15/85-D5**
9.0 - 18V (12V, Nom)	±15V,0.100 A	15 mA/0.333 A	75 mV p-p	75%	±0.2% / ±1%	**BWR-15/100-D12**
18 - 72V (48V, Nom)	±15V,0.100 A	10 mA/0.076 A	75 mV p-p	82%	±0.2% / ±1%	**BWR-15/100-D48**

WIDE INPUT RANGE DC/DC CONVERTERS

INPUT	OUTPUT	NO LOAD/FULL LOAD INPUT CURRENT	LINE/LOAD REGULATION	EFFICIENCY	MODEL
9-18V dc	5V dc, 3000 mA	30 mA / 1700 mA	0.02% / 1.0%	75%	**UPS-5/3000-D12**
9-18V dc	12V dc, 1250 mA	30 mA / 1600 mA	0.02% / 1.0%	78%	**UPS-12/1250-D12**
9-18V dc	15V dc, 1000 mA	30 mA / 1600 mA	0.02% / 1.0%	78%	**UPS-15/1000-D12**
9-18V dc	5V dc, 5000 mA	30 mA / 2800 mA	0.02% / 1.0%	75%	**UPS-5/5000-D12**
9-18V dc	12V dc, 2500 mA	30 mA / 3200 mA	0.02% / 1.0%	78%	**UPS-12/2500-D12**
9-18V dc	15V dc, 2000 mA	30 mA / 3200 mA	0.02% / 1.0%	78%	**UPS-15/2000-D12**
18-36V dc	5V dc, 3000 mA	20 mA / 810 mA	0.02% / 1.0%	77%	**UPS-5/3000-D24**
18-36V dc	12V dc, 1250 mA	20 mA / 780 mA	0.02% / 1.0%	80%	**UPS-12/1250-D24**
18-36V dc	15V dc, 1000 mA	20 mA / 780 mA	0.02% / 1.0%	80%	**UPS-15/1000-D24**
18-36V dc	5V dc, 5000 mA	20 mA / 1350 mA	0.02% / 1.0%	77%	**UPS-5/5000-D24**
18-36V dc	12V dc, 2500 mA	20 mA / 1550 mA	0.02% / 1.0%	80%	**UPS-12/2500-D24**
18-36V dc	15V dc, 2000 mA	20 mA / 1550 mA	0.02% / 1.0%	80%	**UPS-15/2000-D24**
9-18V dc	±12V dc, ±625 mA	25 mA / 1520 mA	0.02% / 1.0%	82%	**BPS-12/625-D12**
9-18V dc	±15V dc, ±500 mA	25 mA / 1520 mA	0.02% / 1.0%	82%	**BPS-15/500-D12**
9-18V dc	±12V dc, ±1250 mA	25 mA / 3050 mA	0.02% / 1.0%	82%	**BPS-12/1250-D12**
9-18V dc	±15V dc, ±1000 mA	25 mA / 3050 mA	0.02% / 1.0%	82%	**BPS-15/1000-D12**
18-36V dc	±12V dc, ±625 mA	25 mA / 750 mA	0.02% / 1.0%	84%	**BPS-12/625-D24**
18-36V dc	±15V dc, ±500 mA	25 mA / 750 mA	0.02% / 1.0%	84%	**BPS-15/500-D24**
18-36V dc	±12V dc, ±1250 mA	25 mA / 1500 mA	0.02% / 1.0%	84%	**BPS-12/1250-D24**
18-36V dc	±15V dc, ±1000 mA	25 mA / 1500 mA	0.02% / 1.0%	84%	**BPS-15/1000-D24**
9-18V dc	+5/±12V dc, 1500/±310 mA	50 mA / 1600 mA	1.0% / 5.0%	78%	**TPS-5/1500-12/310-D12**
9-18V dc	+5/±15V dc, 1500/±250 mA	50 mA / 1600 mA	1.0% / 5.0%	78%	**TPS-5/1500-15/250-D12**
9-18V dc	+5/+12/-5V dc, 1500/+310/500 mA	50 mA / 1470 mA	1.0% / 5.0%	78%	**TPS-12/310-5/1500-D12**
18-36V dc	+5/±12V dc, 1500/±310 mA	40 mA / 780 mA	1.0% / 5.0%	80%	**TPS-5/1500-12/310-D24**
18-36V dc	+5/±15V dc, 1500/±250 mA	40 mA / 780 mA	1.0% / 5.0%	80%	**TPS-5/1500-15/250-D24**
18-36V dc	+5/+12/-5V dc, 1500/+310/500 mA	40 mA / 715 mA	1.0% / 5.0%	80%	**TPS-12/310-5/1500-D24**

MINIATURE DC/DC CONVERTERS

INPUT	OUTPUT	NO LOAD/FULL LOAD INPUT CURRENT	LINE/LOAD REGULATION	OUTPUT NOISE & RIPPLE (MAX)[1]	REFLECTED RIPPLE	ISOLATION VOLTAGE MIN	MODEL
5V dc	12V dc, 80 mA	90 mA / 380 mA	0.3% / 0.4%	20 mV p-p	15 mA p-p	300V dc	**UPS-12/80-D5**
5V dc	15V dc, 65 mA	90 mA / 380 mA	0.3% / 0.4%	20 mV p-p	15 mA p-p	300V dc	**UPS-15/65-D5**
5V dc	±12V dc, ±40 mA	90 mA / 380 mA	0.3% / 0.4%	20 mV p-p	15 mA p-p	300V dc	**BPS-12/40-D5**
5V dc	±15V dc, ±33 mA	90 mA / 380 mA	0.3% / 0.4%	20 mV p-p	15 mA p-p	300V dc	**BPS-15/33-D5**

NOTE 1. 15µF capacitor across each output.

PLUG-IN ADAPTERS

OUTPUT VOLTAGE	RATED OUTPUT CURRENT	LINE/LOAD REGULATION	OUTPUT RIPPLE (MAX)	MODEL
4.8 to 5.3V dc	500mA	0.3% / 0.3%	8 mV RMS	**UPA-5/500**
11.5 to 12.5V dc	200mA	0.3% / 0.3%	8 mV RMS	**UPA-12/200**

1W – 10W DC/DC CONVERTERS

INPUT	OUTPUT	NO LOAD/FULL LOAD REGULATION	LINE/LOAD REGULATION	TEMP. COEF.	OUTPUT NOISE & RIPPLE (MAX)	REFLECTED RIPPLE MAX	MODEL
12V	5V, 200 mA	100 mA / 220 mA	0.05% / 0.1%	0.02% / °C	20 mV p-p	1 V mA p-p	**UPM-5/200-D12**
28V	5V, 200 mA	40 mA / 100 mA	0.05% / 0.1%	0.02% / °C	20 mV p-p	5 mA p-p	**UPM-5/200-D28**
5V	12V, 80 mA	220 mA / 500 mA	0.05% / 0.05%	0.02% / °C	20 mV p-p	25 mA p-p	**UPM-12/80-D5**
5V	24V, 40 mA	220 mA / 500 mA	0.05% / 0.05%	0.02% / °C	20 mV p-p	25 mA p-p	**UPM-24/40-D5**
12V	24V, 40 mA	95 mA / 210 mA	0.05% / 0.05%	0.02% / °C	20 mV p-p	10 mA p-p	**UPM-24/40-D12**
5V	28V, 25 mA	160 mA / 400 mA	0.05% / 0.05%	0.02% / °C	20 mV p-p	20 mA p-p	**UPM-28/25-D5**
12V	28V, 25 mA	80 mA / 180 mA	0.05% / 0.05%	0.02% / °C	20 mV p-p	9 mA p-p	**UPM-28/25-D12**
5V	5V, 600 mA	125 mA / 935 mA	0.02% / 0.04%	0.02% / °C	50 mV p-p	32 mA p-p	**UPS-5/600-D5**
12V	5V, 600 mA	50 mA / 364 mA	0.02% / 0.04%	0.02% / °C	50 mV p-p	24 mA p-p	**UPS-5/600-D12**
28V	5V, 600 mA	20 mA / 135 mA	0.02% / 0.04%	0.02% / °C	50 mV p-p	21 mA p-p	**UPS-5/600-D28**
5V	12V, 250 mA	140 mA / 863 mA	0.02% / 0.04%	0.02% / °C	50 mV p-p	31 mA p-p	**UPS-12/250-D5**
28V	12V, 250 mA	25 mA / 125 mA	0.02% / 0.04%	0.02% / °C	50 mV p-p	21 mA p-p	**UPS-12/250-D28**
12V	24V, 125 mA	125 mA / 530 mA	0.05% / 0.05%	0.02% / °C	20 mV p-p	26 mA p-p	**UPM-24/125-D12**
5V	28V, 100 mA	300 mA / 1350 mA	0.05% / 0.05%	0.02% / °C	20 mV p-p	67 mA p-p	**UPM-28/100-D5**
12V	28V, 100 mA	125 mA / 500 mA	0.05% / 0.05%	0.02% / °C	20 mV p-p	25 mA p-p	**UPM-28/100-D12**
12V	5V, 1000 mA	50 mA / 640 mA	0.02% / 0.04%	0.02% / °C	50 mV p-p	54 mA p-p	**UPS-5/1000-D12**
24V	5V, 1000 mA	25 mA / 320 mA	0.02% / 0.04%	0.02% / °C	50 mV p-p	22 mA p-p	**UPS-5/1000-D24**
28V	5V, 1000 mA	20 mA / 275 mA	0.02% / 0.04%	0.02% / °C	50 mV p-p	22 mA p-p	**UPS-5/1000-D28**
5V	12V, 470 mA	500 mA / 2000 mA	0.02% / 0.04%	0.02% / °C	50 mV p-p	61 mA p-p	**UPS-12/470-D5**
24V	12V, 470 mA	120 mA / 415 mA	0.02% / 0.04%	0.02% / °C	50 mV p-p	26 mA p-p	**UPS-12/470-D24**
5V	24V, 210 mA	500 mA / 2000 mA	0.05% / 0.01%	0.02% / °C	50 mV p-p	100 mA p-p	**UPM-24/210-D5**
12V	24V, 210 mA	200 mA / 830 mA	0.05% / 0.01%	0.02% / °C	50 mV p-p	42 mA p-p	**UPM-24/210-D12**
24V	5V, 2000 mA	45 mA / 640 mA	0.02% / 0.05%	0.02% / °C	50 mV p-p	32 mA p-p	**UPS-5/2000-D24**
28V	5V, 2000 mA	40 mA / 550 mA	0.02% / 0.05%	0.02% / °C	50 mV p-p	33 mA p-p	**UPS-5/2000-D28**
48V	5V, 2000 mA	20 mA / 320 mA	0.02% / 0.05%	0.02% / °C	50 mV p-p	32 mA p-p	**UPS-5/2000-D48**
5V	±12V, ±25 mA	150 mA /350 mA	0.05% / 0.05%	0.02% / °C	20 mV p-p	17 mA p-p	**BPM-12/25-D5**
12V	±12V, ±25 mA	80 mA /165 mA	0.05% / 0.05%	0.02% / °C	20 mV p-p	8 mA p-p	**BPM-12/25-D12**
28V	±12V, ±25 mA	30 mA /65 mA	0.05% / 0.05%	0.02% / °C	20 mV p-p	3 mA p-p	**BPM-12/25-D28**
5V	±15V, ±25 mA	160 mA /400 mA	0.05% / 0.05%	0.02% / °C	20 mV p-p	20 mA p-p	**BPM-15/25-D5**
12V	±15V, ±25 mA	80 mA /80 mA	0.05% / 0.05%	0.02% / °C	20 mV p-p	9 mA p-p	**BPM-15/25-D12**
28V	±15V, ±25 mA	30 mA /80 mA	0.05% / 0.05%	0.02% / °C	20 mV p-p	4 mA p-p	**BPM-15/25-D28**
5V	±12V, ±125 mA	130 mA /965 mA	0.02% / 0.02%	0.01% / °C	35 mV p-p	34 mA p-p	**BPS-12/125-D5**
12V	±12V, ±125 mA	55 mA /380 mA	0.02% / 0.02%	0.01% / °C	35 mV p-p	23 mA p-p	**BPS-12/125-D12**
28V	±12V, ±125 mA	25 mA /145 mA	0.02% / 0.02%	0.01% / °C	35 mV p-p	21 mA p-p	**BPS-12/125-D28**
5V	±15V, ±100 mA	135 mA /955 mA	0.02% / 0.02%	0.01% / °C	35 mV p-p	33 mA p-p	**BPS-15/100-D5**
12V	±15V, ±100 mA	55 mA /376 mA	0.02% / 0.02%	0.01% / °C	35 mV p-p	24 mA p-p	**BPS-15/100-D12**
28V	±15V, ±100 mA	25 mA /143 mA	0.02% / 0.02%	0.01% / °C	35 mV p-p	21 mA p-p	**BPS-15/100-D28**
5V	±15V, ±150 mA	450 mA /1750 mA	0.05% / 0.05%	0.005% / °C	25 mV p-p	87 mA p-p	**BPM-15/150-D5**
24V	±15V, ±150 mA	80 mA /350 mA	0.05% / 0.05%	0.005% / °C	25 mV p-p	18 mA p-p	**BPM-15/150-D24**
28V	±15V, ±150 mA	70 mA /300 mA	0.05% / 0.05%	0.005% / °C	25 mV p-p	15 mA p-p	**BPM-15/150-D28**
5V	±12V, ±230 mA	130 mA /1650 mA	0.02% / 0.02%	0.01% / °C	35 mV p-p	58 mA p-p	**BPS-12/230-D5**
12V	±12V, ±230 mA	55 mA /690 mA	0.02% / 0.02%	0.01% / °C	35 mV p-p	24 mA p-p	**BPS-12/230-D12**
24V	±12V, ±230 mA	25 mA /340 mA	0.02% / 0.02%	0.01% / °C	35 mV p-p	24 mA p-p	**BPS-12/230-D24**
28V	±12V, ±230 mA	25 mA /300 mA	0.02% / 0.02%	0.01% / °C	35 mV p-p	23 mA p-p	**BPS-12/230-D28**
5V	±15V, ±190 mA	135 mA /1700 mA	0.02% / 0.02%	0.01% / °C	35 mV p-p	60 mA p-p	**BPS-15/190-D5**
12V	±15V, ±190 mA	55 mA /710 mA	0.02% / 0.02%	0.01% / °C	35 mV p-p	25 mA p-p	**BPS-15/190-D12**
24V	±15V, ±190 mA	30 mA /350 mA	0.02% / 0.02%	0.01% / °C	35 mV p-p	25 mA p-p	**BPS-15/190-D24**
28V	±15V, ±190 mA	25 mA /300 mA	0.02% / 0.02%	0.01% / °C	35 mV p-p	24 mA p-p	**BPS-15/190-D28**
48V	±15V, ±190 mA	14 mA /180 mA	0.02% / 0.02%	0.01% / °C	35 mV p-p	25 mA p-p	**BPS-15/190-D48**
5V	±12V, ±420 mA	980 mA /4000 mA	0.05% / 0.05%	0.02% / °C	50 mV p-p	120 mA p-p	**BPM-12/420-D5**
12V	±12V, ±420 mA	340 mA /1530 mA	0.05% / 0.05%	0.02% / °C	50 mV p-p	46 mA p-p	**BPM-12/420-D12**
24V	±12V, ±420 mA	175 mA /760 mA	0.05% / 0.05%	0.02% / °C	50 mV p-p	23 mA p-p	**BPM-12/420-D24**
28V	±12V, ±420 mA	130 mA /650 mA	0.05% / 0.05%	0.02% / °C	50 mV p-p	20 mA p-p	**BPM-12/420-D28**
5V	±15V, ±412 mA	260 mA /3700 mA	0.02% / 0.02%	0.01% / °C	35 mV p-p	130 mA p-p	**BPS-15/412-D5**
12V	±15V, ±412 mA	110 mA /1590 mA	0.02% /0.02%	0.01% / °C	35 mV p-p	54 mA p-p	**BPS-15/412-D12**
24V	±15V, ±412 mA	55 mA /770 mA	0.02% / 0.02%	0.01% / °C	35 mV p-p	38 mA p-p	**BPS-15/412-D24**
28V	±15V, ±412 mA	45 mA /660 mA	0.02% / 0.02%	0.01% / °C	35 mV p-p	39 mA p-p	**BPS-15/412-D28**

1W - 10W AC/DC SUPPLIES

OUTPUT VOLTAGE	RATED OUTPUT CURRENT	VOLTAGE ACCURACY	LINE REGULATION	LOAD REGULATION	OUTPUT RIPPLE (MAX)	OUTPUT IMPEDANCE	MODEL
5V dc	250 mA	1.0%	0.05%	0.1%	1 mV RMS	0.05Ω	UPM-5/250
5V dc	500 mA	1.0%	0.05%	0.1%	1 mV RMS	0.05Ω	UPM-5/500
5V dc	1000 mA	1.0%	0.05%	0.1%	1 mV RMS	0.01Ω	UPM-5/1000
5V dc	1000 mA	2.0%	0.25%	0.25%	1 mV RMS	0.01Ω	UPM-5/1000B
5V dc	2000 mA	1.0%	0.05%	0.1%	1 mV RMS	0.005Ω	UPM-5/2000
±5V dc	±250 mA	1.0%	0.05%	0.1%	1 mV RMS	0.05Ω	BPM-5/250
±5V dc	±500 mA	1.0%	0.05%	0.1%	1 mV RMS	0.03Ω	BPM-5/500
±12V dc	±100 mA	2.0%	0.02%	0.05%	2 mV RMS	0.10Ω	BPM-12/100
±12V dc	±200 mA	1.0%	0.02%	0.05%	2 mV RMS	0.05Ω	BPM-12/200
±15V dc	±60 mA	1.0%	0.02%	0.05%	2 mV RMS	0.20Ω	BPM-15/60
±15V dc	±100 mA	1.0%	0.02%	0.05%	2 mV RMS	0.10Ω	BPM-15/100
±15V dc	±200 mA	1.0%	0.02%	0.05%	2 mV RMS	0.05Ω	BPM-15/200
±15V dc	±300 mA	1.0%	0.02%	0.05%	2 mV RMS	0.03Ω	BPM-15/300
±12/5V dc	±100 / 500 mA	1.0%	0.02% / 0.05%	0.05% / 0.1%	2 mV /1 mV RMS	0.10 / 0.05Ω	TPM-12/100-5/500
±12/5V dc	±150 / 1000 mA	1.0%	0.02% / 0.05%	0.05% / 0.1%	2 mV /1 mV RMS	0.10 / 0.05Ω	TPM-12/150-5/1000
±15/5V dc	±100 / 500 mA	1.0%	0.02% / 0.05%	0.05% / 0.1%	2 mV /1 mV RMS	0.10 / 0.05Ω	TPM-15/100-5/500
±15/5V dc	±150 / 1000 mA	1.0%	0.02% / 0.05%	0.05% / 0.1%	2 mV /1 mV RMS	0.10 / 0.05Ω	TPM-15/150-5/1000

CHASSIS MOUNT AC/DC SUPPLIES

OUTPUT VOLTAGE	RATED OUTPUT CURRENT	VOLTAGE ACCURACY	LINE/LOAD REGULATION	OUTPUT RIPPLE (MAX)	OUTPUT IMPEDANCE	MODEL
5V dc	250 mA	1.0%	0.05% / 0.1%	1 mV p-p	0.05Ω	UCM-5/250
5V dc	500 mA	1.0%	0.05% / 0.1%	1 mV p-p	0.05Ω	UCM-5/500
5V dc	1000 mA	1.0%	0.05% / 0.1%	1 mV p-p	0.01Ω	UCM-5/1000
5V dc	2000 mA	1.0%	0.05% / 0.1%	1 mV p-p	0.005Ω	UCM-5/2000
±15V dc	±60 mA	1.0%	0.02% / 0.05%	2 mV p-p	0.20Ω	BCM-15/60
±15V dc	±100 mA	1.0%	0.02% / 0.05%	2 mV p-p	0.10Ω	BCM-15/100
±15V dc	±200 mA	1.0%	0.02% / 0.05%	2 mV p-p	0.05Ω	BCM-15/200
±15V dc	±300 mA	1.0%	0.02% / 0.05%	2 mV p-p	0.05Ω	BCM-15/300

HIGH EFFICIENCY AC/DC SUPPLIES

OUTPUT VOLTAGE	RATED OUTPUT CURRENT	VOLTAGE ACCURACY	LINE/LOAD REGULATION	OUTPUT RIPPLE (MAX)	OUTPUT IMPEDANCE	MODEL
5V dc	5000 mA	80%	0.05% / 0.1%	50 mV p-p	0.002Ω	USM-5/5
5V dc	5000 mA	80%	0.05% / 0.1%	50 mV p-p	0.002Ω	USC-5/5

HIGH VOLTAGE MODULES

OUTPUT VOLTAGE	RATED OUTPUT CURRENT	VOLTAGE ACCURACY	LINE/LOAD REGULATION	OUTPUT RIPPLE (MAX)	OUTPUT IMPEDANCE	MODEL
±120V dc	25 mA	1.0%	0.05% / 0.2%	10 mV RMS	5.0Ω	BPM-120/25
±150V dc	20 mA	1.0%	0.05% / 0.2%	10 mV RMS	5.0Ω	BPM-150/20
±180V dc	16 mA	1.0%	0.05% / 0.2%	10 mV RMS	5.0Ω	BPM-180/16

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VOLTAGE CALIBRATORS

MODEL	OUTPUT RANGE	SETTABLE INCREMENTS	ACCURACY	SOURCE/SINK CURRENT	DISPLAY	POWER	CASE/ MOUNTING
DVC-350A	±1.2000 or ±12.000	100 µV or 1 mV	0.015%	20 mA	4 1/2 DIGIT LCD	9V Battery or 115 VAC Adaptor (optional)	5.75 X 3.60 X 1.29 in (146 X 91 X 33 mm) HAND HELD
DVC-8500	±19.999	1 mV	0.005%	25 mA	4 1/2 DIGIT MECHANICAL	100 VAC (J) 115 VAC (A) 230 VAC (E)	5.59 X 2.11 X 5.78 (142 X 54 X 147 mm)

DIGITAL PANEL METERS

	Model	Power	Std. Input	Case	Features
3.5 Digit LED	DM-3100L-1	+5Vdc	±2Vdc	B	Short Depth Case
	DM3100N-1	+5Vdc	±2Vdc	A	Provisions for 4-20 mA input
	DM-3101-1	+5Vdc	±2Vdc	A	High Intensity Display
	DM3103-1	+5Vdc	±2Vdc	B	High Intensity Display
	DM-31-1	+5Vdc	±2Vdc		Low Cost - Uncased
	DM-3100B-1	115/230VAC	±2Vdc	B	Short Depth Case
	DM3104-1	115/230VAC	±2Vdc	B	High Intensity Display
	DM-9115-1	115/230VAC	±2Vdc	C	NEMA 12 (Vibration Std)
4.5 Digit LED	DM-4101N-1	+5Vdc	±2Vdc	A	High Intensity Display
	DM-9200-1	+5Vdc	±2Vdc	C	NEMA 12 (Vibration Standard)
	DM-4100D-1	+5Vdc	±2Vdc	A	High Speed Sampling Serial/ParallelBCD Output
	DM-4101D-1	+5Vdc	±2Vdc	A	High Intensity Display Serial/Parallel BCD Output
	DM-4101L-1	+5Vdc	±2Vdc	B	Serial BCD Output
	DM-4200-1	+5Vdc	±2Vdc	A	Serial BCD Output
	DM-9215-1	115/230VAC	±2Vdc	C	NEMA 12 (Vibration)
3.5 Digit LCD	DM-3100U-1	+5/9Vdc	±2Vdc	A	Units Display (Batt. Pwr.)
	DM-3100X-1	+5/9Vdc	±2Vdc	B	Battery Powered
	DM-3102A	+5Vdc	±2Vdc	A	Units Display Autoranging (200 mV - 200V)
	DM-LX3-1	+5Vdc	±2Vdc		Low Cost - Uncased
	DM-3100U2	115VAC	±2Vdc	A	Units Display
4.5 Digit LCD	DM-4105-1	+5Vdc	±2Vdc	A	Serial BCD OUT (Batt. Pwr.)
Other Digital Panel Products	DBM-20	+5Vdc	Adjustable	A	20 Segment LED Bar Graph w/ TTL Outputs
	PC-6	+5Vdc		B	10 MHz Counter/Timer

NOTE: Input range kits are available for all DM-3100, 4100, and 9000 Series DPMs

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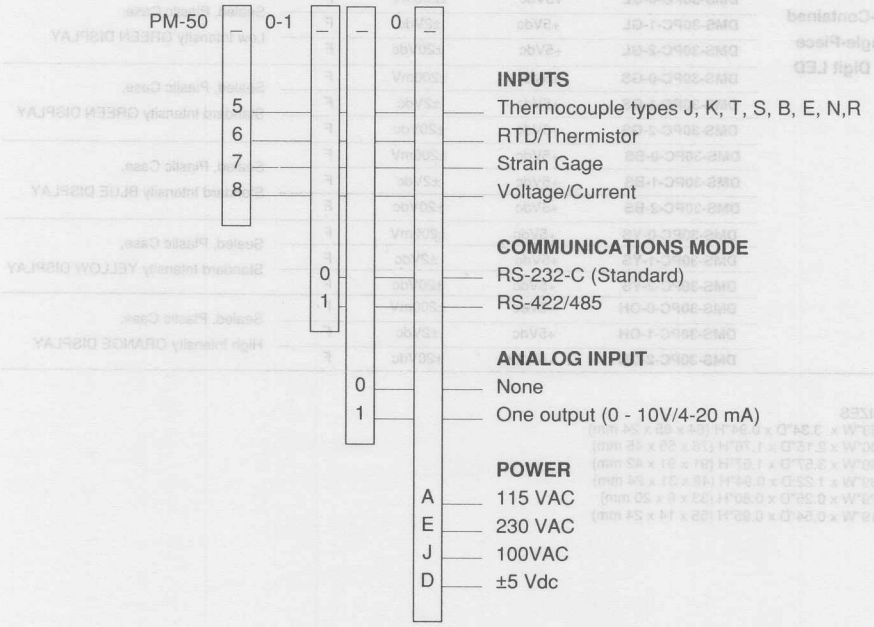
3.5 DIGIT, MINIATURE VOLTAGE METERS

	Model	Power	Std. Input	Case	Features
NEW Self-Contained 3.5 Digit LED Ultra-Miniature	DMH-30PC-0	+5Vdc	±200 mV	E	Encapsulated (Plastic), 24-pin DDIP
	DMH-30PC-1	+5Vdc	±2Vdc	E	Encapsulated (Plastic), 24-pin DDIP
	DMH-30PC-2	+5Vdc	±20Vdc	E	Encapsulated (Plastic), 24-pin DDIP
	DMH-30MM-0	+5Vdc	±200mV	E	Hermetically Sealed, Quartz window, Ceramic 24-pin DDIP, MIL-D-87157 Temperature Range
	DMH-30MM-1	+5Vdc	±2Vdc	E	
	DMH-30MM-2	+5Vdc	±20Vdc	E	
NEW Self-Contained Single-Piece 3.5 Digit LED	DMS-30PC-0-RL	+5Vdc	±200mV	F	Sealed, Plastic Case, Low Intensity RED Display
	DMS-30PC-1-RL	+5Vdc	±2Vdc	F	
	DMS-30PC-2-RL	+5Vdc	±20Vdc	F	
	DMS-30PC-0-RS	+5Vdc	±200mV	F	Sealed, Plastic Case, Standard Intensity RED DISPLAY
	DMS-30PC-1-RS	+5Vdc	±2Vdc	F	
	DMS-30PC-2-RS	+5Vdc	±20Vdc	F	
	DMS-30PC-0-RH	+5Vdc	±200mV	F	Sealed, Plastic Case, High Intensity RED DISPLAY
	DMS-30PC-1-RH	+5Vdc	±2Vdc	F	
	DMS-30PC-2-RH	+5Vdc	±20Vdc	F	
	DMS-30PC-0-GL	+5Vdc	±200mV	F	Sealed, Plastic Case, Low Intensity GREEN DISPLAY
	DMS-30PC-1-GL	+5Vdc	±2Vdc	F	
	DMS-30PC-2-GL	+5Vdc	±20Vdc	F	
	DMS-30PC-0-GS	+5Vdc	±200mV	F	Sealed, Plastic Case, Standard Intensity GREEN DISPLAY
	DMS-30PC-1-GS	+5Vdc	±2Vdc	F	
	DMS-30PC-2-GS	+5Vdc	±20Vdc	F	
	DMS-30PC-0-BS	+5Vdc	±200mV	F	Sealed, Plastic Case, Standard Intensity BLUE DISPLAY
	DMS-30PC-1-BS	+5Vdc	±2Vdc	F	
	DMS-30PC-2-BS	+5Vdc	±20Vdc	F	
	DMS-30PC-0-YS	+5Vdc	±200mV	F	Sealed, Plastic Case, Standard Intensity YELLOW DISPLAY
	DMS-30PC-1-YS	+5Vdc	±2Vdc	F	
	DMS-30PC-2-YS	+5Vdc	±20Vdc	F	
	DMS-30PC-0-OH	+5Vdc	±200mV	F	Sealed, Plastic Case, High Intensity ORANGE DISPLAY
	DMS-30PC-1-OH	+5Vdc	±2Vdc	F	
	DMS-30PC-2-OH	+5Vdc	±20Vdc	F	

CASE SIZES
A 2.53"W x 3.34"D x 0.94"H (64 x 85 x 24 mm)
B 3.00"W x 2.15"D x 1.76"H (76 x 55 x 45 mm)
C 3.60"W x 3.57"D x 1.67"H (91 x 91 x 42 mm)
D 1.89"W x 1.22:D x 0.94"H (48 x 31 x 24 mm)
E 1.29"W x 0.25"D x 0.80"H (33 x 6 x 20 mm)
f 2.19"W x 0.54"D x 0.95"H (55 x 14 x 24 mm)

PROCESS MONITORS/CONTROLLERS

DATEL designs and manufactures a complete line of Process Monitors/Controllers supporting Thermocouples, RTDs, Strain Gages, and Voltage/Current signal inputs. These low cost units contain such features as built-in RS-232 serial port (RS-422/485 optional), user-selectable setpoint outputs (up to 4 discrete and 1 optional Analog), built-in configuration and setup command set, fully isolated inputs (to 1500 Volts, typ.) and a six-character, 14-segment vacuum fluorescent display (blue-green). Each model may be configured and operated from either the front panel or via the serial port. For reliability, accuracy, and low price, DATEL's PM-5000 series Process Monitors/Controllers are simply the best.



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PANEL MOUNT THERMAL PRINTERS

Model	Columns	Input Interface	Power (Note 1)	Character Set	Case	Special Features
DPP-Q7	7	BCD	115/230 VAC	Numeric (decimal or hex) plus sign	A	Simple DATEL DPM interface
APP-20A1	20	Parallel	115/230 VAC	96 char ASCII	A	Inverted, tall character options
APP-20D1	20	Parallel	+12 Vdc	96 char ASCII	A	Inverted, tall character options
APP-A20A21	20	RS-232/20 mA loop	115/230 VAC	96 char ASCII	A	Inverted, tall, condensed character options
APP-A20D21	20	RS-232/20 mA loop	+12 Vdc	96 char ASCII	A	
APP-20A3	20	IEEE-488	115/230 VAC	96 char ASCII	A	Inverted, tall character options
MPP-20A	20	RS-232/Parallel	115 VAC	127 char ASCII	A	Inverted, tall, enhanced character options
MPP-20D	20	RS-232/Parallel	+12 Vdc	127 char ASCII	A	
MPP-20E	20	RS-232/Parallel	230 VAC	127 char ASCII	A	
APP-48A1	48	Parallel	115 VAC	192 char ASCII	B	Inverted character options
APP-48A2	48	RS-232	115/230 VAC	192 char ASCII	B	Inverted character options
APP-48D2	48	RS-232	+12 Vdc	192 char ASCII	B	Inverted character options
APP-48A3	48	IEEE-488	115/230 VAC	192 char ASCII	B	Inverted character options
APP-48D3	48	IEEE-488	+12 Vdc	192 char ASCII	B	Inverted character options
APP-M20A1	20	Parallel	115/230 VAC	96 char ASCII	C	Hardened for shock, vibration and humidity (mobile)
APP-M20A21	20	RS-232	115/230 VAC	96 char ASCII	C	
APP-M20D21	20	RS-232	+12 Vdc	96 char ASCII	C	
APP-M48D1	48	Parallel	+12 Vdc	192 char ASCII	D	
APP-M48D2	48	RS-232	+12 Vdc	192 char ASCII	D	
NEW **GPP-42**	42	Serial/Parallel	115/230 VAC (50/60 Hz)	256 char ASCII	E	8 International Character Sets High Res Graphics, 200 Line Buffer CUSTOM CHARACTERS AVAILABLE

NOTE 1. 100 VAC versions available for most models ("J" version); European line cords also available ("E" version). Consult factory.

CASES

A = 4.44"W x 2.76"H x 8.00"D
B = 8.20"W x 2.84"H x 8.14"D
C = 5.36"W x 3.74"H x 8.00"D (Including mobile-mount brackets)
D = 9.25"W x 3.25"H x 10.44"D (Including mobile-mount brackets)
E = 8.20"W x 2.84"H x 10.50"D

MULTIBUS I BOARDS

Model	A/D Channels	A/D Resolution	A/D Speed	PGA	In/Out Ranges	D/A Channels	D/A Resolution	Notes
ST-702	8 D Isolated 1 KV	13 Bits	33 ms	x50, x100	5V Down to 50 mV	None	- -	Direct thermocouple connections, on board linearize and CJC
ST-711 ST-732	32S / 16D	12 Bits	20 µs	x1 to x1 K Software	5V, 10V Down to 50 mV	2 (732)	12 Bits	On board start timer, Interrupt
ST-703	None	- -	- -	- -	2.5V to 10V 4 to 20 mA	4 Isolated	12 Bits	350V Isolation per channel
ST-724	None	- -	- -	- -	5V, 10V 4 to 20 mA	4	12 Bits	
ST-728	None	- -	- -	- -	5V, 10V 4 to 20 mA	4 or 8	12 Bits	
ST-716	None	- -	- -	- -	5V, 10V	4 or 8	16 Bits	
ST-705	8 D	13 Bits	33 ms	x1 to x200	4V Down to 20 mV	None	- -	RS-232 subsystem and CPU, Direct thermocouple connection, linearize, CJC
ST-519	TTL discrete I/O	- -	- -	- -	TTL	- -	- -	72 TTL lines, In/Out, Interrupt

PC/AT A/D-D/A BOARDS

Model	A/D Channels	A/D Resolution	A/D Speed	Prog. Gain Amplifier	In/Out Ranges	D/A Channels	D/A Resolution	Notes
PC-414A	4 SE w/simul sampling	12 Bits	1.5 MHz	x1 or x10	5V, 10V, 1V	1	12 Bits	4K-sample FIFO memory, analog trigger, parallel data port, counter/timer, DMA Vectored interrupt
PC-414B	4 SE	14 Bits	500 KHz	---	5V, 10V	1	12 Bits	
PC-414C	4 SE	12 Bits	1 MHz	---	5V, 10V	1	12 Bits	
PC-414D	1 SE	12 Bits	4 MHz	---	1V	1	12 Bits	
PC-414E	16 SE	12 Bits	400 KHz	x1 to x100	10V to 100 mV	1	12 Bits	
PC-430A	4 SE w/simul sampling	12 Bits	1.5 MHz	x1 or x10	5V, 10V, 1V	None	---	Local 32 MHZ 320C30 DSP, 512K memory,DMA Fast "no prgmg" command executive, DSP library, Vectored interrupt
PC-430B	4 SE	14 Bits	500 KHz	---	5V, 10V	None	---	
PC-430C	4 SE	12 Bits	1 MHz	---	5V, 10V	None	---	
PC-430D	1 SE	12 Bits	4 MHz	---	1V	None	---	
PC-430E	16 SE	12 Bits	400 KHz	x1 to x100	10V to 100 mV	None	---	
PC-462	4 Monitor Channels	12 Bits	25 KHz	---	0 to ±15V or 5V, 10W	2 Isolated, V or I mode	12 Bits	Programmable power DAC

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

VMEBUS A/D - D/A BOARDS

Model	A/D Channels	A/D Resolution	A/D Speed	Prog. Gain Amplifier	In/Out Ranges	D/A Channels	D/A Resolution	Notes
DVME-601A	16 S/ 8 D Expandable to 256	12 Bits	20 µs	x1 to x1K	5, 10V down to 50 mV	None	---	68010 CPU 256K memory RS-232, 5 TTL I/O Counter/Timers "No prgmg" Command Exec. Vectored interrupt
DVME-601B		12 Bits	4 µs					
DVME-601C		16 Bits	35 µs					
DVME-601D		16 Bits	400 ms					
DVME-601E		12 Bits	2 µs					
DVME-611/612A	32 S / 16 D Expandable to 256	12 Bits	20 µs	x1 to x128 Software Pgmble	5V, 10V down to 50 mV	2 (612)	12 Bits	Short I/O SA:16, SD:16 Vectored interrupt
DVME-611/612B		12 Bits	4 µs					
DVME-611/612C		16 Bits	35 µs					
DVME-611/612D		16 Bits	400 ms					
DVME-611/612E		12 Bits	2 µs					
DVME-611/612F		14 Bits	4 µs					
DVME-613	16 S/8 D Isolated 500V	12-14-16 Bits	40 µs	x1 to x100	5V, 10V down to 50 mV	None	---	8 In/8 Out TTL, SA:24, SD:16 Start timer, interrupt
DVME-624	None	---	---	---	2.5 to 10V 4 to 20 mA	4 Isolated	12 Bits	SA:16, SD:16 350V Isolation
DVME-626	None	---	---	---	5V, 10V	6	16 Bits	SA:16, SD:16
DVME-628	None	---	---	---	2.5 to 10V 4 to 20 mA	8	12 Bits	SA:16, SD:16
DVME-641	32 S/16 D	Slave MUX board	6 µs Settling	---	5V, 10V 4 to 20 mA	---	---	Slave input expander to 601, 611, 612
DVME-643	8D Isolated	Slave MUX board	2.5 ms Settling	x50, x100	5V Down to 50 mV	---	---	Slave input expander to 601, 611, 612
DVME-645	16 S/8D	Slave MUX board	6 µs Settling	---	5V, 10V	---	---	Simultaneous Sample/Hold Expander to 601, 611, 612
DVME-614A	4 Simul. S/H	12 Bits	1.5 MHz	x1 or x10	1V, 5V, 10V	1	12 Bits	4K-sample FIFO memory Analog trigger Parallel data port Sample counter/timer Simultaneous sampling Vectored interrupt
DVME-614B	4 S	14 Bits	500 KHz	---	5V, 10V			
DVME-614C	4 S	12 Bits	1 MHz		5V, 10V			
DVME-614D	1 S	12 Bits	4 MHz		5V, 10V			
DVME-614E	16 S	12 Bits	400 KHz	x1 to x100	1, 5, 10V, 100mV			
DVME-630A	4 Simul. S/H	12 Bits	1.5 MHz	x1 or x10	1V, 5V, 10V	None	---	Local 32 MHz 320C30 DSP, 512 K Memory, Fast "no prgmg" command Executive, Interrupt DSP library
DVME-630B	4 S	14 Bits	500 KHz	---	5V, 10V			
DVME-630C	4 S	12 Bits	1 MHz		5V, 10V			
DVME-630D	1 S	12 Bits	4 MHz		5V, 10V			
DVME-630E	16 S	12 Bits	400 KHz	x1 to x100	1, 5, 10V, 100mV			
DVME-622	None	---	---	---	5V, 10V	16 Simul. Update	12 Bits	3 µs settling per channel
DVME-621	None	---	---	---	5V, 10V @ 100 mA or 160 mA	4 Isolated	12 Bits	Power DAC's, voltage or current mode, active drivers, 500V isolation

HIGH-RELIABILITY PROGRAMS

DATEL is committed to meeting the demading requirements of military, aerospace, and severe environment applications. Toward that end, DATEL offers several options in its quality program.

OPTION 1 — MIL-STD-883 Class H Compliant Devices

DATEL Inc. is **QUALIFIED** by the Defense Electronics Supply Center for the manufacture of selected hybrid microcircuits in **FULL COMPLIANCE** with Military Specification **MIL-H-38534** (Hybrid Microcircuits), FSC 5962, and **MIL-STD-1772 SECTION B**.

The accompanying chart gives a concise overview of MIL-STD-883 screening requirements and their implications for DATEL customers.

TEST	METHOD	PURPOSE
Internal Visual (Precap)	Method 2017	Eliminates devices with potential for failure under mechanical, electrical, or thermal stress.
Stabilization Bake	Method 1008, Test Condition C, 24 hrs. at 150 °C	Eliminates device failure due to storage at elevated temperatures.
Temperature Cycling	Method 1010, Test Condition C, -65 to 150 °C	Determines resistance of device to sudden exposure to extreme temperature changes. Removes potential failures due to thermal stress on bonds, etc.
Constant Acceleration	Method 2001, Test Condition A, Y AXIS, 5 kg.	Eliminates potential failures due to structural or mechanical weakness not detected in shock or vibration test.
Burn-in Test	Method 1015, Test Condition B, 160 hrs. at +125 °C	Stresses devices at temperature in order to eliminate infant mortality failures.
PDA 10%	Static Tests performed at +25 °C	Percent defective allowable - Rejects lots with static test failures greater than 10%.
Final Electrical Test	Performed at +25 °C and at max. and min. operating temperatures	Verifies that device still meets specified data sheet parameters.
Seal Fine and Gross	Method 1014, Test Condition A (fine), 1 x 10^{-7} cc/Sec. for volume of ≥0.5 to <1.0 cm^3 and 5 x 10^{-8} cc/Sec. for volume of ≥1.0 to <10.0 cm^3. Test Condition C (gross)	Insures hermeticity of device package. Eliminates degradation due to absorption of water vapor or other contaminants.
External Visual	Method 2009	Insures that materials, design, construction, marking, and workmanship conform with applicable procurement documentation.

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

MIL-STD-883 compliancy also requires that complete documentation be available to support the product. An analysis of the design along with element and package evaluations are performed to ensure a high quality product. The manufacturing process is also stringently controlled in order to obtain the high quality level.

Initial qualification requires passing the MIL-STD-883 test for groups A, B, C, and D. After initial qualification, groups A & B are tested for all lots. Group C is tested initially and to qualify any product changes which may occur. Group D testing is also performed initially and at intervals not exceeding 6 months for future lots.

MIL-STD-883 PRODUCTS

ANALOG-TO-DIGITAL CONVERTERS

MODEL NO.	RESOLUTION	CONVERSION TIME	LINEARITY
ADC-HZ12B/883B	12 Bits	8 µSec	±1/2 LSB
ADC-HX12B/883B	12 Bits	20 µSec	±1/2 LSB
ADC-816/883B	10 Bits	800 nSec	±1/2 LSB
ADC-511/883B	12 Bits	1 µSec	±3/4 LSB
ADC-228/883B	8 Bits	4 nSec	±1/2 LSB
ADC-208/883B	8 Bits	50 nSec	±1.5 LSB
ADC-207/883B	7 Bits	50 nSec	±1 LSB
ADS-111/883B	12 Bits	500 KHz	±3/4 LSB

DIGITAL-TO-ANALOG CONVERTERS

MODEL NO.	RESOLUTION	SETTLING TIME	LINEARITY
DAC-HZ12B/883B	12 Bits	3 µSec	±1/2 LSB
DAC-HP16B/883B	16 Bits	15 µSec	±2 LSB
DAC-HK12B/883B	12 Bits	3 µSec	±1/2 LSB
DAC-HF12/883B	12 Bits	50 nSec	±1/2 LSB
DAC-HF10/883B	10 Bits	25 nSec	±1/2 LSB
DAC-HF8/883B	8 Bits	25 nSec	±1/2 LSB

DATA ACQUISITION SUBSYSTEMS

MODEL NO.	RESOLUTION	INPUT CHANNELS	THROUGHPUT
HDAS-76/883B	12 Bits	4 Diff.	75 KHz
HDAS-75/883B	12 Bits	8 SE	75 KHz
HDAS-16/883B	12 Bits	16 SE	50 KHz
HDAS-8/883B	12 Bits	8 Diff.	50 KHz

MULTIPLEXERS

MODEL NO.	CHANNELS	SETTLING TIME	ACCESS TIME
MX-826/883B	8 SE	200 nSec	70 nSec

SAMPLE-AND-HOLD AMPLIFIERS

MODEL NO.	LINEARITY	ACQUISITON TIME	BANDWIDTH
SHM-4860/883B	0.01%	200 nSec	16 MHz

OPTION 2 — DATEL QL SCREENING PROGRAM

TEST	TEST CONDITION	PURPOSE
Internal Visual (100% Precap)	Test Method 2017	Eliminate visual defects prior to seal
Stabilization Bake 100%	TM 1008, Condition C 24 hours at + 150 °C (Optional if TM 1030 is used)	Eliminates failures due to high temp storage
Temperature Cycling, 100%	TM 1010, Condition C -65 to +150 °C, 10 cycles	Eliminates failures due to mechanical weakness
100% Constant Acceleration	TM 2001, Condition A Y1 Axis, 5000 G	Eliminates failures due to mechanical weakness
100% Burn-in	Static burn-in 160 hrs. at +125 °C (Similar to TM 1015 or TM 1030)	Eliminates failures due to infant mortality
100% Final Electrical Test	Performed at +25 °C, T_{MIN}, and T_{MAX} operating temperatures	Verifies that devices meet speicifications over temperature range
100% Fine and Gross Leak	Test Method 1014 Condition A (fine) 5×10^{-7} cc/Sec. Condition C (gross)	Insures hermeticity for high humidity environments
100% External Visual	Test Method 2009	Insures proper marking, construction, workmanship

-QL PRODUCTS

SAMPLE-HOLD AMPLIFIERS

MODEL NO.	LINEARITY	ACQUISITION TIME	HOLD MODE DROOP
SHM-45MM-QL	0.01%	200 nSec.	0.5 µV/µSec.
SHM-4860MM-QL	0.01%	200 nSec.	0.5 µV/µSec.
SHM-6MM-QL	0.02%	2 µSec.	10 µV/µSec.
SHM-HUMM-QL	0.1%	25 nSec.	50 µV/µSec.

OPERATIONAL AMPLIFIERS

MODEL NO.	INPUT OFFSET VOLTAGE	GAIN BANDWIDTH	OUTPUT
AM-500MM-QL	3 mV	130 MHz	+10V at 50 mA
AM-1435MM-QL	5 mV	1000 MHz	+ 7V at 14 mA

DATA ACQUISITION SUBSYSTEMS

MODEL NO.	RESOLUTION	INPUT CHANNELS	THROUGHPUT
HDAS-16MM-QL	12 Bits	16 Single-Ended	50 KHz

DATEL, Inc. 11 Cabot Boulevard, Mansfield, MA 02048-1194/TEL (508) 339-3000/TLX 174388/FAX (508) 339-6356

ANALOG-TO-DIGITAL CONVERTERS

MODEL NO.	RESOLUTION	CONVERSION TIME	LINEARITY
ADC-817AMM-QL	12 Bits	2 µSec.	± 1 LSB
ADC-HX12BMM-QL	12 Bits	20 µSec.	± 1/2 LSB
ADC-HC12BMM-QL	12 Bits	300 µSec.	± 1/2 LSB
ADC-815MM-QL	8 Bits	700 nSec.	± 1/2 LSB
ADC-825MM-QL	8 Bits	1 µSec.	± 1/2 LSB

SAMPLING ANALOG-TO-DIGITAL CONVERTERS

MODEL NO.	RESOLUTION	SPEED	LINEARITY
ADC-HS12BMM-QL	12 Bits	66 KHz	± 1/2 LSB

DIGITAL-TO-ANALOG CONVERTERS

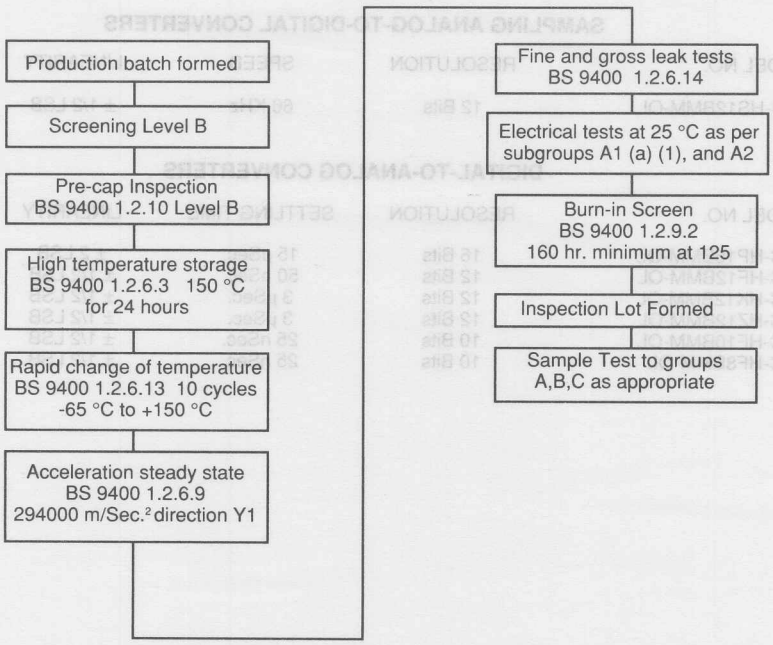
MODEL NO.	RESOLUTION	SETTLING TIME	LINEARITY
DAC-HP16BMM-QL	16 Bits	15 µSec.	± 2 LSB
DAC-HF12BMM-QL	12 Bits	50 nSec.	± 1/2 LSB
DAC-HK12BMM-QL	12 Bits	3 µSec.	± 1/2 LSB
DAC-HZ12BMM-QL	12 Bits	3 µSec.	± 1/2 LSB
DAC-HF10BMM-QL	10 Bits	25 nSec.	± 1/2 LSB
DAC-HF8BMM-QL	10 Bits	25 nSec.	± 1/2 LSB

OPTION 3 — BS9000 PROGRAM

DATEL also has a BS9000 program in compliance with British Standards for high reliability devices. BS9000 is the United Kingdom's national system for the independent inspection approval and surveillance of manufacturers, distributors and test laboratories in the electronic component industry.

The accompanying product flow gives an overview of the BS9000 products through screening and quality conformance inspection.

BS9000 Screening Requirements



BS9000 PRODUCTS

ANALOG-TO-DIGITAL CONVERTERS

MODEL NO.	RESOLUTION	CONVERSION TIME	LINEARITY
ADC-208MM-BS9400-G0140	8 BITS	66 nSec	±2 1/2 LSB
ADC-303MM-BS9400-G0106	8 BITS	10 nSec	±3/4 LSB
ADC-303JM-BS9400-G0106	8 BITS	10nSec	±3/4 LSB
ADC-304MM-B29400-G0177	8 BITS	50 nSec	±1/2 LSB

Parts qualified to the BS9000 specification have a quality level equivalent to MIL-M-38510 giving a quality factor of 1.

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DESC STANDARD MILITARY DRAWING PROGRAM

The Standard Military Drawing (SMD) program is a program administered by the Defense Electronics Supply Center (DESC) in Dayton, Ohio. Under this program a certified MIL-STD-1772 manufacturer, such as DATEL Inc., may supply a hybrid device using one government controlled Source Control Drawing (SCD). This saves both the customer and supplier time and effort.

DATEL Inc. is an active participant in the DESC SMD program. At publication time the following DESC Dreawing numbers have been assigned and are approved or are pending approval. Please contact DATEL Inc. for current status and future SMD compliant products.

DESC DRAWING NUMBER	DATEL MODEL NUMBER
5962-88508	ADC-HX/883B
5962-88508	ADC-HZ/883B
5962-89528	DAC-HKB/883B
5962-89528	DAC-HKB-2/883B
5962-89531	DAC-HPB/883B
5962-89531	DAC-HPB-1/883B
5962-90857	ADC-208/883B (pending)
5962-89996	DAC-HF8/883B (pending)
5962-89996	DAC-HF10/883B (pending)
5962-89996	DAC-HF12/883B (pending)
5962-88514	HDAS-8/883B (pending)
5962-88514	HDAS-16/883B (pending)

STILL AVAILABLE

The following older DATEL component products have not been included in this new databook. For new designs the component products offered in this databook will provide economically superior performance. For existing designs we at DATEL are committed to supplying our older products to our customers for as long as possible and practical. Please contact our Sales Department for information regarding price, delivery, and minimum order quantity on any of the following.

ADC-B500
ADC-B500-1
ADC-B505
ADC-B304
ADC-ECONOVERTER-EXX-HS
ADC-EHB1-EXX-HS-BUO4
ADC-EH10B1
ADC-EH10B2
ADC-EH12B2
ADC-EH12B3
ADC-EH8B1
ADC-EH8B2
ADC-EK10B
ADC-EK12B
ADC-EK12DC
ADC-EK12DM
ADC-EK12DR
ADC-EK8B
ADC-ET10BC
ADC-ET10BM
ADC-ET12BC
ADC-ET12BM
ADC-ET12BR
ADC-ET8BC
ADC-ET8BM
ADC-E12B4
ADC-E12D2
ADC-E12D2-EX
ADC-E12D3
ADC-HX12BMM-QL
ADC-HZ12BMM-QL
ADC-MC8BC
ADC-MC8BM
ADC-149-14B
ADC-32AC
ADC-32C
ADC-32M
ADC-33C
ADC-33M
ADC-510MC
ADC-510MM
ADC-5101
ADC-574AT
ADC-574ZA
ADC-574ZB
ADC-574ZC
ADC-674ZA
ADC-674ZB
ADC-674ZC
ADC-7109
ADC-800
ADC-810MC
ADC-810MM
ADC-811MC
ADC-811MM
ADC-815MC
ADC-815MM
ADC-815MM-QL
ADC-816/883B
ADC-816MC
ADC-816MM
ADC-817AMC
ADC-817AMM
ADC-817AMM-QL
ADC-825MC
ADC-825MM
ADC-825MM-QL
ADC-826MC
ADC-826MM
ADC-827AMC
ADC-830C
ADC-847A
ADC-847B
ADC-847M
ADC-856C
ADC-856M
ADC-881
ADC-974
ADS-105MC
ADS-106MC
ADS-125MC
AM-227
AM-427-1A
AM-427-1B
AM-427-2B
AM-427-2M
AM-430A
AM-430B
AM-450-2
AM-450-2M
AM-452-2
AM-452-2M
AM-460-2
AM-462-2
AM-464-2
AM-464-2M
AM-543MC
DAC-DG12B1
DAC-DG12B1-EXX-HS-BU04
DAC-DG12B2
DAC-DG12B2-EXX-HS
DAC-HB12B
DAC-HB8B-EXX
DAC-HF10BMM-QL
DAC-HF12BMM-QL
DAC-HF8BMM-QL
DAC-HI10B
DAC-HI10B-EXX-HS-BU04
DAC-HI12B
DAC-HI-12B-EXX-HS
DAC-HI8B
DAC-HI8B-EXX-HS-BU04
DAC-HK-12BMM-QL
DAC-HK12BMM-2-QL
DAC-HP16BMM-QL
DAC-HP16BMM-1-QL
DAC-HZ12BMM-QL
DAC-IC10B
DAC-IC10BC
DAC-IC10BM
DAC-I10B
DAC-I10B-EXX-HS
DAC-I12B
DAC-I12B-EXX-HS-BU04
DAC-I12D
DAC-UP10BC
DAC-UP8BC
DAC-08BC
DAC-08BM
DAC-0805MR
DAC-169-16B
DAC-169-16D
DAC-298B
DAC-4910B
DAC-4912D
DAC-562C
DAC-562M
DAC-608C
DAC-610C
DAC-612C
DAC-7134BL
DAC-7134UL
DAC-7523
DAC-7533
DAC-7541
DAC-8308
HDAS-16MM-QL
MDAS-16
MDAS-8D
MDAS-940D
MDAS-940S
MS-13
MS-6
MS-7
MVD-409
MX-1606M
SCM-100A
SCM-100B
SCM-101
SDAS-8A1
SDAS-8A2
SDAS-8A3
SDAS-8E1
SHM-IC-1
SHM-IC-1M
SHM-LM-2
SHM-UH
SHM-UH3
SHM-2
SHM-2-EXX-HS-BU04
SHM-2E
SHM-2E-EXX-HS
SHM-5
SHM-5-EXX-HS-BU04
VFQ-1C
VFQ-1R
VFQ-2C
VFQ-3C
VFV-10K
VFV-100K
VI-7660-1
VI-7660-2
VR-182A
VR-182B
VR-182C

SUBSTITUTION GUIDE FOR DISCONTINUED COMPONENT PRODUCTS

The following products are no longer available from DATEL. Where applicable, the nearest equivalent DATEL replacement is listed. Some of these replacement products are functionally similar only and may not be pin-for-pin compatible with the discontinued product.

Discontinued Model	Nearest Equivelent
ADC-300	ADC-208
ADC-301	None
ADC-302	None
ADC-303	None
ADC-310	None
ADC-508MM	ADC-505BMM
ADC-515BMC	ADC-500BMC
ADC-515BMM	ADC-500BMM
ADC-520MM	ADC-505BMM
ADC-521MM	ADC-505BMM
ADC-7109	ADC-ET Series
ADC-810MM-QL	ADC-511/883B
ADC-816MM-QL	ADC-511/883B
ADC-826MM-QL	ADC-511/883B
ADC-827AMM	ADC-817AMM
ADC-B300E	None
ADC-B301E	None
ADC-B302E	None
ADC-B303	None
ADC-B310E	None
ADS-105MM	ADS-112MM
ADS-106MM	ADS-112MM
ADS-115MC	ADS-112MC
ADS-115MM	ADS-112MM
ADS-116MC	ADS-112MC
ADS-116MM	ADS-112MM
ADS-125MM	ADS-112MM
ADS-126MC	ADS-112MC
ADS-126MM	ADS-112MM
ADS-21AC	ADS-21PC
ADS-22AC	ADS-21PC
AM-100 Series	AM-551
AM-200 Series	AM-543MC
AM-427-2A	AM-427-2B
AM-453-2C/2M	AM-450-2
AM-460-2M	AM-450-2M
AM-7650-1/-2	None
DAC-330	DAC-HF10
DAC-7134BJ/BK/UJ/UK	DAC-7134BL/UL
DAC-VR Series	DAC-HK12
DAS-952R	None
DILS-1,2,3*	None
HDAS-8MM-QL	HDAS-8/883B
MS-11*	None
MS-12*	None
MS-2*	None
MS-3*	None
MS-4*	None
MS-5*	None
MS-9*	None
SCM-103/102	None
SHM-LM-2M	SHM-IC-1M
SHM-360	None
SHM-361	None
SHM-9 Series	SHM-IC-1
TP Series*	None

*Available through distributors

SUBSTITUTION GUIDE FOR DISCONTINUED COMPONENT PRODUCTS

The following products are no longer available from DATEL. Where applicable, the nearest equivalent DATEL replacement is listed. Some of these replacement products are functionally similar only and may not be pin-for-pin compatible with the discontinued product.

Discontinued Model	Nearest Equivalent
ADC-300	ADC-208
ADC-301	None
ADC-302	None
ADC-303	None
ADC-310	None
ADC-508MM	ADC-505BMM
ADC-512BMC	ADC-500BMC
ADC-512BMM	ADC-500BMM
ADC-520MM	ADC-505BMM
ADC-521MM	ADC-505BMM
ADC-710B	ADC-ET Series
ADC-810MM-CL	ADC-511/883B
ADC-816MM-CL	ADC-811/883B
ADC-826MM-CL	ADC-511/883B
ADC-827AMM	ADC-817AMM
ADC-830CE	None
ADC-831CE	None
ADC-832CE	None
ADC-833	None
ADC-837CE	None
ADS-105MM	ADS-112MM
ADS-106MM	ADS-112MM
ADS-115MC	ADS-112MC
ADS-115MM	ADS-112MM
ADS-116MC	ADS-112MC
ADS-116MM	ADS-112MM
ADS-125MM	ADS-112MM
ADS-126MC	ADS-112MC
ADS-126MM	ADS-112MM
ADS-214C	ADS-212PC
ADS-224C	ADS-212PC
AM-100 Series	AM-5651
AM-200 Series	AM-5439MC
AM-427-2A	AM-427-2B
AM-453-2C/2M	AM-450-2
AM-460-2M	AM-450-2M
AM-7850-1/-2	None
DAC-330	DAC-HF10
DAC-713/813/K/U/UK	DAC-713/813U/UL
DAC-VR Series	DAC-HK12
DAS-982P	None
DIL8-1,2,3*	None
HDAS-8MM-CL	HDAS-8/883B
MS-11*	None
MS-12*	None
MS-2*	None
MS-3*	None
MS-4*	None
MS-5*	None
MS-9*	None
SCM-102/102	None
SHM-UM-2M	SHM-IO-1M
SHM-380	None
SHM-381	None
SHM-9 Series	SHM-IO-1
TP Series*	None

*Available through distributors

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DATEL

ORDERING GUIDE

This ordering guide is presented as a procedural guide. For a formal statement of policies, refer to the TERMS AND CONDITIONS OF SALE found on the Quotation form or on the Customer Acknowledgement copy of the Sales Order.

PLACING AN ORDER
When ordering a DATEL product, give the complete model number, product description, and option description. Place orders with a DATEL field sales representative or with the factory by letter, telephone, FAX, or TELEX. *Minimum order and minimum per shipment is $100.*

OUTSIDE THE U.S.A. AND CANADA Place overseas orders with a DATEL Sales Subsidiary (in West Germany, France, the United Kingdom, and Japan) or with a DATEL overseas sales representative. Orders received directly will be treated the same as if placed through our overseas sales representative. In countries without a DATEL representative, orders should be placed by TELEX and confirmed by air mail.

FIELD SALES REPRESENTATIVE
DATEL employs field sales representatives throughout the United States, Canada, Europe, and the Far East. DATEL also has Sales Subsidiaries in Munich, West Germany; Paris, France; London, England; and Tokyo and Osaka, Japan. Only these sales representatives are authorized by DATEL to solicit sales, and any information or data received by sources other than these authorized representatives or the DATEL factory are not considered binding.

PRICES
All prices are F.O.B. , Mansfield, Massachusetts, U.S.A. in U.S. dollars. Applicable federal, state, and local taxes are extra and paid by buyer. Prices are subject to change without notice.

TERMS Net 30 days

DISCOUNTS
Quantity discounts are available when placed in a single order. OEM discounts are available on an order or contract basis; consult the factory for details

QUOTATIONS
Price and delivery quotations made by DATEL or its authorized field sales representatives are valid for 30 days unless otherwise stated.

DELIVERY
DATEL uses an IBM System 4381, for efficient processing of orders. All orders placed with DATEL are acknowledged within a few days by an acknowledgement copy of our sales order form. This copy indicates pertinent information including a formal statement of terms and conditions of sale and estimated delivery date. This date has preference over all other agreed upon dates unless otherwise specified.

DATEL ships all products in rugged commercial containers suitable for insuring safe delivery under normal shipping conditions. Unless shipping method is specified, the best available method will be used. Shipping charges are normally prepaid and billed to the customer except for Air Freight charges which are sent collect. The appropriate data sheet and/or instruction is packed with each product shipped.

ORDER CANCELLATION
All orders entered with DATEL are binding and are subject to a cancellation charge if cancelled before or after the scheduled shipping date appearing on the acknowledgement copy of the sales order form. Refer to DATEL's Standard Terms and Conditions for specific charges.

WARRANTY
DATEL warrants that all of its products are free from defects in material and workmanship under normal use and service for a period of one year from date of shipment. DATEL's obligations under this warranty are limited to replacing or repairing, at its option, at its factory or facility, any of the products which shall within the applicable period after shipment be returned to DATEL's facility, transportation charges prepaid, and which are after examination disclosed to the satisfaction of DATEL to be thus defective. This warranty shall not apply to any such equipment which shall have been repaired or altered except by DATEL or which shall have been subjected to misuse, negligence, or accident. In no case shall DATEL's liablilty exceed the original purchase price. The aforementioned provisions do not extend the original warranty period of any product which has either been repaired or replaced by DATEL.

RETURNS
You will need a **return authorization number** and shipping instructions from the factory when returning products for any reason. Items should not be returned air freight collect as they connot be accepted. It is absolutely necessary to return products in the manner stated here, otherwise considerable delay will result in processing the return.

RETURNS OUTSIDE THE U.S.A. AND CANADA Contact the local sales representative or factory for authorization and shipping instructions first.

CERTIFICATE OF COMPLIANCE
When requested by the customer DATEL will provide a standard Certificate of Compliance with all shipments. This request must be specified on the purchase order.

ANALOG-TO-DIGITAL CONVERTERS
SAMPLING A/D CONVERTERS
FLASH A/D CONVERTERS
DIGITAL-TO-ANALOG CONVERTERS
SAMPLE-AND-HOLD AMPLIFIERS
MULTIPLEXERS
OPERATIONAL AMPLIFIERS
ISOLATION AMPLIFIERS
INSTRUMENTATION AMPLIFIERS
DATA ACQUISITION SUBSYSTEMS
ACTIVE FILTERS
V/F-F/V CONVERTERS
DIGITAL PANEL METERS
CALIBRATORS
PROCESS MONITORS/CONTROLLERS
THERMAL PRINTERS
POWER SUPPLIES
DC/DC CONVERTERS
DATA ACQUISITION BOARDS
DSP/DATA ACQUISITION PRODUCTS

DATEL

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